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Low power flipped voltage follower current mirror with improved input output impedances

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Abstract. High performance sub-volt current mirror are widely used in building mixed-mode low power VLSI systems. The performance of current mirror is decided by its key parameters which includes large operating range, low input compliance voltage, wide swing, large bandwidth along with very low input and very high output resistances. In this paper, a design of high performance low power current mirror is shown. The proposed current mirror is based on flipped voltage follower which enables the current mirror to work at low voltage. For improvement in input output resistance the proposed current mirror is employed with super transistor and super cascode stage. The current mirroring with minimum error is achieved till 1mA with power dissipation in the range of micro watt. The achieved bandwidth is 2.1 GHz along with low input and high output resistances as 0.407 ohm and 50 giga ohm, respectively. The process corner, temperature analysis and noise analysis of the proposed current mirror is also shown in this paper. The complete analysis is done using HSpice on 0.18 um technology at a dual supply voltage of 0.5 V.

Keywords. Current mirror; flipped voltage follower; super transistor; super cascode; input output resistance.

1. Introduction

Current mirror is a circuit which generates the output as a replica of input current at a high impedance node so as to avoid the constant current irrespective of type of load. Its uses can be seen in many applications, like current amplification, comparator design, filtering, as a level shifter, etc. [1, 2]. Current mirror with wide operating range, large bandwidth, low input and high output resistances are some of the key requirements. The simplest widely used configuration is cascode current mirror which provides high output impedance and better accuracy but at the expense of decreased voltage swing and large supply voltage which is not suitable for low voltage low power applications. Being a core block of analog circuits, its efficiency directly affects any IC performance. In this regard, a number of techniques have been reported in literatures which make the current mirror to work efficiently at reduced supply [3]. For example, few highly cited current mirror circuits based on: bulk-driven [4–6], floating gate [7–9], quasi-floating gate [10–13] and bulk-driven quasi-floating gate [14–16] can be easily found in literature. The contributions made were on removal of threshold voltage from the input signal path through auxiliary input and improvement in performance parameters by tuning the input transistor's transconductance as it inversely affects the input resistance and directly affects the bandwidth. However, these types of techniques require special fabrication steps. At present the cell called flipped voltage follower (FVF) [17] is extensively being used to solve the performance issues faced at low supply voltage. Basically FVF is a cascode amplifier with a negative feedback. Compared to conventional voltage follower, the FVF configuration provides very low output impedance which can be used as an input in a current mirror design. Also the supply voltage required for its operation is very low. FVF application in design of analog circuits low voltage current mirrors reported in literature can be found in [18–28].

In this paper, a FVF based current mirror design is proposed which has wide bandwidth with very low input impedance and extremely high output impedance. The current mirroring is carried via FVF block. However, for improvement of current mirror's input and output resistance, the configuration called super transistor [29, 30] is utilized both at the input and output section. This resulted in input resistance lesser than an ohm whereas output impedance in range of mega ohms. Further improvement in output resistance is achieved via super cascode stage [21] which boosts the impedance level from mega ohms to tens of giga ohms. The paper is presented as follows: section 2

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discusses in short the basic understanding of FVF cell. Section 3 briefs about the proposed current mirror design followed with simulation results in section 4. Finally, the conclusions are presented in section 5.

2. Flipped voltage follower

The voltage follower, a common drain configuration (shown in figure 1(a)) also named as source follower is widely used as voltage buffer in analog designs. Under no body effect consideration, the output follows the input voltage with a DC level shift of one gate-source voltage drop, i.e., $V_{out} = V_{in}$-$V_{gs,M1}$. The desired characteristics of voltage follower are high input and relatively low output resistance, high bandwidth and large swing. However, in most of the analog designs the output resistance of conventional voltage follower is sufficient not low enough to meet the requirements. The output resistance of the voltage follower is given as $1/gm_1$ where gm_1 is the transconductance of transistor M_1. Moreover, as the sourcing and sinking capabilities are different the slew rate observed is non-symmetrical in nature. The possible solution reported in literature is the cell called flipped voltage follower (FVF) [17] as shown in figure 1(b). The configuration is basically a cascode with a shunt feedback due to which the output resistance seen in this configuration compared to its conventional design is relatively very low, approximately gets reduced by a factor of gmr_0 (usually ranges in tens of ohms). The effective output resistance for the FVF is given as $1/gm_2gm_{1r01}$ where gm_i and r_{0i} are the transconductance and output resistance of transistor M_i respectively. Besides this the cell offers high current sinking capability, low supply requirement, wide bandwidth and low static power dissipation. The brief on working of FVF can be found in [17].

3. Proposed current mirror

This section details about the complete implementation of the proposed current mirror along with its operation.

Any efficient current mirror includes its definition in terms of its enhanced parameters governing the performance. These parameters include high accuracy in current transfer, low compliance voltage, very low input and very high output resistances, and wide bandwidth. The conventional FVF current mirror circuit is shown in Figure 2. The FVF current mirror consists of four N-channel MOS transistors (M_1-M_4) where transistor M_3 and current source I_{B1} forms a negative feedback due to which a low impedance node is seen at the drain of transistor M_1 [17, 31]. The low impedance node here is fed with the input current I_{in}. The current flowing into M_3 is held constant due to current source I_{B1}. Any variation in the input current is sensed by the transistor M_1 and accordingly produces suitable change in its V_{gs} which modulates the output current (I_{out}). The constant DC voltage V_{bias} is to maintain M_3 and M_4 in saturation regime. The FVF current mirror works at low supply, and possess low input and high output resistance. Performing routing small-signal analysis gives the input and output resistances of the FVF current mirror as ($1/gm_1gm_3r_{03}$) and ($gm_4r_{04}r_{02}$) respectively where g_{mi} and r_{0i} denote the transconductance and output resistance of related transistor. However, the input (output) impedance level is not low (high) enough to fulfill the requirements in many of analog circuits. To fulfill these gaps the current mirror

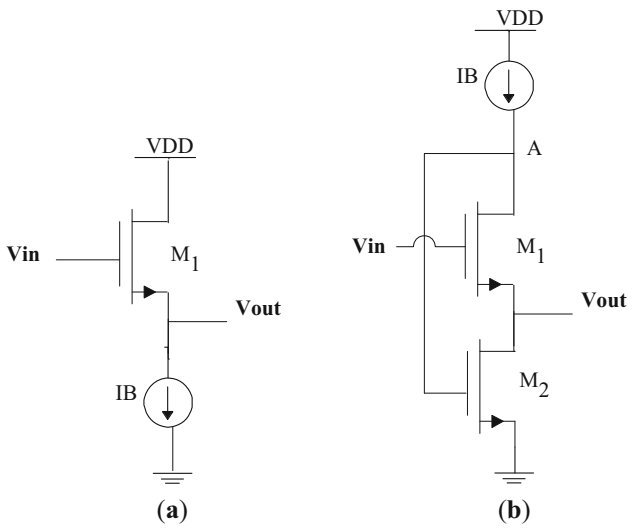

Figure 1. (a) Conventional Voltage follower (common Drain); (b) Flipped voltage follower (FVF).

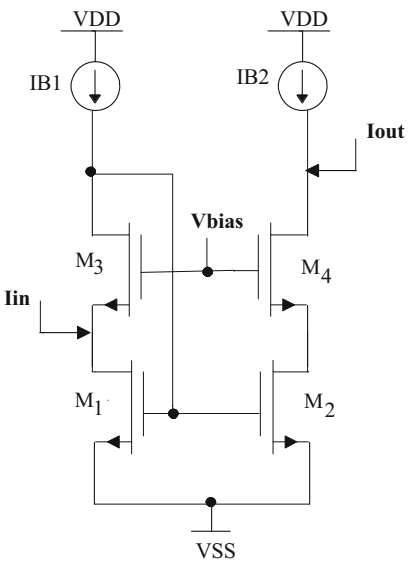

Figure 2. Conventional FVF current mirror.

proposed uses super transistor configuration [30] in the input as well to the output section. Super transistor creates a local negative feedback loop which helps in modulating the resistance level. The proposed FVF current mirror employing super transistor configurations is shown in figure 3.

As seen in the input section, the transistors M_3, M_7 and M_8 with the help of DC current sources I_{B4} and I_{B5} forms super transistor configuration. Here transistor M_7 and M_8 along with M_3 creates a local negative feedback loop which reduces the resistance seen at the drain of M_1 to a very low value. The input resistance compared to conventional FVF is further reduced here is by a factor of $(g_m r_0)^2$. Similarly, in the output section transistors M4, M_5 and M_6 along with DC current sources I_{B2} and I_{B3} forms a super transistor configuration resulting in increased output resistance by a factor of $(g_m r_0)^2$ compared to FVF current mirror. The resulting low input and high output resistances increases the performance of FVF current mirror. Further increment in output resistance of proposed current mirror is done via super cascode structure [21] which provides an additional multiplying factor of $(g_m r_0)^2$. The super cascode stage is implemented using transistor M_9 and M_{10} where M_{10} is driven by the drain potential of M_4 via the inverting amplifier realized using M_9 and I_{B7}. This inverting amplifier stage provides the additional gain-boosting which significantly boost the impedance level. In summary, the total resistance seen at the output is approximately $(g_m r_0)^4$ times higher than conventional FVF current mirror.

3.1 *Small signal analysis*

The symbols used in analysis matches with standard spice model parameters of MOS transistors and have their usual meaning. All the MOS transistors are assumed to be working in saturation region.

3.1a *Input resistance*: The small signal model for calculating the input resistance ($R_{in,prop.}$) of the proposed current mirror is shown in figure 4.

At node 2

$$i_{in} + g_{m3}V_{72} + \frac{V_1 - V_2}{r_{03}} + \frac{V_8 - V_2}{r_{08}} - g_{m8}V_2 = g_{m1}V_1 + \frac{V_2}{r_{01}} \tag{1}$$

also

$$i_{in} = \frac{V_2}{r_{01}} + \left(g_{m1} + \frac{1}{R_1}\right)V_1 + \frac{V_8}{R_5} \tag{2}$$

At node 8

$$\frac{V_8}{R_5} = g_{m8}V_2 + \frac{V_2 - V_8}{r_{08}} \tag{3}$$

Simplifying (3)

$$\frac{V_8}{R_5} = \frac{g_{m8}r_{08}}{r_{08} + R_5}V_2 \tag{4}$$

At node 1

$$\frac{V_1}{R_1} = -g_{m3}V_{72} - \frac{V_1 - V_2}{r_{03}} \tag{5}$$

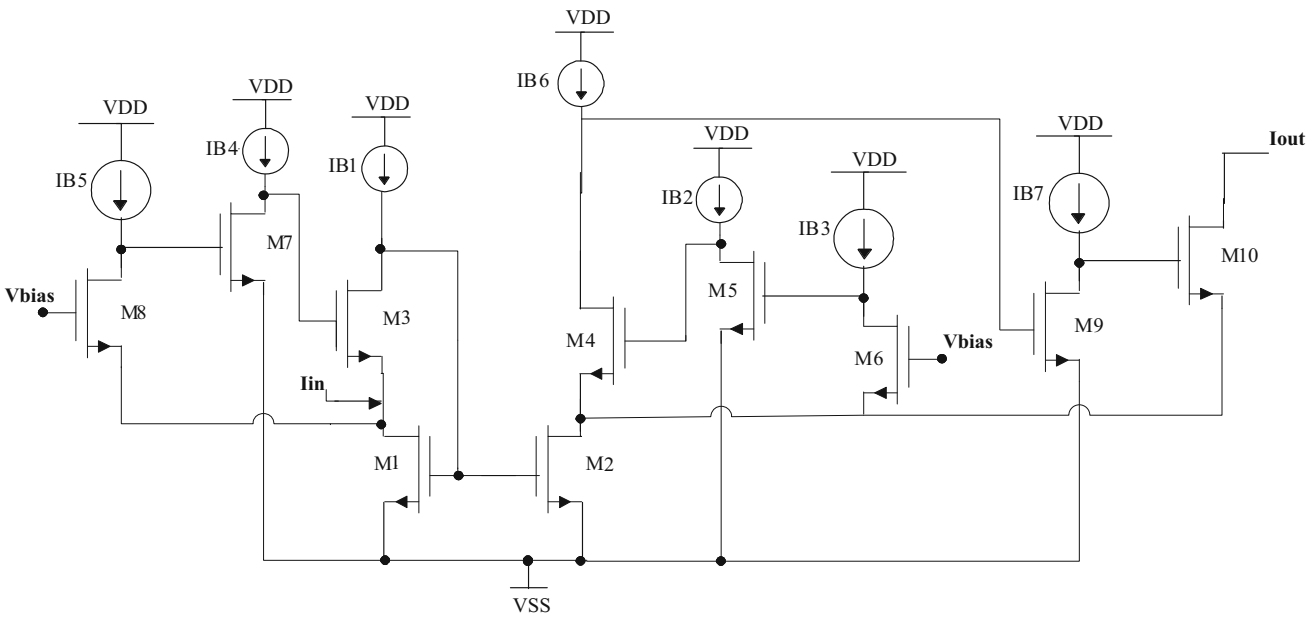

Figure 3. Proposed FVF current mirror.

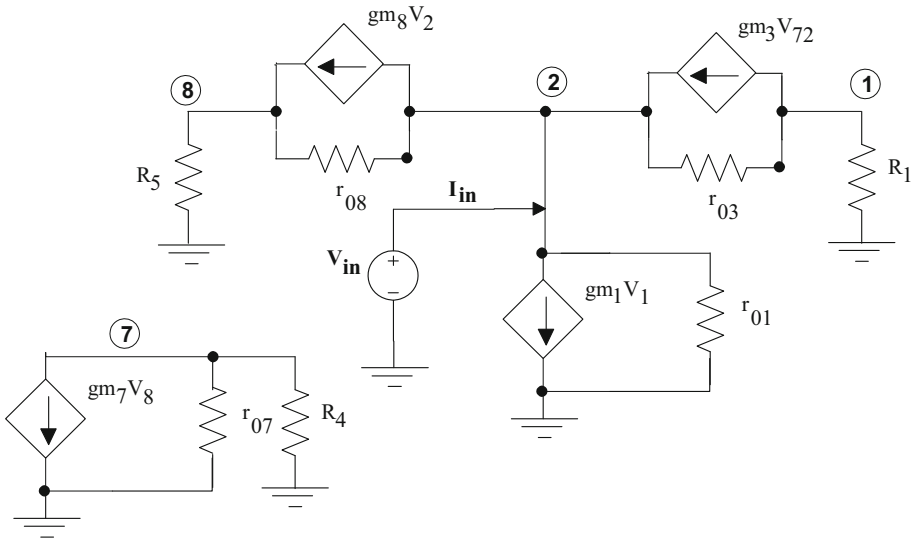

Figure 4. Small signal model for calculating input resistance.

Simplifying (5)

$$V_1 = g_{m3}(R_1//r_{03})(V_2 - V_7) \tag{6}$$

At node 7

$$\frac{V_7}{R_4} + g_{m7}V_8 + \frac{V_7}{r_{07}} = 0 \tag{7}$$

Simplifying (7)

$$V_7 = -g_{m7}(R_4//r_{07})V_8 \tag{8}$$

From (6) & (8)

$$V_1 = g_{m3}(R_1//r_{03})(V_2 + g_{m7}(R_4//r_{07})V_8) \tag{9}$$

Simplifying (9)

$$V_1 = g_{m3}g_{m7}g_{m8}(R_1//r_{03})(R_4//r_{07})(R_5//r_{08})V_2 \tag{10}$$

From (2) & (10)

$$i_{in} = \frac{V_2}{r_{01}} + \left(g_{m1} + \frac{1}{R_1}\right)V_1 + \frac{g_{m8}r_{08}}{r_{08} + R_5}V_2 \tag{11}$$

Since $g_m r_0 > > 1$

$$i_{in} \approx g_{m1}g_{m3}g_{m7}g_{m8}(R_1//r_{03})(R_4//r_{07})(R_5//r_{08})V_2 \tag{12}$$

Simplifying (12)

$$R_{in} = \frac{V_2}{i_{in}} \approx \frac{1}{g_{m1}g_{m3}g_{m7}g_{m8}(R_1//r_{03})(R_4//r_{07})(R_5//r_{08})} \tag{13}$$

For an ideal current source, $R_1 = R_4 = R_5 = \infty$

$$R_{in,prop.} \approx \frac{1}{g_{m1}(g_{m3}r_{03})(g_{m7}r_{07})(g_{m8}r_{08})} \tag{14}$$

From (14), it can be observed that a decrement in the input resistance by $(g_{mi}r_{0i})^2$ times compared to conventional FVF current mirror is achieved using super transistor configuration.

3.1b *Output resistance*: The small signal model for calculating the output resistance ($R_{out,prop.}$) of the proposed current mirror is shown in figure 5.

At node 10

$$i_{out} = g_{m10}V_{93} + \frac{V_{10} - V_3}{r_{10}} \tag{15}$$

At node 3

$$V_3 = \left(i_{out} + g_{m4}V_{53} + \frac{V_4 - V_3}{r_{04}} - g_{m6}V_3 + \frac{V_6 - V_3}{r_{06}}\right)r_{02} \tag{16}$$

At node 4

$$g_{m4}V_{53} + \frac{V_4 - V_3}{r_{04}} + \frac{V_4}{R_6} = 0 \tag{17}$$

Simplifying (17)

$$g_{m4}V_5 - g_{m4}V_3 - \frac{V_3}{r_{04}} + \frac{V_4}{r_{04}//R_6} = 0 \tag{18}$$

Since $g_m r_0 > > 1$

$$g_{m4}V_5 - g_{m4}V_3 + \frac{V_4}{r_{04}//R_6} = 0 \tag{19}$$

Simplifying (19)

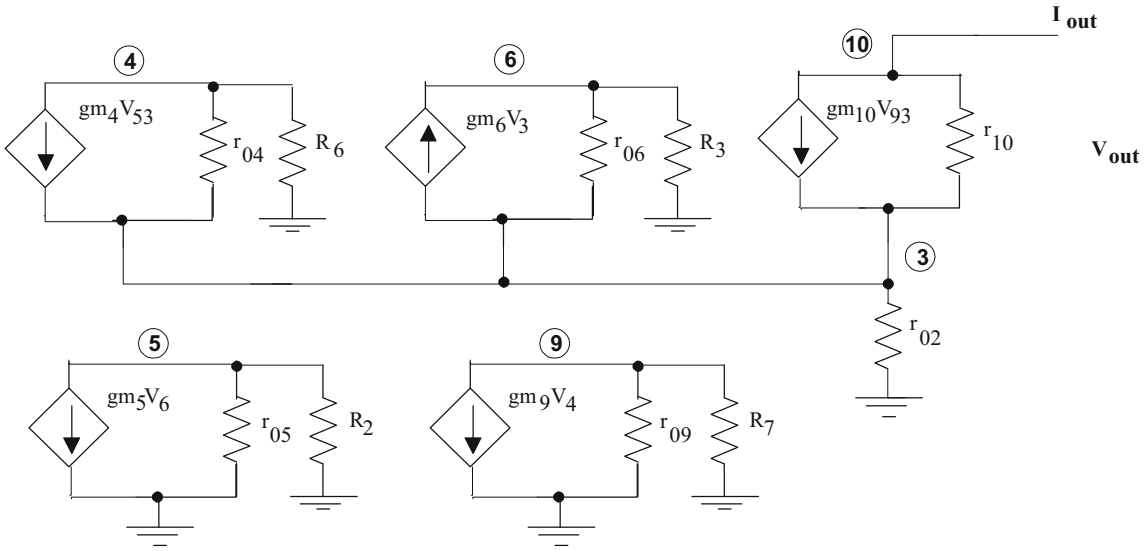

Figure 5. Small signal model for calculating output resistance.

$$V_4 = -g_{m4}(r_{04}//R_6)V_{53} \tag{20}$$

Similarly, at node 6

$$-g_{m6}V_3 + \frac{V_6 - V_3}{r_{06}} + \frac{V_6}{R_3} = 0 \tag{21}$$

Solving (21)

$$V_6 = g_{m6}(r_{06}//R_3)V_3 \tag{22}$$

At node 5

$$g_{m5}V_6 + \frac{V_5}{r_{05}} + \frac{V_5}{R_2} = 0 \tag{23}$$

Simplifying (23)

$$V_5 = -g_{m5}(r_{05}//R_2)V_6 \tag{24}$$

From (22) & (24)

$$V_{53} = -g_{m5}g_{m6}(r_{05}//R_2)(r_{06}//R_3)V_3 \tag{25}$$

From (20) & (25)

$$V_4 = g_{m4}g_{m5}g_{m6}(r_{04}//R_6)(r_{05}//R_2)(r_{06}//R_3)V_3 \tag{26}$$

At node 9

$$g_{m9}V_4 + \frac{V_9}{r_{09}} + \frac{V_9}{R_7} = 0 \tag{27}$$

Simplifying (27)

$$V_9 = -g_{m9}(r_{09}//R_7)V_4 \tag{28}$$

From (26) & (28)

$$V_9 = -g_{m4}g_{m5}g_{m6}g_{m9}(r_{04}//R_6)(r_{05}//R_2)(r_{06}//R_3)(r_{09}//R_7)V_3 \tag{29}$$

Since $g_m r_0 > > 1$

$$V_{93} = -g_{m4}g_{m5}g_{m6}g_{m9}(r_{04}//R_6)(r_{05}//R_2)(r_{06}//R_3)(r_{09}//R_7)V_3 \tag{30}$$

From (15), (16), (22), (25), (26) & (30)

$$i_{out} = -g_{m4}g_{m5}g_{m6}g_{m9}g_{m10}(r_{04}//R_6)(r_{05}//R_2)(r_{06}//R_3)(r_{09}//R_7)i_{out}r_{02} + \frac{V_{10} - i_{out}r_{02}}{r_{10}} \tag{31}$$

Since $g_m r_0 > > 1$

$$g_{m4}g_{m5}g_{m6}g_{m9}g_{m10}(r_{04}//R_6)(r_{05}//R_2)(r_{06}//R_3)(r_{09}//R_7)r_{02}i_{out} = \frac{V_{10}}{r_{10}} \tag{32}$$

Simplifying (32)

$$R_{out} = \frac{V_{10}}{i_{out}} \approx g_{m4}g_{m5}g_{m6}g_{m9}g_{m10}(r_{04}//R_6)(r_{05}//R_2)(r_{06}//R_3)(r_{09}//R_7)r_{10}r_{02} \tag{33}$$

For an ideal current source, $R_2 = R_3 = R_6 = R_7 = \infty$

$$R_{out.prop.} \approx (g_{m4}r_{04})(g_{m5}r_{05})(g_{m6}r_{06})(g_{m9}r_{09})(g_{m10}r_{10})r_{02} \tag{34}$$

From (34), due to super transistor an increment in the output resistance by $(g_{mi}r_{0i})^2$ times compared to conventional FVF current mirror can be seen possible through

super transistor which further gets enhanced by $(g_{mi}r_{0i})^2$ through super cascode.

3.1c *Frequency response*: The frequency response is a function of its gain and feedback capacitance. The small-signal model for calculating current gain of the proposed current mirror is shown in figure 6. Here, the output conductance is neglected. Also the C_{gd} effects are neglected in comparison to C_{gs} of saturation mode transistors.

At node 2

$$i_{in} - g_{m3}V_2 = g_{m1}V_1 + sC_{gs3}V_2 \tag{35}$$

At node 1

$$-g_{m3}V_2 + s\left(C_{gs1} + C_{gs2}\right)V_1 = 0 \tag{36}$$

From (35) & (36)

$$i_{in} = \left(g_{m3} + sC_{gs3}\right)\frac{s\left(C_{gs1} + C_{gs2}\right)}{g_{m3}}V_1 + g_{m1}V_1 \tag{37}$$

Simplifying (37)

$$i_{in} = \frac{C_{gs3}\left(C_{gs1} + C_{gs2}\right)}{g_{m3}}\left(s^2 + \frac{g_{m3}}{C_{gs3}}s + \frac{g_{m1}g_{m3}}{C_{gs3}\left(C_{gs1} + C_{gs2}\right)}\right)V_1 \tag{38}$$

At node 4

$$i_{out} = g_{m4}V_{53} \tag{39}$$

At node 3

$$g_{m4}V_{53} = sC_{gs4}V_{35} + g_{m6}V_3 + sC_{gs6}V_3 + g_{m2}V_1 \tag{40}$$

Simplifying (40)

$$\left(g_{m4} + sC_{gs4}\right)V_{53} = \left(g_{m6} + sC_{gs6}\right)V_3 + g_{m2}V_1 \tag{41}$$

At node 6

$$g_{m6}V_3 = sC_{gs5}V_6 \tag{42}$$

Simplifying (42)

$$V_3 = \frac{sC_{gs5}}{g_{m6}}V_6 \tag{43}$$

At node 5

$$g_{m5}V_6 = sC_{gs4}V_{35} \tag{44}$$

Simplifying (44)

$$V_6 = \frac{sC_{gs4}}{g_{m5}}V_{35} \tag{45}$$

From (41), (43) & (45)

$$\left(g_{m4} + sC_{gs4}\right)V_{53} = \left(g_{m6} + sC_{gs6}\right)\left(\frac{sC_{gs5}}{g_{m6}}\right)\left(\frac{sC_{gs4}}{g_{m5}}\right)V_{35} + g_{m2}V_1 \tag{46}$$

Simplifying (46)

$$V_{53} = \frac{g_{m2}g_{m5}g_{m6}}{C_{gs4}C_{gs5}C_{gs6}\left(\frac{g_{m4}g_{m5}g_{m6}}{C_{gs4}C_{gs5}C_{gs6}} + s\frac{g_{m5}g_{m6}}{C_{gs5}C_{gs6}} + s^2\frac{g_{m6}}{C_{gs6}} + s^3\right)}V_1 \tag{47}$$

From (39) & (47)

$$i_{out} = \frac{g_{m2}g_{m4}g_{m5}g_{m6}}{C_{gs4}C_{gs5}C_{gs6}\left(s^3 + \frac{g_{m6}}{C_{gs6}}s^2 + \frac{g_{m5}g_{m6}}{C_{gs5}C_{gs6}}s + \frac{g_{m4}g_{m5}g_{m6}}{C_{gs4}C_{gs5}C_{gs6}}\right)}V_1 \tag{48}$$

From (38) & (48)

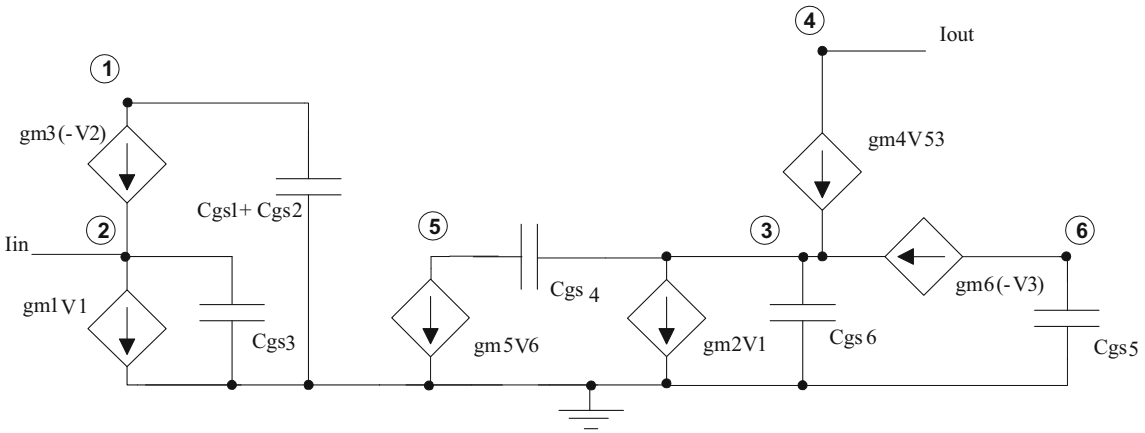

Figure 6. Small signal model for calculating current gain.

$$A_I = \frac{i_{out}}{i_{in}} = \frac{g_{m2}g_{m4}g_{m5}g_{m6}g_{m3}}{C_{gs4}C_{gs5}C_{gs6}C_{gs3}\left(C_{gs1}+C_{gs2}\right)\left(s^3+\frac{g_{m6}}{C_{gs6}}s^2+\frac{g_{m5}g_{m6}}{C_{gs5}C_{gs6}}s+\frac{g_{m4}g_{m5}g_{m6}}{C_{gs4}C_{gs5}C_{gs6}}\right)\left(s^2+\frac{g_{m3}}{C_{gs3}}s+\frac{g_{m1}g_{m3}}{C_{gs3}\left(C_{gs1}+C_{gs2}\right)}\right)} \tag{49}$$

Simplifying (49)

$$A_I = \frac{g_{m2}g_{m3}g_{m4}g_{m5}g_{m6}/\left(C_{gs1}+C_{gs2}\right)C_{gs3}C_{gs4}C_{gs5}C_{gs6}}{\left(s^3+\frac{g_{m6}}{C_{gs6}}s^2+\frac{g_{m5}g_{m6}}{C_{gs5}C_{gs6}}s+\frac{g_{m4}g_{m5}g_{m6}}{C_{gs4}C_{gs5}C_{gs6}}\right)\left(s^2+\frac{g_{m3}}{C_{gs3}}s+\frac{g_{m1}g_{m3}}{C_{gs3}\left(C_{gs1}+C_{gs2}\right)}\right)} \tag{50}$$

Table 1. W and L of MOS transistors used in the proposed current mirror.

Transistors	W (um)	L (um)	Transistors	W (um)	L (um)
M1	25	0.24	M6	5	0.24
M2	25	0.24	M7	0.24	0.24
M3	5	0.24	M8	5	0.24
M4	5	0.24	M9	2	0.24
M5	0.24	0.24	M10	5	0.24

Supply=± 0.5V, Vbias=0.5V, IB1=IB6=IB7=10uA, IB2-IB5=20uA

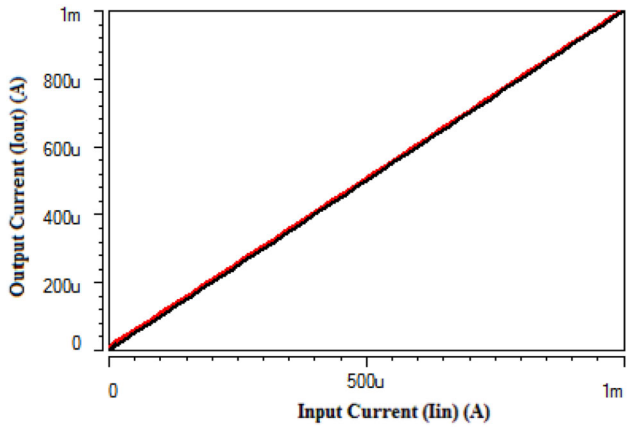

Figure 7. Current transfer characteristic of the proposed current mirror for input current ranging from 0 to 1 mA.

The equation (50) is the current gain (transfer function) of the proposed current mirror circuit. The proposed current mirror is inherently stable since $\frac{g_{m6}}{C_{gs6}} > \frac{g_{m4}}{C_{gs4}}$.

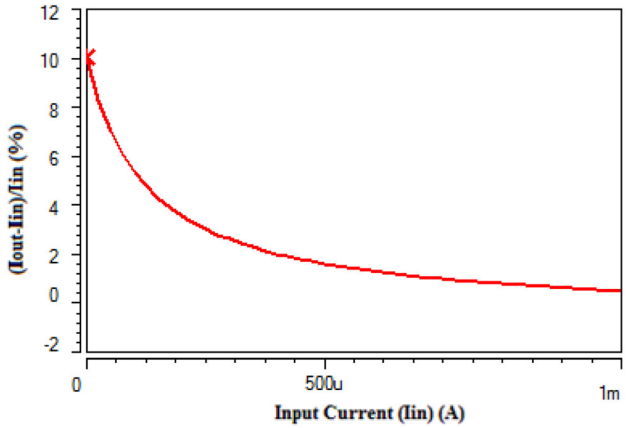

Figure 8. Error in current transfer characteristic of the proposed current mirror.

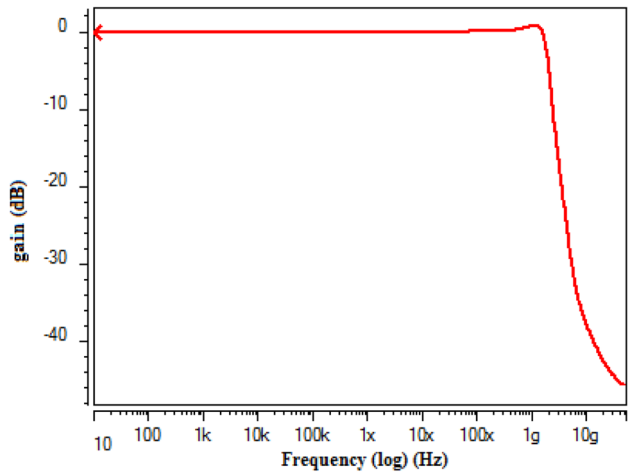

Figure 9. Frequency response for bandwidth calculation of the proposed current mirror.

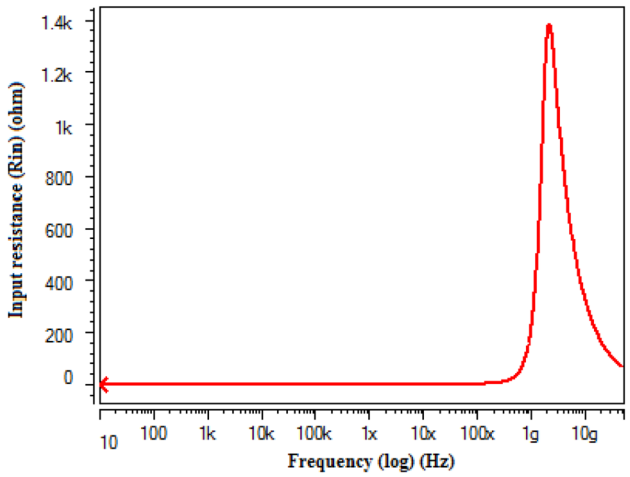

Figure 10. Input resistance of the proposed current mirror.

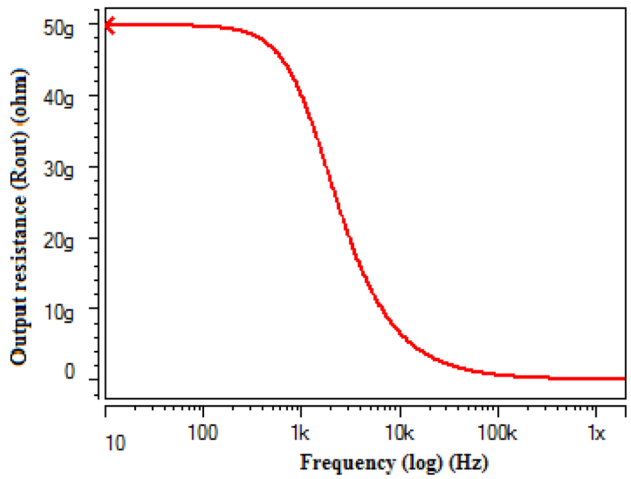

Figure 11. Output resistance of the proposed current mirror.

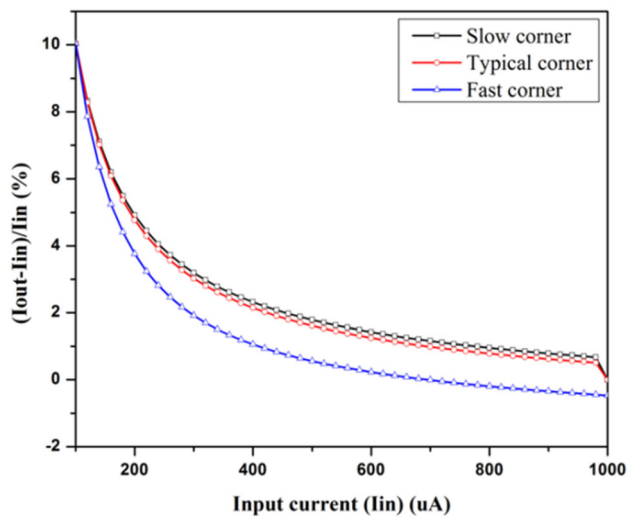

Figure 12. Process corner analysis of current transfer error ratio.

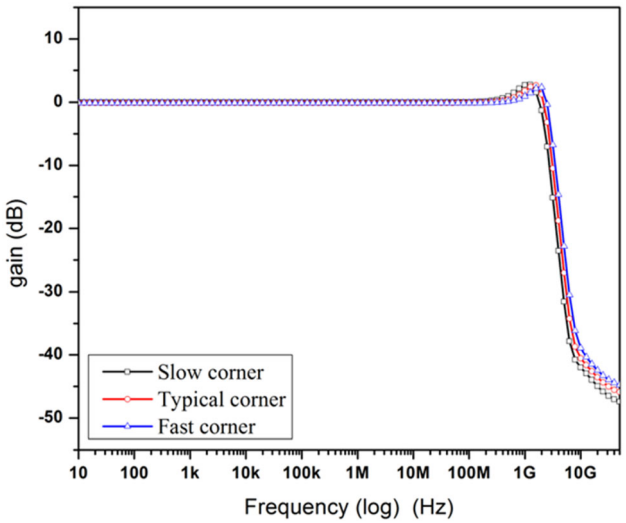

Figure 13. Process corner analysis of frequency response.

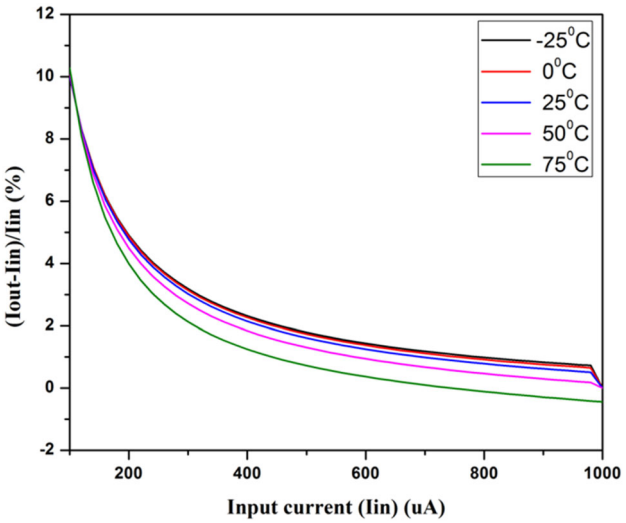

Figure 14. Temperature analysis of current transfer error ratio.

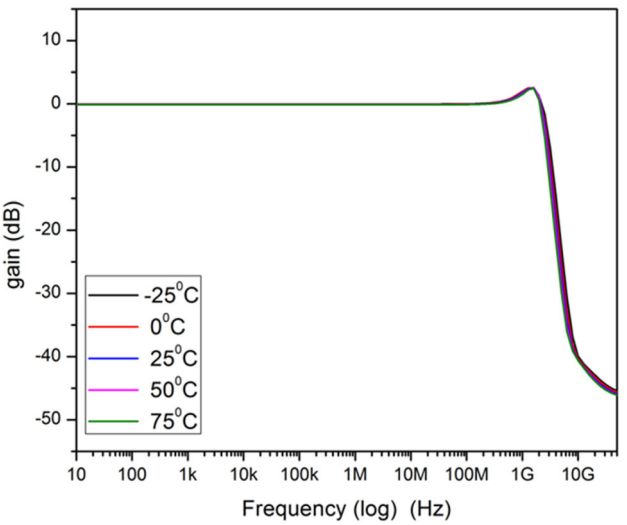

Figure 15. Temperature analysis of frequency response.

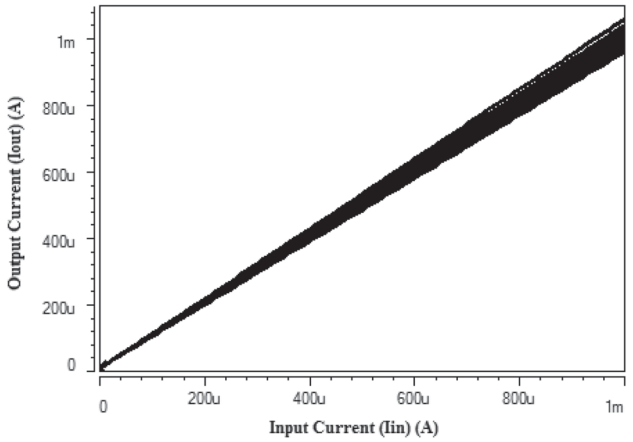

Figure 16. Monte Carlo (100 runs) of current transfer characteristic.

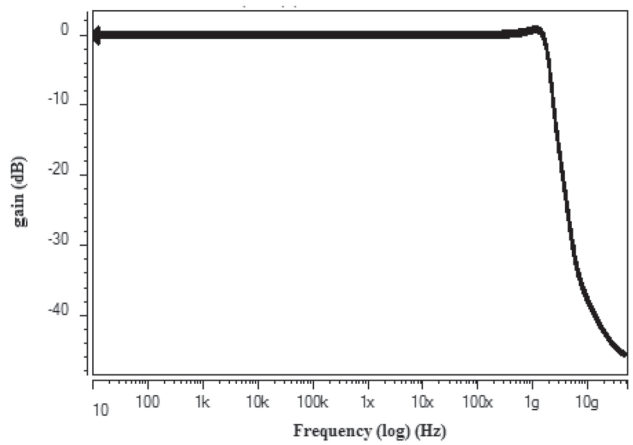

Figure 17. Monte Carlo (100 runs) of frequency response.

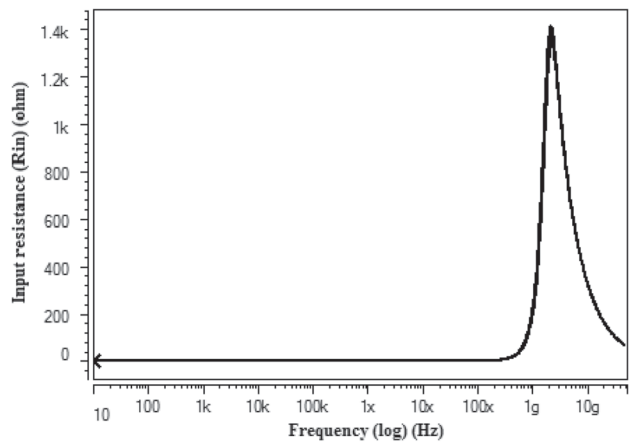

Figure 18. Monte Carlo (100 runs) of input resistance.

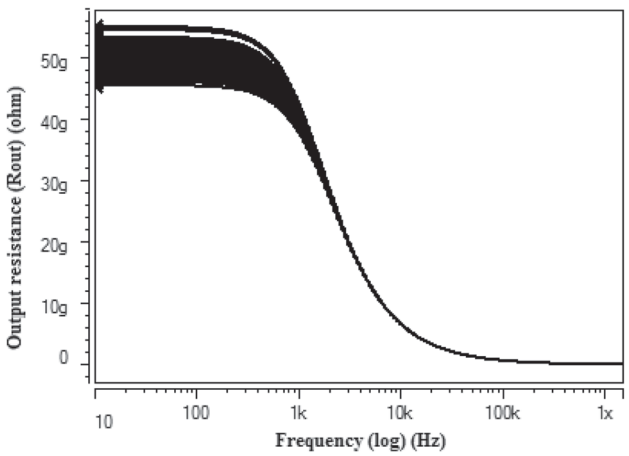

Figure 19. Monte Carlo (100 runs) of output resistance.

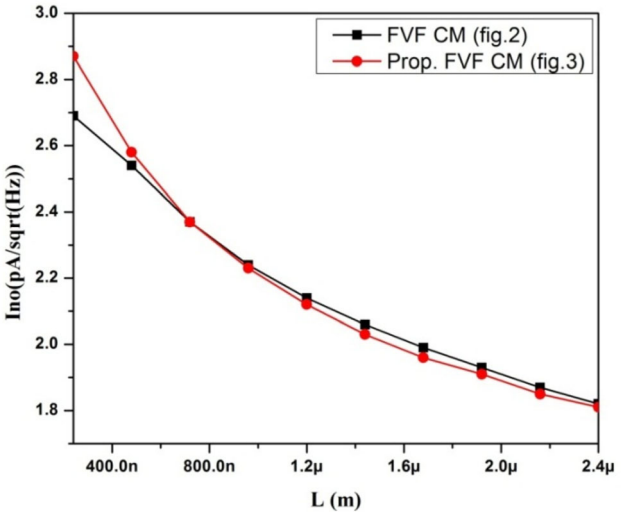

Figure 20. Noise versus L.

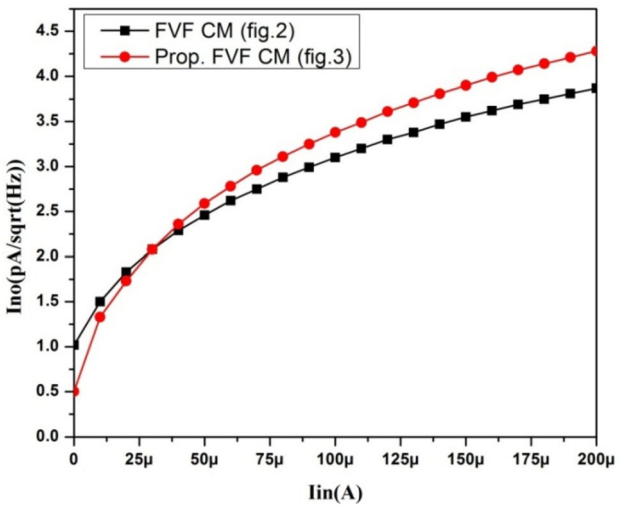

Figure 21. Noise versus input current.

Table 2. Comparison of parameters of the proposed current mirror with FVF current mirrors.

Parameters	[22]	[23]	[24]	[25]	[26]	[27]	[28]	This work
Input current range (uA)	–	300	300	0-440	0-100	1000	0-200	0-1000
Input compliance voltage (V)	145m	58m	58m	52m	39.6m	–	–	0.3m
Current transfer error (%)	–	0.02	0.28	1.71	0.6	0.16	0.22	0.38
Input resistance (ohm)	–	13.3	12.8	21.43	496	68.3	130	0.407
Output resistance (ohm)	200M	34.3G	39.5G	1.14G	1M	10.5G	9.5G	50G
Bandwidth (Hz)	40M	210M	216M	6.17G	181M	402M	2.7G	2.1GHz
Noise ($pA/\sqrt{Hz}$)	6.9	–	4.97	–	–	7.8	–	3.1
Supply (V)	1.2	1	1	1	0.9	1	0.8	$\pm$ 0.5
Power (uW)	–	42.5	42.5	916.65	154	110	79.33	156
Technology (um)	CMOS 2	TSMC 0.18	TSMC 0.18	TSMC 0.18	0.18	0.18	0.18	0.18

4. Simulation results

The proposed current mirror circuit shown in figure 3 is simulated in 0.18 um technology at $\pm$ 0.5 V supply with the help of HSpice simulator. The device dimension of transistors and other assumed parameters for circuit simulations are listed in table 1. The selection of input bias currents is to ensure lower V_{in} and offset in the circuit. The channel length of the transistors is kept at its minimum value.

The current transfer characteristic of the proposed current mirror ranging from 0 to 1 mA is shown in figure 7 and the corresponding current copying error as percentage is shown in figure 8.

The error is minimum at high input current, i.e., the curve varies from 10% for low input current and further decreases to less than 1% when input current reaches to milli ampere range. The frequency response, input resistance and output resistance plots are shown in figures 9 to 11, respectively. The proposed current mirror's bandwidth is found as 2 GHz as shown in figure 9. As expected from the small-signal analysis, the input and output resistances are very low and extremely high value respectively. The input resistance is found to be below one ohm, i.e., 0.407 ohm (shown in figure 10) whereas the output resistance is 50 giga ohm (shown in figure 11).

The robustness of proposed current mirror circuit against environmental variations is shown with the help of process corner analysis and temperature variation. The circuit is simulated on three different process corners, namely Slow, Typical and Fast. The variation in output current to input current at these process corners as a percentage in current transfer error ratio is shown in figure 12 and also its impact on bandwidth is shown in figure 13.

For temperature analysis, the proposed current mirror is simulated for temperatures ranging from -25^{0}C to 75^{0}C at the steps of 25^{0}C. The percentage error in current transfer at these temperatures is shown in figure 14 whereas the effect of varying temperature on frequency response is shown in figure 15. It can be observed that the proposed current mirror operates within acceptable range in whole design space. Further the Monte Carlo runs against channel length variation is performed by applying 5% mismatch in the channel length with the help of Gaussian distribution. The Monte Carlo (100 runs) has been performed on DC and AC responses of proposed current mirror shown in figures 16 to 19 where it can be observed that the manufacturing process does not have significant degeneration in the mentioned specifications. So, the structure of the proposed FVF current mirror has a good stability under the mismatch analysis.

Current mirrors being commonly used in high frequency analog circuits, its low noise operation is one of the important parameter. During noise analysis for the conventional and proposed FVF current mirror, the input and output noise levels are normalized with respect to square root of the noise bandwidth.

The total output noise as a function of varying channel length is shown in figure 20 and also the impact of input current in noise is shown in figure 21. As seen noise performance of proposed circuit is comparable to that of conventional FVF current mirror.

The complete simulated HSpice results of the proposed current mirror are shown in table 2 and also compared with recently reported low power, FVF current mirrors.

5. Conclusion

A low voltage high performance efficient current mirror design in terms of input and output resistances has been presented and verified through HSpice 0.18 um simulation results. The current mirroring transistors were configured as flipped voltage follower structure which made it to operate with better accuracy at dual supply of 0.5 volt. For parameter improvement in terms of input and output resistances, the super transistor stage was used both at the input and output section. Moreover, for further boosting of output impedance in giga ohm range the super cascode configuration was used. Simulations showed improvement compared to other previously reported works. The low voltage low power current mirror having wide bandwidth with enhanced input output resistance favors its application

as a building block in low-voltage high-speed mixed-mode VLSI systems.

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