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Compact modeling of through silicon vias for thermal analysis in 3-D IC structures

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Abstract. Heat mitigation is a major challenge in 3-D IC (Three-Dimensional Integrated Circuit) realization. A study of analytical thermal behavior of the TSV (Through Silicon Via) is very important. Simple and compact yet other models were found deficient to solve this problem in the literature survey. In this paper, resistance networks are used to model the heat transfer of the TSVs in both vertical and horizontal directions in simpler and compact models. The accuracy of such models is compared to those from the commercially available CFD (computational fluid dynamics) tool. The errors of corrections between the tool and developed models are corrected by multiplication factors, resulting in 4.18% accuracy. Varying the thicknesses of a liner, filler, soldering, and substrate materials is studied concerning heat transfer and physical behavior of three planar TSV stacked systems. The major purpose is to incorporate both vertical and horizontal thermal resistance networks captured more accurately in heat dissipation paths. Proposed models of TSVs can be used in the active interposer simulations or the face-to-face fabrication stacked methods of the 3-D IC structures.

Keywords. Thermal conductivity; interposer; fitting coefficient; thermal resistance.

1. Introduction

Through Silicon Vias (TSVs) are the pillars of the Three-Dimensional Integrated Circuit (3-D IC) structures. They are used in active and passive interposers. The reason for getting heated is high current sustained inside the TSV; hence more parasitic effects are observed; thus thermal energy is generated. TSVs interconnects are manufactured using dual damascene procedures, usually with copper, as explained in [1, 2]. TSVs, when grouped in arrays, exhibit more electromagnetic and mutual thermal coupling through the silicon substrate, resulting in the degradation of the slew of the signals/clocks. Hence, more power consumption can occur as studied in [3]. Thermal Through Silicon Vias (TTSVs) are introduced to reduce the temperatures, as one approach to solve thermal challenges [4]. For this, the thermal generations inside the signal TSVs should be well studied. Such observations conclude that thermal convection of the 3-D ICs is not scaled by stacking [5–11]. Demonstrated via effects must be considered to evaluate accurately the thermal capability of 3-D ICs. Thermal simulations for the TSVs should be done in the multi-planar environment than simulating in single planar along with intermediate structures taken into consideration, because of the following advantages: eliminating initialization of thermal boundary conditions for every die/plane, with a lesser number of iterations, resulting in more accuracy [12, 13].

Physically, heat traverses in all directions from the point of heat source. The novel method of considering the TSV in one-dimensional space is found to be insufficient to model heat transfer of the objects involved [14–16]. Hotspot models have been shown to be efficient for design stages and thermal analysis. Jason and Zhang [17] formulate the TTSV via minimization problem with temperature constraints as a constrained nonlinear programming problem based on the thermal resistive models. Haihua Su *et al* [18] perform a full-chip leakage power estimation considering the power supply, and temperature variations can guide sources of the power losses. Ankur Jain *et al* [19] model the heat and aid in the development of thermal design guidelines for 3-D ICs. Brent Goplen and Sapatnekar [20] have come up with an efficient thermal-via-placement method. Resulting thermal-via placements have lowered the

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temperatures and thermal gradients with minimal use of thermal vias. Lau and Yue [21] concluded that distinguished pairs of staggered heat sources on the 3-D TSV chips lead to better thermal performance than the pair of overlapped heat sources. Ayala *et al* [22] proposed an effective mechanism to optimize the thermal profile of 3-D integrated systems with the use of a nano-grid of TSVs. Accurate modeling of the thermal effect has been developed in a 5-tier 3-D IC stack. Later, they proposed the capability of a nanostructure of TTSVs to improve the thermal response of the 3-D systems.

Madhavan Swaminathan [23] from Georgia University discusses the novel electrical design challenges for 3-D integrations, which helps in addressing the thermal issue as one of the major challenges. The electrical modeling of interposer is not trivial, due to lossy and semiconducting behavior and temperature effect. Electrothermal modeling of TSV interconnects, using the Partial Element Equivalent Circuit (PEEC) method, was discussed by Xiao-Peng Wang *et al* [24].

Therefore the research gap related to the present investigation is lack of simple models, lateral conduction given less importance, and heat losses ignored in the 3-D stacks, where the TSVs join from one plane to another. The present paper considers heat transmission in all the directions, by representing in lateral and vertical directions to capture this physical phenomenon in simple and compact models. The developed models consider the physical structures of the components and material parameters to match in the industry. The mesh-based simulation is done by the Autodesk's 2017 versioned CFD tool [25], through which FEM (Finite-Element Method) analysis is compared to check the accuracy of the developed models. CFD modeling considers the thermal flow distribution on the structures. The material property, mesh grids, and physical structures are major parameters involved in the simulations.

Following section 2 has a brief explanation of the single-plane thermal models in comparison with multimode multi-planar models. Section 3 discusses the thermal performance of TSV parameters with various results observed using computations and CFD tool readings. Relevant conclusions and summary are drawn in section 4.

2. Compact modeling of TSV

Employing the control system theory, the basic analogy of a physical thermal system can be represented with an equivalent electrical resistance model. The resistance is considered as positive resistance, as per the present realization of sub-micron technology behaviors inside the TSVs, implying that thermal resistance increases to oppose the rate of current. A heat source is analogous to the current source. Min Ni *et al* [26] analyze the use of TTSV in reducing the temperatures, in a multi-tier multi-die 3-D system. Electrical voltages are analogous to temperature gradients in the circuit. Electrical resistance is analogous to thermal resistance. Current sources are analogous to thermal sources. Thus, the heat transfer phenomenon can be as simplified as shown in figure 1. Total heat generated from the heat sources is represented by the current source I_s. Total heat dissipated from the circuit is represented by drain current I_d. Thus, a voltage-controlled current source in the circuit is the current source I_d. The ambient temperature is represented by circuit ground. The maximum temperature in a 3-D IC stack is near the heat sources represented by V_a. The minimum temperature is located near the dissipation surfaces of the heat sink, represented by V_b. Hence, the following equations (A) and (B) for the circuit shown in figure 1 are obtained:

$$I_s = \frac{T_a - T_b}{R_{ab}} + \frac{T_a}{R_a}, \tag{A}$$

$$I_d = \frac{T_a - T_b}{R_{ab}} - \frac{T_b}{R_b}. \tag{B}$$

In this system, a decrease in R_{ab} causes a decrease in V_a and an increase in V_b. This implies that TTSVs anyway decrease the maximum heat and increase the minimum heat in a 3-D stack system. Similarly, Kirchhoff's law is applied for the entire three-tier stacking of TSV as shown in figure 2a. This shows the entire assembly of the 3-D planar structure with single TSV, considered in the experimental setup. The group of the TSVs is also studied in the later part under the same 3-D planar structure. The materials and the structure remain the same even in case of different technologies and dimensions in the various foundries. Hence, in this structure, Si_1, Si_2, Si_3 are three dies, along with ILD layers (Inter-Layer Dielectric) interconnected with soldering material, surrounded by a bonding material. Each *Si* layer has the BEOL (Back End Of Line) metallization composed internally, as ILD (shown with violet color in figure 2b), via TSV, where there are actual heat sources inside each of the dies (q_1, q_2, and q_3). Different thermal resistances R_1–R_9 are associated with the structure. T_0–T_7 are different temperature nodes, as shown in figure 2a. R_s is the heat sink resistance. On applying Kirchhoff's Current Law (KCL), on this structure, equations can be obtained.

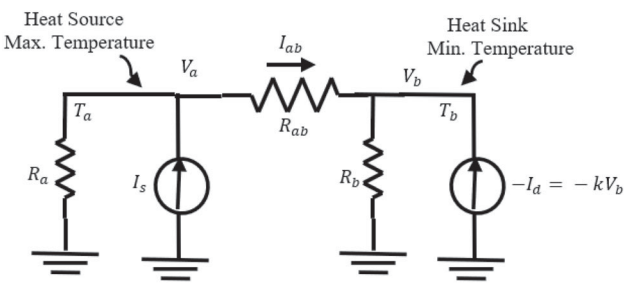

Figure 1. Electrical modeling of TSV thermal parameters.

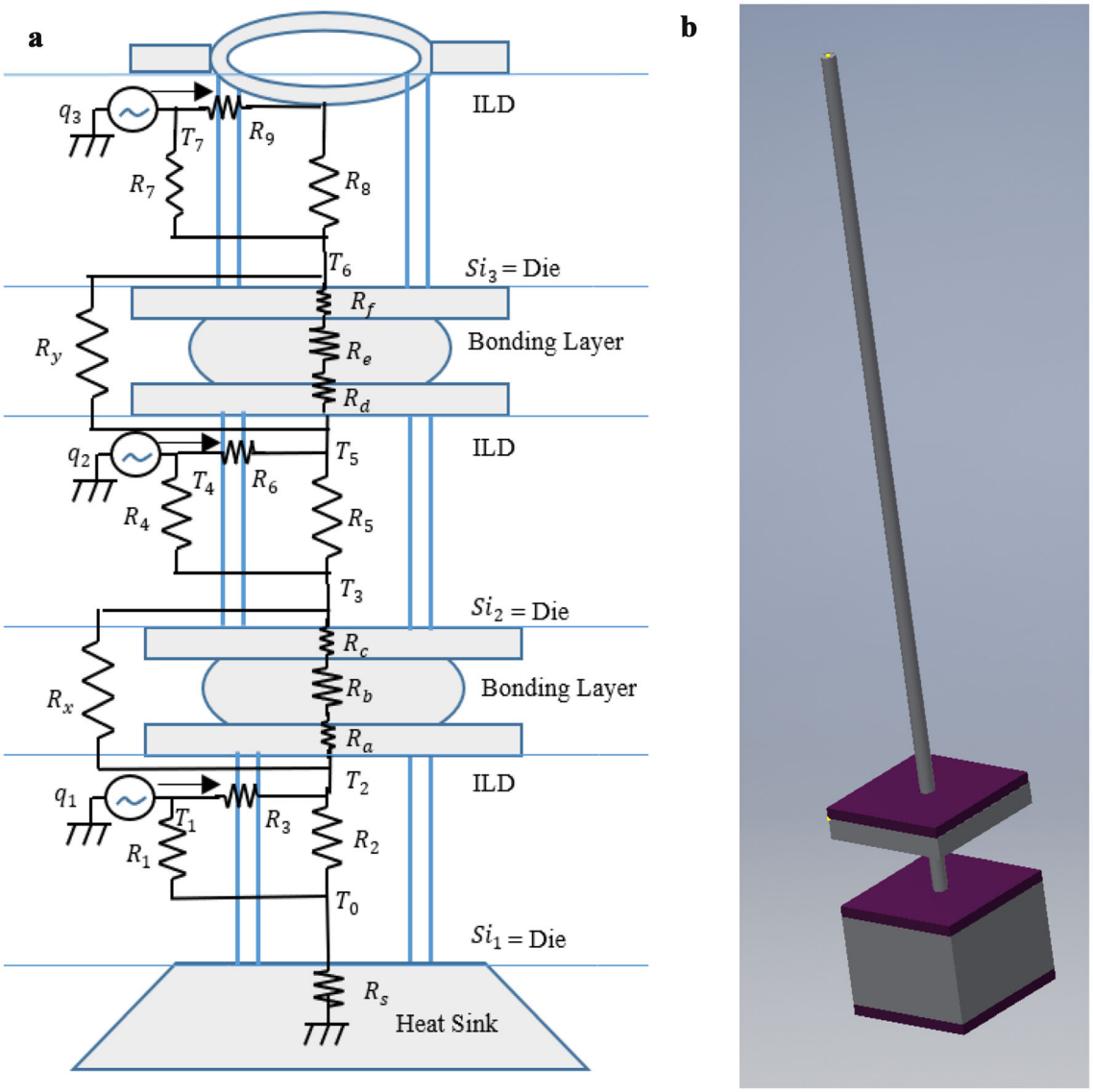

Figure 2. (**a**) Three-tier/planar structure of stacked TSV with analogous electrical resistances. (**b**) Si_2, Si_3, ILD parts of three-tier/planar structure of stacked TSV, structure used in CFD simulations.

These thermal resistances are based on the physical shape and dimensions of TSVs. Footprint of the experimental step is represented by A_0 area; tSi, t_D, and t_b are thickness of the silicon substrate, ILD layer, and bonding layer, respectively; k_{si}, k_s, k_D, k_b, k_L, and k_f are the thermal conductivities of the substrate, soldering, ILD, bonding, liner, and filler materials of TSV, respectively; r and t_L are the radii of TSV and thickness of insulator liner, respectively [27]. In the experimental setup of figure 2a the whole TSV structure does not run through like TTSV inside the 3-D IC stacks, that is entering through the bonding material and substrates; x_1 and x_2 are fitting coefficients used to optimize the thermal resistance models to match software simulations to decrease

$$q_3 = \frac{T_7 - T_6}{R_9 + R_8} + \frac{T_7 - T_6}{R_7} \tag{1}$$

$$\frac{T_7 - T_6}{R_7} + \frac{T_7 - T_6}{R_8 + R_9} = \frac{T_6 - T_5}{R_y} + \frac{T_6 - T_5}{R_f + R_e + R_d} \tag{2}$$

$$\frac{T_6 - T_5}{R_y} + \frac{T_6 - T_5}{(R_f + R_c + R_d)} = \frac{T_5 - T_4}{R_6} + \frac{T_5 - T_3}{R_5} \tag{3}$$

$$q_2 = \frac{T_4 - T_5}{R_6} + \frac{T_4 - T_3}{R_4} \tag{4}$$

$$\frac{T_5 - T_3}{R_5} + \frac{T_4 - T_3}{R_6} = \frac{T_3 - T_2}{R_x} + \frac{T_3 - T_2}{R_a + R_b + R_c} \tag{5}$$

$$\frac{T_3 - T_2}{R_x} + \frac{T_3 - T_2}{(R_a + R_b + R_c)} = \frac{T_2 - T_1}{R_3} + \frac{T_2 - T_0}{R_2} \tag{6}$$

$$q_1 = \frac{T_1 - T_2}{R_3} + \frac{T_1 - T_0}{R_1} \tag{7}$$

$$T_0 = R_s(q_1 + q_2 + q_3) \tag{8}$$

the discrepancy of models from CFD simulations. They can be practically determined only by the CFD simulations because simulations consider material property, material mesh structure, and lattice structures including the physical dimensions. Therefore, x_1. and x_2. could be used to compromise due to afore-mentioned reasons. Because of this reason the horizontal thermal transfer is more complex as described through R_3, R_6, R_9, R_x, and R_y; 'l_{ext}' is the segment if TSV extends into the silicon substrate in the first plane. Solving (1)–(8), by the substation of (11)–(25), results in different nodal temperatures (T_0–T_7) in three planar 3-D IC stacks using matrices method, as in (9):

$$X \times Y = Z \tag{9}$$

where X matrix represents the values in the equation of temperature nodes from T_0 to T_7. Y matrix represents the unknown temperature nodes, and Z matrix represents the sources of thermal energies.

These models can be used to solve any 'N' number of planes. For N-plane 3-D IC structures, R_1–R_3 are the resistances of TSVs in the first plane. R_4–R_6 are the resistance of TSVs in the second plane. R_7–R_9 represent TSV in the third plane, and it can be repeated for a larger scale. R_2, R_5, and R_6 are the resistance of filler material. R_3, R_6, and R_9. are the resistance of liner material. R_a, R_c, R_d, and R_f are the resistances of pads of the TSVs, as in figure 3a. R_b and R_e are resistances of soldering material. They are short cylindrical micro-bump structures, made up of soldering material as shown in figure 3b. The volume of the pad (15) and the soldering bumps (16) are required to subtract in calculating R_x and R_y resistors in equation (25). R_x and R_y are the resistances of bonding materials. In the rest of the paper, these developed models will be called Model M. The little bulging of the soldering sidewalls is ignored and it is considered as a short cylindrical shape for the simplicity of calculations. The loose connections or the voids in soldering bumps ld to huge leakage of current. Therefore, the thermal energy liberated will be more. Hence, considering the resistance of such components is important in this paper. The basic thermal conduction resistance can be calculated as follows:

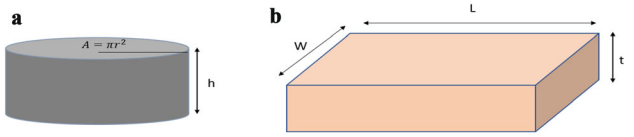

Figure 3. (**a**) A micro-bump soldering shape and its area. (**b**) The pad of the TSVs and its area.

$$R = \frac{Q}{kP} \tag{10}$$

where Q is the length of the conductor, P is the area of the conductor, and k is the thermal coefficient of the conducting material. Similarly, all resistors could be obtained as

$$R_1 = \frac{1}{x_1 A}\left(\frac{t_D}{k_D} + \frac{l_{ext}}{k_{si}}\right) \tag{11}$$

where $A = A_0 - \pi(r + t_L)^2$

$$R_2 = \left(\frac{t_D + l_{ext}}{x_1 k_f \pi r^2}\right) \tag{12}$$

$$R_3 = \frac{\ln(r + t_L) - \ln r}{2\pi x_2 k_L (t_D + l_{ext})} \tag{13}$$

$$R_4 = \frac{1}{x_1 A}\left(\frac{t_D}{k_D} + \frac{tSi_2}{k_{si}}\right) \tag{14}$$

$$V_p = tWL \tag{15}$$

$$V_s = \pi r^2 h \tag{16}$$

$$R_5 = \frac{t_D + tSi_2}{x_1 k_f \pi r^2} \tag{17}$$

$$R_6 = \frac{\ln(r + t_L) - \ln r}{2\pi x_2 k_L (t_D + tSi_2)} \tag{18}$$

$$R_7 = \frac{1}{x_1 A}\left(\frac{t_D}{k_D} + \frac{tSi_3}{k_{si}}\right) \tag{19}$$

$$R_8 = \frac{tSi_3}{x_1 k_f \pi r^2} \tag{20}$$

$$R_9 = \frac{\ln(r + t_L) - \ln r}{2\pi x_2 k_L t_{si3}} \tag{21}$$

$$R_s = \left(\frac{tSi_1 - l_{ext}}{x_1 k_{si} A_0}\right) \tag{22}$$

$$R_a = R_c = R_d = R_f = \frac{t}{k_f x_1 WL} \tag{23}$$

$$R_b = R_e = \frac{h}{k_s x_2 \pi r^2} \tag{24}$$

$$R_x = R_y = \frac{1}{k_b x_2}\left(\frac{2t + h}{\ln(A) - (\ln(V_p) + \ln(V_s))}\right). \tag{25}$$

3. Result analysis

The Autodesk tools set is used to draw the polygons and substituted material constants are used to get the analytical simulation results. The experimental setup permits more than 25000 mesh points for each of the components in the assembly. The run time was high because of these more mesh points to get accurate temperatures. Radiation and other effects are ignored. Heat flux is uniform and normal to the top surfaces. Adiabatic boundary conditions are applied on all four sides of the stacked system and isothermal between stacked surfaces. CFD results and model value were compared and various graphs drawn.

Footprint area A_0 of the setup used is 100 μm × 100 μm. The thicknesses of the first silicon die are 500 μm and l_{ext} = 1 μm. The bottom surface of the heatsink is assumed to be at 25°C. The top layers of each plane have a uniform power density of 700 W/mm^3, and each ILD layer of heat sources has 70 W/mm^3. The liner of TSV used is SiO_2 (k_L. = 1.4 W/(m K)). Low-k dielectricmaterials are used [27] for ILD (k_D = 1.4 W/(m K)), soldering (k_s = 1.0 W/(m K) and bonding (k_b = 1.0 W/(m K)). Since ILD will have power-dissipating metals, k_D is adopted to have the effects of metal within ILD layers. In the following sections, the various components affecting the temperatures inside the TSVs are discussed. A summary of the average errors and maximum errors is listed in Table 1.

3.1 *Variation of the filler material radius*

The thermal performance is studied by varying the different radii of the filler material (copper) used, in the experiments. To consider general manufacturability dimensions, the radius of the filler material 'r' is varied from 0.5 to 17 μm. Due to limitation of fabrications, $tSi_2 = tSi_3$ = 5 μm, chosen for 0.5 μm ≤ r ≤ 1 μm and $tSi_2 = tSi_3$ = 45 μm, chosen for 6 μm ≤ r ≤ 17 μm. Other parameters are as shown in figure 4a. As the radius (r) thickness of the filler material (copper) got increased from 0.5 to 17 μm the temperatures (ΔT) developed inside the TSV decreased. However, when 0.5 μm ≤ r ≤ 1 μm, a rise in temperature observed, because of more lateral thermal conduction. Model M achieves reasonable accuracy with the use of fitting coefficients. Model M follows CFD values. The maximum error between these two models is 12.7% and the average error between the models is 4.7%.

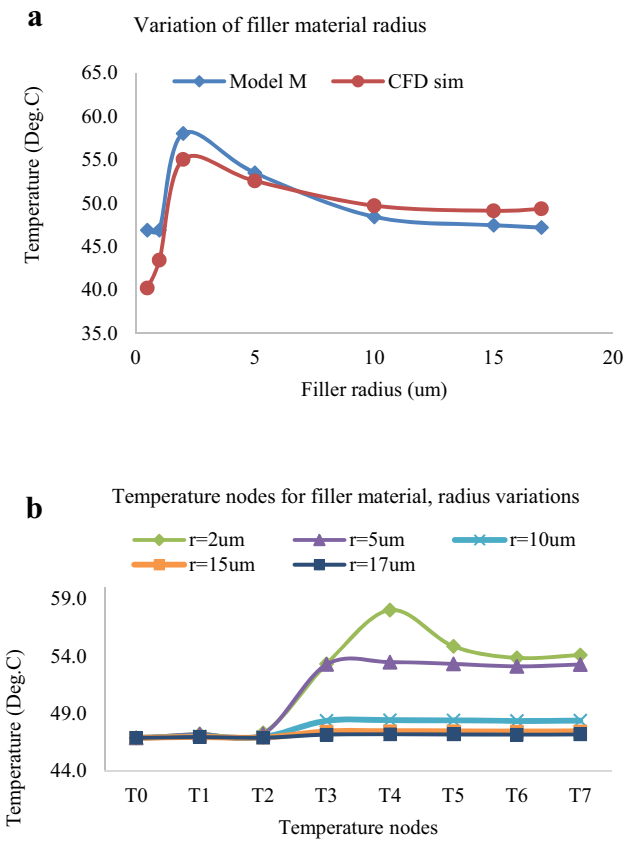

Figure 4. (**a**) Effects of variation of filler material radius in three planar, 3-D IC stacked systems. Other parameters used are t_L = 0.5 μm and t_D = 7 μm; for 0.5 μm ≤ r ≤ 5 μm $tSi_2 = tSi_3$ = 5 μm. For 6 μm ≤ r ≤ 17 μm $tSi_2 = tSi_3$ = 45 μm, x_1 = 1.5 and x_2 = 0.6. (**b**) Nodal temperature variations, in three planar, 3-D IC stacked systems, when the filler material radius is varied. Other parameters used are t_L = 0.5 μm and t_D = 7 μm; for 0.5 μm ≤ r ≤ 5 μm $tSi_2 = tSi_3$ = 5 μm. For 6 μm ≤ r ≤ 17 μm $tSi_2 = tSi_3$ = 45 μm, x_1 = 1.5 and x_2 = 0.6.

The different temperatures observed at the different nodes are as shown in figures 2a and 4b. As shown in (12)–(20) the resistances R_2, R_5, and R_8 significantly decrease, and (non-monotonically) abnormally from T_2, the nodal temperature starts decreasing. As filler material gets thicker than 0.5–5 μm, temperature variations in T_0–T_7 remain the

Table 1. The errors and temperature observations summary.

Models	Material	Max. error	Avg. error	Max. temp. (°C)	Min. temp. (°C)
Variation of filler	Cu	12.70%	4.7%	58.02	46.88
Variation of liner	SiO_2	13.15%	5.2%	53.78	53.66
Variation of substrate	Si	12.08%	4.8%	49.50	49.36
Variation of soldering	Cu-Sn	12.07%	4.8%	54.50	47.20
Group of TSVs	–	7.35%	1.4%	–	–

same inside the 3-D stacked assembly. The highest observed temperature is 58.02°C, and the lowest is 46.88°C.

3.2 *Variation of the liner material thickness*

The thickness (t_L) of the liner material SiO_2 is varied from 0.5 to 6 µm; this results in thermal energy getting accumulated inside the liner material, as shown in figure 5a. Other parameters considered are also presented in figure 5a. Here the maximum difference is 13.15%, and the average difference accuracy is 5.2% between Model M and CFD simulations.

As illustrated in (13), (18), and (21) R_3, R_6, and R_9 increase as, linear thickness increases, resulting in temperature rises. Figure 5b shows that T_0–T_2 and T_3–T_7. nodal temperatures remain almost constant irrespective of liner thickness, but there is a significant change from T_2 to T_3, because rest of the nodes are far from the heat sink; also the thermal circuits end in these nodes. The highest temperature observed is 53.78°C and the lowest is 53.66°C.

3.3 *Variation of the substrate material thickness*

If the thicknesses of tSi_2 and tSi_3 are varied, reduction in temperature is observed in the three planar 3-D IC stacked systems shown in figure 6a. Other parameters in this experiment are presented in figure 6a. Thicknesses within the range 1 µm $\leq tSi_2 = tSi_3 \leq$ 10 µm decrease the temperature inside TSV and for $tSi_2 \geq \leq$ 20 µm, temperature difference (ΔT) increases. As tSi_2 and tSi_3 increase, thermal resistance along a vertical path increases rather than in a horizontal direction. Hence, as specified in (11), (14), and (19), R_1, R_4, and R_7 increase as substrate thickness increases, as shown in figure 2a. In figure 6a, Model M's overall error difference is 12.08% and the average error difference is 4.8% with the actual simulations.

Figure 6b presents different nodal temperatures. The maximum value is 49.50°C. The smallest value is 49.36°C. Non-monotonical slopes are observed at nodes T_2–T_3 for all variations of the substrate thicknesses, because the more efficient heat sink absorbs heat from its serial heat sources. Also, the thermal circuits end at these nodes.

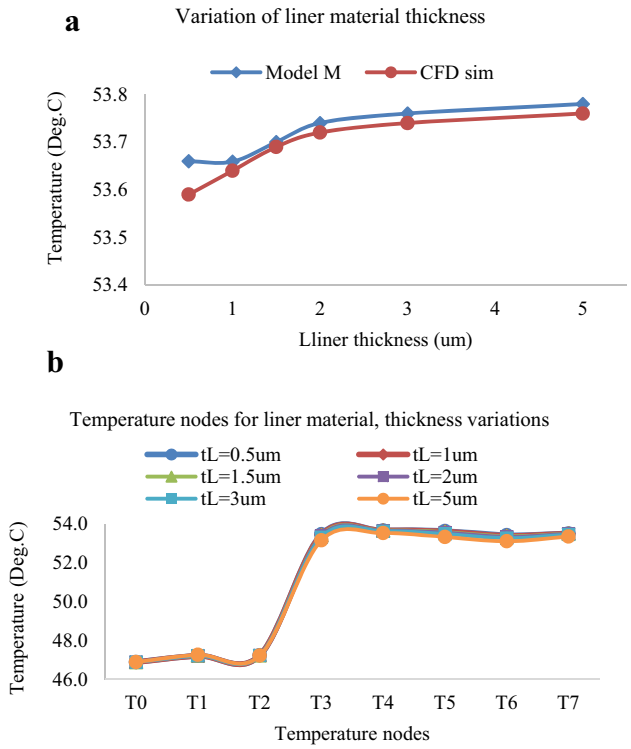

Figure 5. (**a**) Effects of variation of liner material thickness in three planar, 3-D IC stacked systems. Other parameters used are $tSi_2 = tSi_3 = 45$ µm, $r = 5$ µm, and $t_D = 7$ nm. For 0.5 µm $\leq t_L \leq 5$ µm $x_1 = 1.5$ and $x_2 = 0.6$. (**b**) Nodal temperature variations, in three planar, 3-D IC stacked systems, when the liner material thickness is varied. Other parameters used are $tSi_2 = tSi_3 = 45$ µm, $r = 5$ µm, and $t_D = 7$ nm. For 0.5 µm $\leq t_L \leq 5$ µm $x_1 = 1.5$ and $x_1 = 0.6$.

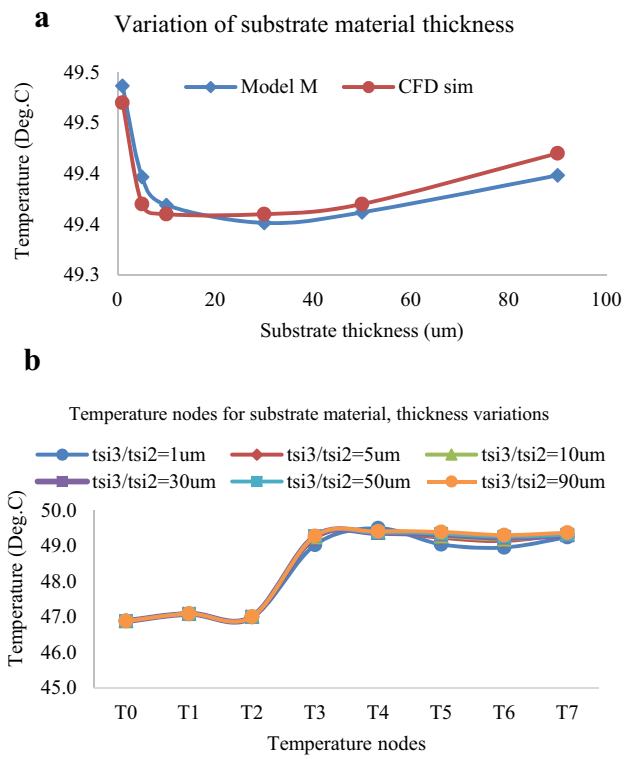

Figure 6. (**a**) Effects of variation of substrate thickness in three planar, 3-D IC stacked systems. Other parameters used are $t_L = 1$ µm, $t_D = 7$ µm, and $r = 8$ µm. For 10 µm $\leq tSi_2 = tSi_3 \leq 90$ µm $x_1 = 1.5$ and $x_2 = 0.6$. (**b**) Nodal temperature variations in three planar, 3-D IC stacked systems, when the substrate material thickness is varied. Other parameters used are $t_L = 1$ µm, $t_D = 7$ µm, $r = 8$ µm, $x_1 = 1.5$, and $x_2 = 0.6$.

3.4 *Variation of soldering material thickness*

T soldering material could play an important role while using the bonding layers between two stacked dies. This is not well studied as a part of thermal circuits in the series of papers referred to. This is the major thermal heat component that distributes heat next to TSV in the stacked assembly. Hence, ignoring this may not lead to a complete study of the components involved in the stacking of 3-D IC systems. Figure 7a covers the effects of thickness variations. Other parameters considered are presented in figure 7a. As specified in (24), R_b, R_e are the resistances of soldering materials. For 1 µm $\leq h \leq$ 10 µm, the temperature increases with a speedy slope; however, for $h \geq$ 10 µm, the temperature difference (ΔT) takes almost the same temperature. This shows that the thermal resistance will decrease remain at almost same temperatures, as it allows a more vertical thermal path for increased thicknesses. Model M's average error is 4.8%, whereas the maximum error is 12.07%. Figure 7b shows that the nodal value changes as the thickness of soldering material varies from 1 to 30 µm.

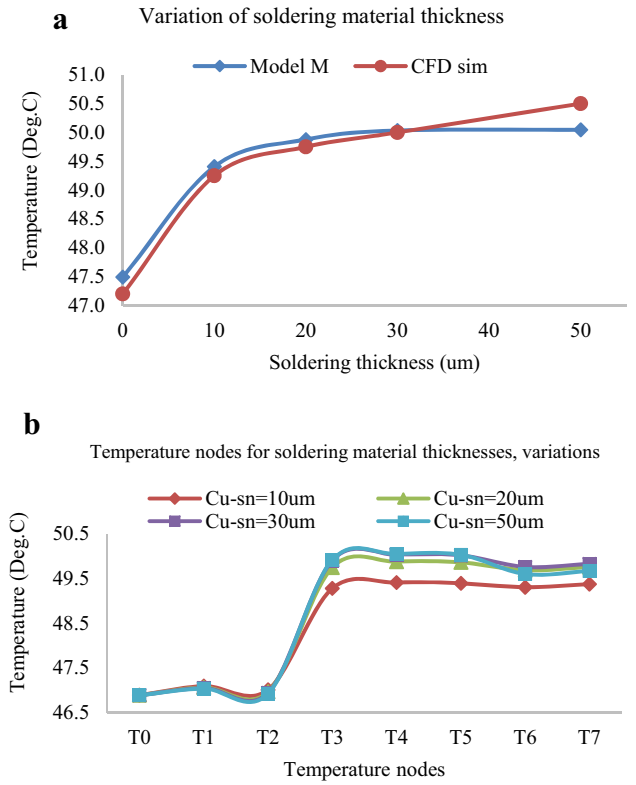

Figure 7. (**a**) Effects of variation of soldering material thickness in three planar, 3-D IC stacked systems. Other parameters used are t_L = 1 µm, t_D = 7 µm, and r = 8 µm. For 0.5 µm $\leq h \leq$ 50 µm x_1 = 1.5 and x_2 = 0.6. (**b**) Nodal temperature variations in three planar, 3-D IC stacked systems, when the soldering material thickness is varied. Other parameters used are t_L = 1 µm, t_D = 7 µm, and r = 8 µm. For 0.5 µm $\leq h \leq$ 50 µm x_1 = 1.5 and x_2 = 0.6.

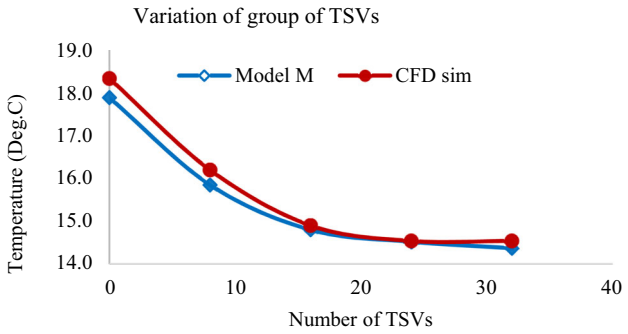

Figure 8. Temperature variation in three planar, 3-D IC stacked systems, when multiple TSVs are used instead of single TSVs. Other parameters used are t_L = 2 µm, t_D = 7 µm, $tSi_2 = tSi_3$ = 20 µm, and r_0 = 10 µm. For $1 \leq n \leq 32$ x_1 = 1.5 and x_2 = 0.6.

In figure 7b, the T_2–T_3 nodes show non-monotonical thermal values because the heat sink absorbs from the heat sources; also the thermal circuits end at these nodes. The maximum heat dissipated is at 54.50°C, and the minimum observed temperature is 47.20°C.

3.5 *Variation of the group of TSVs*

Many studies have revealed that, instead of a thicker diameter of a single TSV, thinner diameters of many TSVs can reduce the temperature rise inside the TSVs. Usually, TTSV will be used as a solution. However connecting the same signal net to multiple TSVs, similar to via ladders, or via pillars fashion, as used in the physical design of the chip-making process, can reduce the total resistance as well as improve the EM (electromigration) and physical strength of the signal nets. Therefore, an experiment is carried out where a TSV with radius 'r_0' is divided into 'n' number; hence the radius of new TSVs should be related to the original TSVs radius of 'r_0' as $r_n = \frac{r_0}{\sqrt{n}}$. Since the thermal resistance goes in a parallel fashion, the total resistance effect will decrease.

Figure 8 illustrates the decrease in temperature difference (ΔT), as multiple TSVs increase till 32 sets connecting to the same signal net. Here, the lateral surfaces increase to conduct the heat. Therefore, heat gets distributed in multiple TSVs. However, it is limited to value 'n'. The total error difference is about 7.35%. Model M's average error differs within 1.4%, compared with CFD simulations.

4. Conclusions

The present available literature reviews, disadvantageously or unfortunately, are lacking in simple models. Lateral thermal conduction has been given less importance and heat losses are ignored in the 3-D IC stacks, where the

TSVs join or connect from one plane to another. Heat dissipation path from the source of heat is not simply the addition of vertical and horizontal resistance networks. It spreads out three-dimensionally. Such a complex phenomenon is fundamentally flawed by incorporating both vertical and horizontal thermal resistance networks captured in accurate heat dissipation paths. These models can be extended to a different process with different materials and different geometrical parameters. Different materials will decide the x_1 and x_2 values. The various graphs reveal different facts. The modeled equations follow the commercially available tool simulations. The error correction gets uses of multiplication factors. On increasing the thicknesses of filler material the thermal resistance decreases, as more heat conducts through the filler material. Another study shows that, on increasing the thickness of dielectric material, thermal energy increases inside liner material. Also it is seen that, on increasing thickness of the substrate material, the thermal issue re-appears, because it must carry the same power developed in all TSVs materials. On increasing the thickness of soldering material the thermal resistance decreases, as more heat passes through the soldering material, in a vertical path. The group of TSVs effect shows that the thermal issue reduces as heat gets distributed among other TSVs.

Another important observation is that, in general, the smaller the thickness of filler, liner, soldering, and substrate materials, the larger the heat conducted in the horizontal direction than in vertical direction. Conversely, for higher thickness of the afore-mentioned materials, heat conduction is more in vertical than horizontal directions; hence, the abnormal temperature curves are observed in the graphs. Thermal residual stresses in silicon can be the scope of further analysis of this paper. In this work, it has been demonstrated that, presented thermal models can have 4.18% accuracy compared with software simulated values.

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Subscripts and symbols

R_1, R_4, R_7	Resistances of the silicon substrate (Ω)
R_s	Resistance of the heatsink (Ω)
R_3, R_6, R_9	Resistances of the liner (Ω)
R_2, R_5, R_8	Resistances of the filler (Ω)
R_x, R_y	Resistances of the bonding material (Ω)
R_a, R_c, R_d, R_f	Resistances of TSV pads (Ω)
R_b, R_e	Resistances of the soldering material (Ω)
ΔT	Temperature difference (°C)
T_0–T_7	Temperature nodes of the 3-D IC stack (no units)
q_1, q_2, q_3	Voltage sources (W/mm^3)
x_1, x_2	Fitting coefficients (no units)
A_0	Footprint of experimental area (μm^2)
A	Larger area of the silicon substrate (μm^2)
tSi	Thickness of the silicon substrate (μm^2)
t_D	Thickness of the ILD (Inter-Layer Dielectric) layer (μm^2)
t_b	Thickness bonding layer (μm^2)
k_{si}	Thermal conductivity of silicon substrate (W/m K)
k_D	Thermal conductivity of ILD (W/m K)
k_b	Thermal conductivity of bonding material (W/m K)
k_L	Thermal conductivity of liner (W/m K)
k_f	Thermal conductivity of filler (W/m K)
k_s	Thermal conductivity of soldering material (W/m K)
r	Radius of TSV (μm)
t_L	Thickness of insulator liner (μm)
l_{ext}	TSV segment, extended into silicon substrates (μm^2)
V_p	Volume of TSV pad (μm^3)
V_s	Volume of soldering bump (μm^3)
h	Height/thickness of the soldering bump (μm)

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