Sādhanā (2020)45:207
https://doi.org/10.1007/s12046-020-01440-z

A time-interleaved pipelined ADC with ultra high speed sampling

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MS received 25 March 2020; revised 6 May 2020; accepted 5 July 2020

Abstract. Based on a standard 0.18μm BiCMOS process, a 12 bit 2GSps ADC is achieved using time-interleaved pipelined architecture in this work. The DC offset caused by the mismatch of ADC channels is removed due to the application of digital calibration technology, which improves the performance of the ADC. The power supply voltage is 1.8 V and the power consumption is 100 mW for each lane. The measurement results indicated that the circuit in this paper can be used in multi-channel time-domain interleaved pipelined ADC architecture to achieve a 2GSps ultra high speed ADC.

Keywords. Time-interleaved; DC offset; digital calibration; pipelined ADC.

1. Introduction

In modern communication system, high performance analog-digital converters (ADCs) are key components with the characteristics of low power and high spurious free dynamic range (SFDR). High speed ADCs with IF sampling capability are widely applied in wireless communication system, which enable the architecture of cellular base stations evolving from multi-narrowband receivers to a single wideband multi-channel receiver. That simplifies the signal processing, and hence reduces the cost and complexity of communication system [1–5].

Different ADC architectures have various advantages, such as low power, high resolution or high speed. Achieving low power and high performance ADCs is now a research hotspot, especially for hand-held mobile terminals. Pipelined ADC is considered as a good candidate to fulfill the trade-off between speed and resolution, and relatively moderate power dissipation could be achieved simultaneously. Most reported pipelined ADCs have the features of 12-16 bits resolution, 70-80 dB SNR, and 85-95 dB SFDR with 100-300 MS/s sampling frequencies [6–9]. High frequency signal in the switched-capacitor circuit of front-end sampling will increase the linearity distortion and the signal path mismatch between the sampling circuits and multiply digital-to-analog converter (MDAC) sampling network is another source of linearity distortion, which can degrade the SFDR. Therefore, realizing good SFDR with high SNR is a challenge for pipelined ADC with IF sampling, especially at the cost of relative low power dissipation. The input buffer is the key component to achieve high linearity with IF sampling [10].

Recently, high-speed ADCs with resolution greater than 10-bits and sample rates higher than hundred MHz have been spread [11–14], and some of them has reached 14-bits with sample rates well into gigahertz range [15–17]. To address the GHz range sampling requirement for the mobile communication service industry, high performance track and hold (T&H) front-end with large bandwidth is needed to guarantee a good track phase for a broad frequency in the GHz spectrum section [18]. A BiCMOS input buffer, such as in [15] and [19], would be more interesting for greater resolution and speed, and those GHz ADCs achieved in a standard CMOS process below 65 nm usually benefit from the scaled down parasitic parameters [16, 17, 20–22], which also means a higher cost. In this work, we chose a standard 0.18 μm BiCMOS process to implement a 12-bit 2GSps ADC, which is a trade-off between the speed requirement and the cost. An improved T&H with good linearity is proposed, and the effectiveness is proved by the measurement results. Based on the proposed T&H, a 12-bit 2GSps pipelined ADC is demonstrated. In order to eliminate the DC offset and other errors caused by the mismatch of ADC channel, digital calibration technology is illustrated and results gave better performance. This paper is organized as follows. Section 2 presents the ADC design principle with ADC architecture and digital correction logic. Section 3 describes the measurement results, and in section 4, the conclusions are provided

2. ADC design

2.1 *ADC topology*

High-speed ADCs usually use multiple time-interleaved pipelined architecture to achieve the overall design to

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Published online: 18 August 2020

achieve GSps ultra high speed analog to digital conversion [23]. To achieve a 2GSps high speed ADC, the mathematical modeling based on Matlab is completed for each ADC channel with sample and hold device. The time-interleaved GSps high speed ADC shown in figure 1 is composed of four lanes, and each ADC lane is composed of 6 sub-ADC stages, and the 6-level process is implemented by 3-3-3-3-3-2 pipelined architecture. The reference channel for error calibration is not shown in figure 1 which has the same topology as other four lanes.

The single channel ADC using pipelined architecture includes a sample-and-hold (S&H), five 3-bit ADCs, five DACs, a clock buffer, a regulator, a voltage reference generator and a 2-bit flash ADC. The analog input is sampled and held by the S&H part, and then it is quantized to three bits by the 3-bit ADC. The output of the ADC is fed to the 3-bit DAC, and then the DAC output is subtracted from the held signal of the S&H part. The difference is magnified four times and then fed to the second stage, and the residue is also preceded by the second ADC, which provides another three bits output. The process continues until the gained-up signal reaches the 2-bit flash ADC at last. The output of each level is converted to 12 bit output by digital logic module. The clock is generated by the clock buffer circuit, and the non-overlapping clock is generated by a special phase generation circuit, which is buffered in each level to achieve the timing requirements, so as to ensure the proper timing of pipeline operation and minimize the non-overlapping time [6], [24], and a high performance clock buffer with good low-jitter sampling is obligatory to support high frequency input signal. A reference buffer is necessary to maintain a stable differential voltage for the DAC. The whole internal reference source is designed to provide reliable reference voltage and current for the chip. The circuit uses first-order temperature compensation to achieve a high precision of the output voltage under the PVT change.

The output encoding data and timing schemas for single channel pipelining are illustrated in figure 2. Each stage outputs the bits at different points, so the sample at the same time should be time-aligned by shift registers, and then the time-aligned bits are fed to the digital correction logic module [25]. The sampled input signal outputs the time-aligned bits and then processes the following sampling signal.

2.2 *T&H*

The T&H front-end is used to isolate the ADC external driving network from the kick-back and charge injection caused by the switching of the sampling capacitances [10]. The proposed T&H front-end is shown in figure 3. The T&H block consists of an input buffer, an auxiliary stage and an output buffer. The input buffer with switched-emitter-follower (SEF) stage uses linearity compensation technique to maintain GHz input linearity performance, which enhances the analog input bandwidth of the T&H front-end and makes it suitable for high speed sampling system [26]. The capacitor Cc is connected in parallel to the emitter of Q4 and the emitter of Q12 by mirror load technology. Its charge-discharge current equals the charge-discharge current of hold capacitor C_H. Therefore, for high frequency applications the capacitive current of the replica circuit maintains constant emitter current, eliminating the influence of the transconductance and current nonlinearity of the driving bipolar transistor on the sampling nonlinearity. The distortion is also optimized by means of a high-impedance PMOS output load, and low-noise performance is achieved using a bipolar differential input stage (only shows the single-channel circuit in figure 3) [27]. During sampling phase, transistors Q7 ~ Q9 turn off, and the output of the auxiliary stage replicates the sampling voltage. When in hold mode, transistors Q5 and Q12 turn off, and Q7 ~ Q9 turn on. The closed-loop, composed of Q7, Q8, Q11,

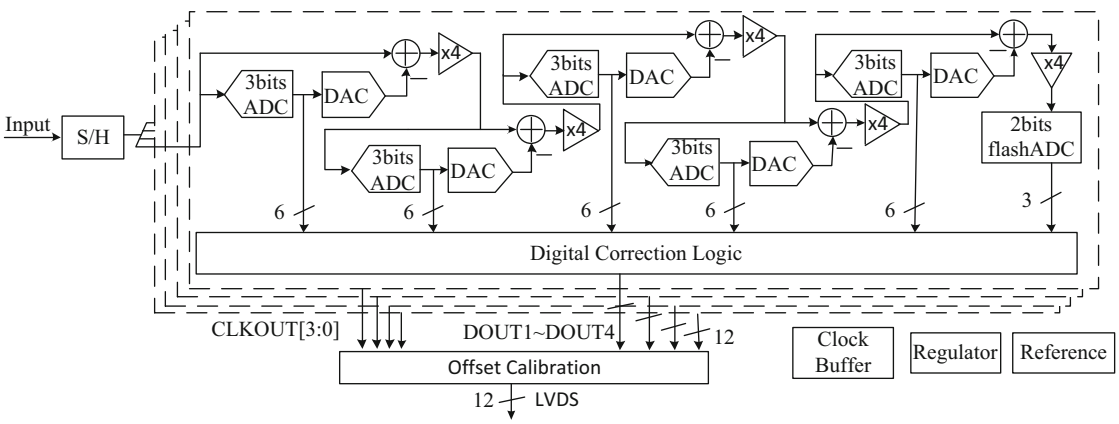

Figure 1. Time-interleaved GSps high speed ADC topology.

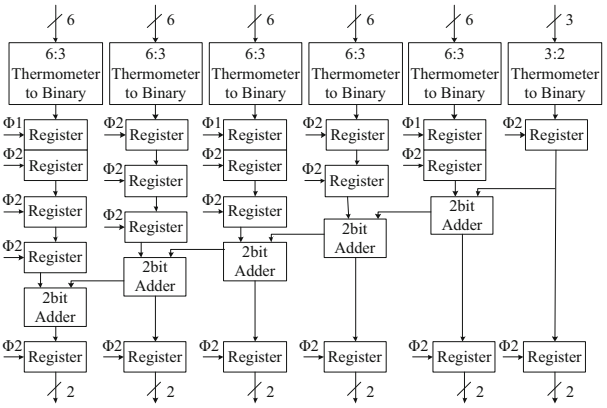

Figure 2. Digital encoding data principle.

Q14 ~ Q18, maintains a stable biasing voltage for the SEF circuit, which will decrease the settling time and result in a higher sampling bandwidth compared with T&Hs reported in [27] and [28] .

2.3 *Sub ADC*

The sub-ADC utilizes the same topology, and it is presented in figure 4 [7]. Non-overlapping clock Ph1 and Ph2 control the sampling and integration process of the sub-ADC. During phase Ph1, the input signal is sampled to the eight capacitors, and at the same time the signal is preceded by the comparator of the three bits ADC. During phase Ph2, the output of the sub-ADC controls the switches of the DAC, and the output settles finally. High frequency sampling for high-resolution pipelined ADCs needs good clock circuit, which provides reliable clock phase for sampling and charge transform. It also means low clock jitter design

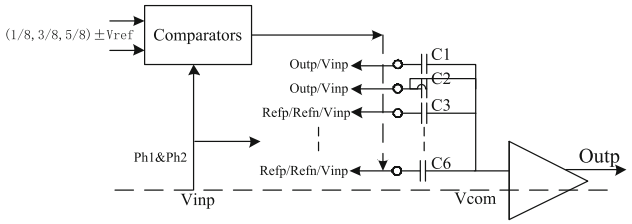

Figure 4. Sub-ADC topology.

is necessary to reduce sampling variations. In this work, input clock amplification and duty cycle stabilization techniques are utilized to ensure high-precision sampling. Low noise amplifier and delay locked loop are used in the clock circuit design. Dithering technique is used to improve small signal linearity, INL and DNL. The injected known random amount of noise decreases SNR to exchange for better SFDR.

A telescopic gain-boost operational amplifier (op-amp) used in the ADC shown in figure 5 is carefully designed to achieve good trade-off between gain-bandwidth (GBW) and power dissipation, and ensures enough gain, phase margin and settling time. The folded-cascade op-amps increase the dc gain of the whole op-amp. The N-gain-boost op-amp topology is similar to the P-gain-boost shown in figure 5 except for the PMOS input transistors. To achieve the objective bandwidth, g_m of the input M1 should be large enough at a certain source current I_d, and two-stage topology is preferred, not showing the second-stage in detail. Figure 6 presents the corner simulation results of the loop gain, the bandwidth and the phase margin for the op-amp in stage-1 in different temperature (-45°C, 60°C and 125°C), which indicates that in the worst case the loop gain is 72 dB, the loop bandwidth is 3.5 GHz and the phase margin is 57.

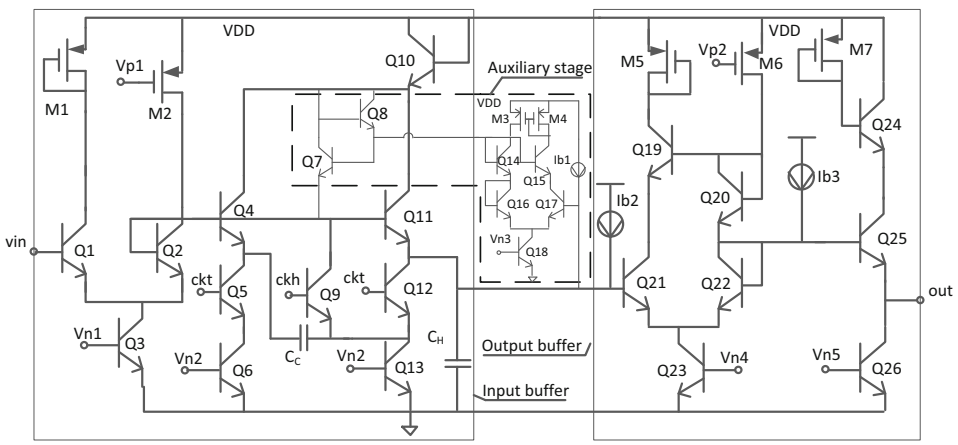

Figure 3. T&H front-end (half-cell).

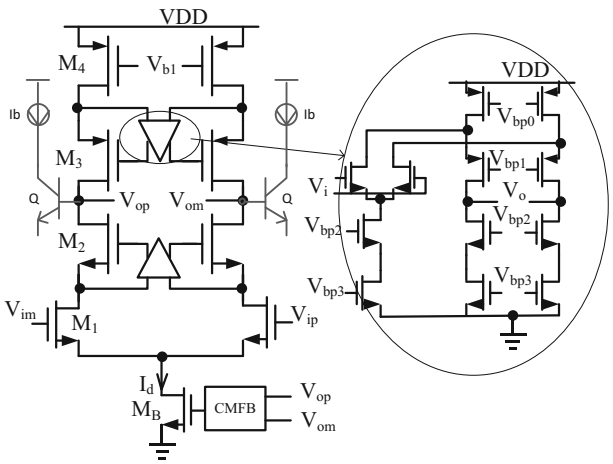

Figure 5. Op-amp topology in this work.

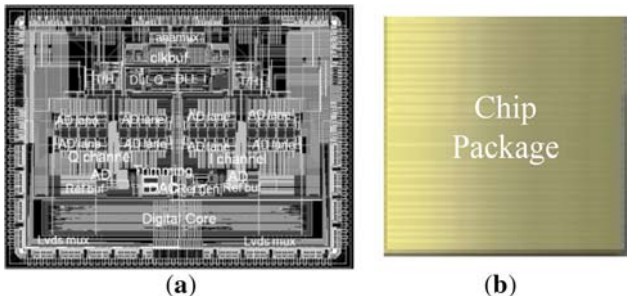

Figure 8. (a) Layout, (b) chip package.

2.4 *Digital calibration logic*

Digital calibration techniques are usually used to correct the nonlinearity caused by capacitor mismatch, open-loop gain of op-amp, channel gain error, skew, jitter and so on

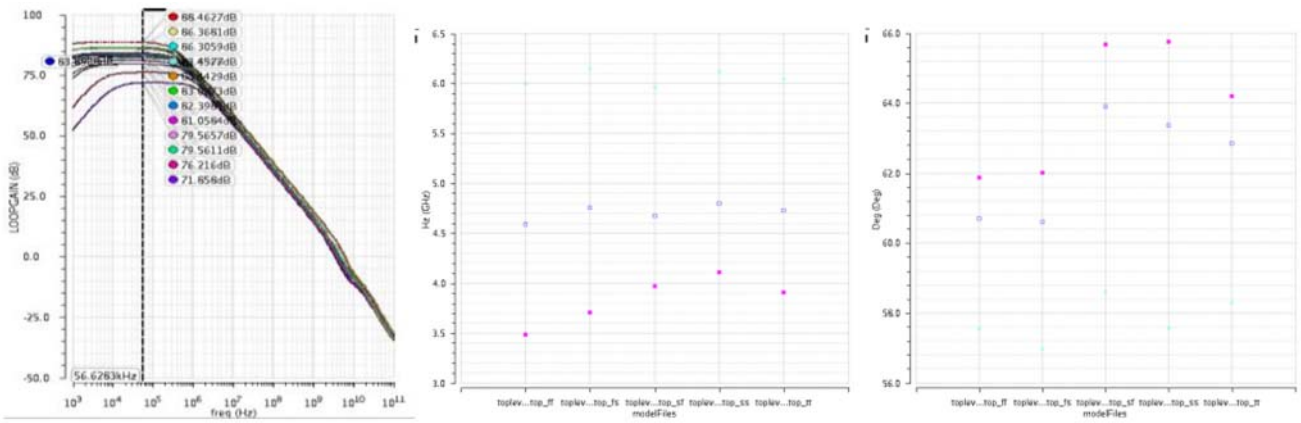

Figure 6. Corner simulation results of the op-amp in stage-1 in different temperature.

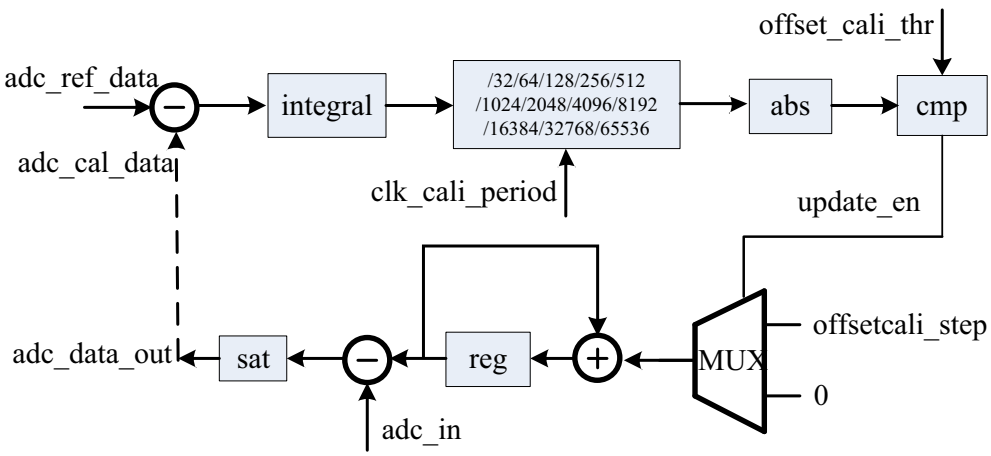

Figure 7. DC offset digital calibration topology.

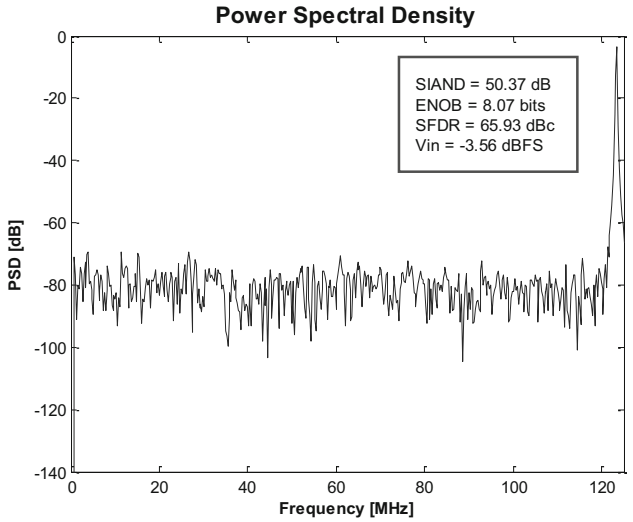

Figure 9. 123 MHz input signal with 250MSps for one lane.

[6]. At the same time, in this paper digital calibration module is used to remove the above errors background based on a pseudorandom sequence and the method discussed in [15].

The DC offset digital calibration principle is shown as follows: The difference value is achieved by subtracting the sampled digital signal with the theoretical intermediate value $2^{n-1}/2$ of the sub-ADC sampling data, and it is summed by an accumulator with enough periods, then the final accumulation value will converge to the channel mismatch error. Finally, the error value will be eliminated by the iteration of the feedback loop. The detailed calibration topology is illustrated in figure 7. The signal *adc_ref_data* originates from the reference ADC, and the initial *adc_cal_data* value is the signal from the sub-channel to be calibrated. The difference signal of the sub-ADC and the reference ADC is integrated within configurable data length, and then the average value is calculated using shift register. After taking the absolute value of the data, it is compared with the DC calibration threshold value *offset_cali_thr*, which is configurable. If the difference value is higher than the threshold value, the configurable calibration step *offsetcali_step* is accumulated until the value reaches the threshold value. The calibration data is finally subtracted from the un-calibrated sub-channel to obtain the ADC output. The analog inter-stage gain errors are also corrected on-chip using digital radix converter with a background calibration engine.

3. Measurement results

The ADC was designed based on parameter optimization and noise analysis, and it was fabricated in a standard 0.18 μm BiCMOS process. The whole circuit area measures 6.5 × 8.5 mm^2. Figure 8 shows the layout and chip package. The silicon area of the chip is not currently optimized due to the existences of test modules and dummy channel. The best achievable area would be less than 4 × 6 mm^2. To achieve good test results, the input signal path needs to be designed properly. The analog input source was provided by a double balun input network, which converts the single-ended signal to a differential input for the ADC and covers an input signal range from 4.5 MHz to 3 GHz with good linearity. The pipelined ADC operates from a single 1.8 V supply, which is provided by Agilent E3631. The sampling clock is generated by an on-chip frequency divider from an off-chip clock source with low jitter of less than 50 fs. The digital output sequence of the one ADC lane is captured by

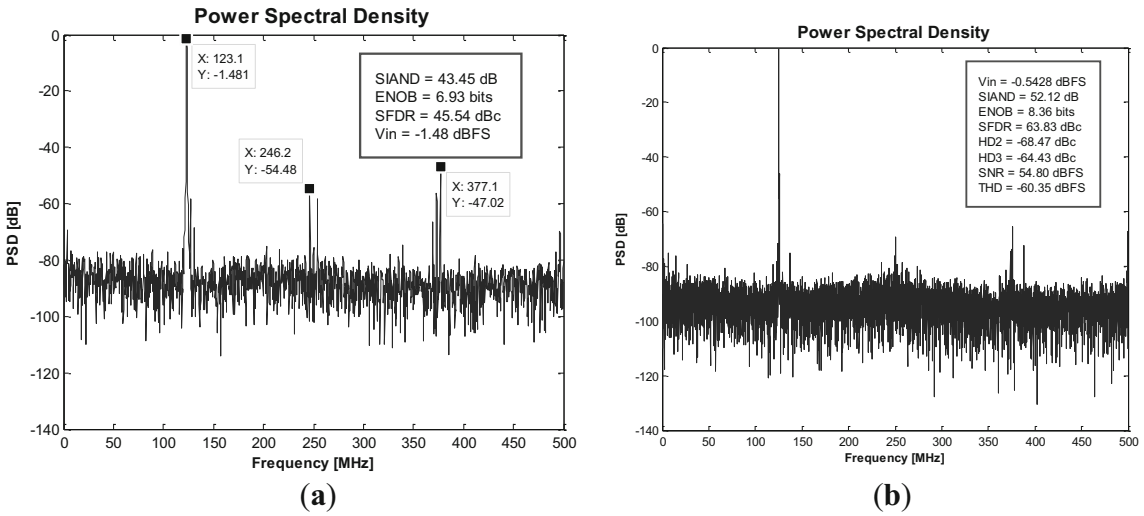

Figure 10. FFT result of 123 MHz input signal with 1GSps (a) before calibration, (b) after calibration.

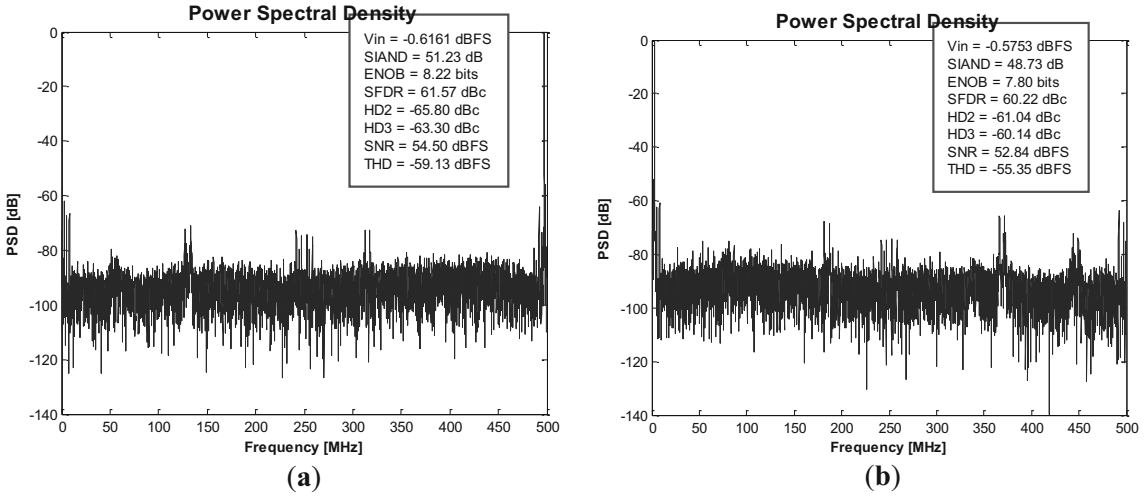

Figure 11. (a) 498 MHz input signal with 1GSps, (b) 998 MHz input signal with 1GSps.

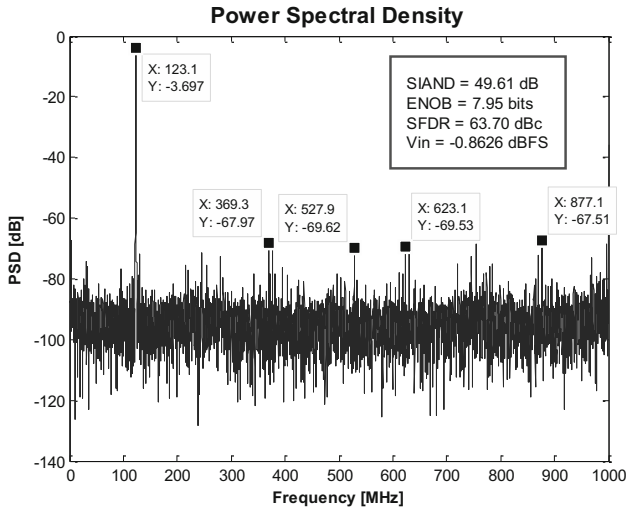

Figure 12. 123 MHz input signal with 2GSps.

Agilent Logic analyzer 16804A, and special MATLAB program for the signal processing of ADC is used. The equivalent power dissipation of each ADC lane is about 100 mW.

The FFT result is shown in figure 9, the input signal is 123 MHz with a 250 MSps sample rate for one ADC lane. The PSD results before calibration and after calibration of the time-interleaved high-speed ADC with 1GSps sampling frequency are illustrated in figure 10 with input signal centered at 123 MHz. It is indicated that the SFDR increases 18 dB. The SFDR is nearly 63.8 dBc with an SNR of 54.8d BFS with calibration. In addition, a 498 MHz and a 998 MHz input signals are applied for the pipelined ADC, respectively, shown in figure 11. The achieved SNR and SFDR are 54.5 dBFS and 61.6 dBc for 498 M input signal, and 52.8 dBFS and 60.2 dBc for 998 MHz input signal. When the sample rate increases to 2GSps, the third harmonic distortion and the interleaved spurs get close for a -0.9 dBFS signal amplitude, and the third harmonic distortion is the only limitation for the SFDR when the signal amplitude is higher (figure 12).

Table 1. Performance comparison with other reported ADCs.

References	Power W	Fs GHz	SNDR dB	SNR dB	Process nm
[15]	23.9	2.5	–	61	130 nm BiCMOS
[30]	0.575	1	–	62	180 nm BiCMOS
[31]	0.25	1	55	59	130 nm CMOS
[32]	0.35	0.8	58	60	90 nm CMOS
[33]	1.26	1	56	57	180 CMOS
This work	0.46	2	50	55	180 nm BiCMOS

A selection of published Nyquist ADCs [29, 30] based on BiCMOS and CMOS process with closest in performance and sampling rates to this work is expanded in table 1. The summary includes the power, sampling rate, SNDR, SNR and process. This work is not excellent for its SNDR and SNR, but a lower power dissipation with 2GSps sample rate is achieved, which is suitable for the application of low power device with several GSps sampling requirement.

4. Conclusions

A 12-bit 2GSps interleaved pipelined ADC is achieved in a standard 0.18 μm BiCMOS process in this paper. Digital calibration technology is applied to improve the

performance. Each channel occupied 100 mW power dissipation with a sampling frequency of 500 MHz. Measurement results for input signal frequency of 123 MHz, 498 MHz and 998 MHz are shown. For 1 GHz sample rate, the SNR of the ADC is 54.8 dBFS, 54.5 dBFS and 52.8 dBFS, respectively, and the SFDR is 63.8dBc, 61.6dBc and 60.2dBc, respectively. The SNDR is limited by the third harmonic distortion when the sample rate increases to 2 GHz.

Lower power dissipation would be achieved if the 12-bit 2Gsps interleaved pipelined ADC implemented in 90 nm or even 45 nm technology due to the less parasitic effect. Therefore, most of recent works of ADCs higher than 2Gsps sampling rate are implemented in nano-dimension. In our work, we take a trade-off between the cost and several GSps sampling requirement.

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