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Novel realizations of digitally controlled low power current controlled current conveyor for tuning filter outputs with constant power consumption

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Abstract. This paper presents a dual output resistance tunable current controlled current conveyor (DO-RTCCCII). In the existing current conveyor the change in bias current is required to alter the design parameter R_x which is the intrinsic resistance of input X terminal. This variation changes the internal dc bias conditions such as saturation margins as well as total power consumption of the block. A resistance trimming block is added at X terminal which is controlled by some programmable bits. The usage of programmable bits helps to achieve the desired response without changing bias current, dc operating point and total power consumption. The port relationships of the DO-RTCCCII block are checked and the circuit and design parameters of current follower, voltage follower are analyzed. The operation of filter circuit is also included to illustrate usefulness of the proposal. The circuit has been designed and simulated using 28 nm CMOS bulk technology model parameters on Cadence Virtuoso/AMS environment (eldo simulator) using 0.75 V supply voltage and results have been verified with post layout netlist.

Keywords. Current controlled current conveyor; digital programmability; filter tuning; variable resistance; electronic tuning.

1. Introduction

There is significant research interest in current mode circuits as is evident from their adoption in applications such as instrumentation, analog signal processing, telecommunication systems, high speed computer interfaces, and the backplane of complex electronic systems [1]. However, the voltage mode circuits have prevailed due to ease in measuring voltage, very high input impedance while looking into the gate of MOS device and the ease with which high voltage gain is achievable. However, the behavior of voltage mode circuits is severely affected with supply voltage downsizing and subsequent reduction in threshold voltage.

The restrictions imposed on the performance of current mode circuits are not that stringent as the emphasis is on branch currents instead of node voltages. As the supply voltage has become the major concern in modern electronic circuit especially using portable and battery powered equipment so the circuit with low-voltage operation has become necessary. The current mode techniques are more suitable for these purposes in comparison with voltage mode ones [2–6].

Further, tunable characteristic of an analog cell is desirable feature to cancel offsets without changing basic characteristics of the circuit and it controls its performance parameters. Significant research efforts have been put in order to provide tuning feature via digital and analog methods. The digital tuning is preferred over analog tuning due to limitations for low voltage applications owing to limited allowable range [7]. Second generation current controlled current conveyor (CCCII) is an analog block having terminal characteristics similar to current conveyor CCII except an electronically controllable resistance at X terminal. The resistance is varied by changing the input bias current which alters the dc bias conditions. In literature some basic tuning is performed using the feature of variability of resistance with bias current [8–12] of current conveyor blocks e.g., DO-CCCII. However, this leads to increase in total dc power consumption as bias current is dc current flowing in every branch of current conveyor block. Digital programming is also explored in [13–17]. Active RC filters [13, 14], Gm-C filters; suffer from either poor

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linearity or higher power consumption issue. For improving these two parameters Gm-RC [15–17] filters are used to improve linearity and power consumption but due to the usage of resistor and capacitor banks. These filters suffer from higher process variation. To control process variation in Gm-RC filter programming is involved for tuning the values of resistance and capacitances which requires resistor and capacitor banks, reference voltage generator and amplifiers. Due to usage of these blocks the addition of programming or tuning feature in Gm-RC filter increases linearity at the expense of highly increased area and power consumption. Some authors have used digital programming to reduce area as well as power consumption by avoiding reference generation blocks e.g., bandgap. These digital programming methods [18–30] include variation of bias current, Current Distribution Networks (CDNs), and R-2R networks. The CDN [18–28] is included at Z port of CCCII block. This CDN network architecture increases the area of CCCII block due to addition of branches of digitally controlled CDNs and some power consumption. In deep submicron technology CDN network also suffers from the device degradation issues. Few works based on resistor networks such as simple resistor networks [29] and R-2R network [30], are available. The R-2R network, however, increases area of the circuit and also increases the current consumption as these networks use switches to bypass current into ground terminal when switches are in OFF condition. In this paper digital tuning concept is explored and a new block of RTCCCII circuit is proposed which is implemented with less area and power consumption. It can be implemented in the running status of circuit and helps to overcome the circuit offsets so that theoretical results match closely with the one predicted by CAD tools.

In this paper resistance tunable current conveyor (DO-RTCCCII) is proposed. The resistance at the X terminal of DO-RTCCCII is adjusted through externally controlled digital bits. There are no major changes in dc bias conditions in the proposed method therefore the power consumption remains almost constant for every combination of resistance in contrast to CCCII where power consumption changes with variation in resistance. Thus, this technique provides flexibility to user to change characteristics at the start of application and tune the run time response as per requirement using digital bits which is useful for offset cancellation.

2. Existing current controlled current conveyor

Figure 1 shows the symbolic diagram of the existing DO-CCCII and its CMOS based schematic [3] is depicted in figure 2. It uses one mixed trans-linear loop comprising of transistors M1 to M4 as input cell. Transistors M5, M6, M7, M8 and M9 allow dc biasing to the mixed loop by bias current I_B. The circuit acts as a voltage follower between terminal Y and terminal X, and presents high input

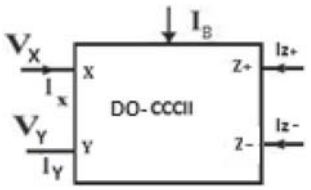

Figure 1. Symbol for basic DO-CCCII.

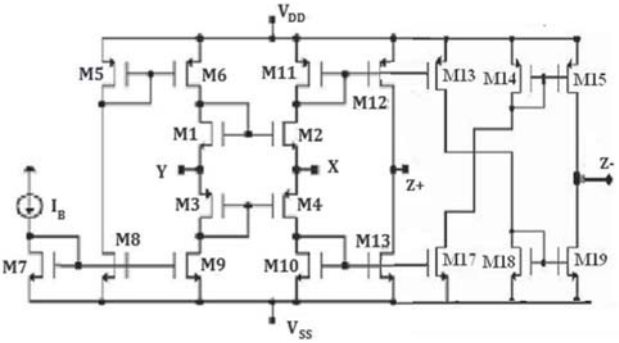

Figure 2. CMOS based circuit of DO-CCCII.

impedance at terminal Y and low impedance at terminal X. The current at branch related to node Z is replica of the current flowing through terminal X and is realized using two complementary mirrors.

The terminal relationship between current and voltage variables for different terminals of the basic CCCII block is represented as

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} R_x & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{1}$$

where

$$R_x = \frac{1}{\left(g_{m_2} + g_{m_4} + \left(\frac{1}{r_{o_2} || r_{o_2}}\right)\right)} \sim \frac{1}{\sqrt{8\beta_n I_B}} \tag{2}$$

where g_{m2} and g_{m4} are transconductance of the MOS transistors M4 and M2 used in figure 2 while r_{02} and r_{04} corresponds to output resistance of the MOS transistors M4 and M2.

The CCCII based circuits use R_X for adding electronic tunability to the design therefore bias current (I_B) need be changed. The transistors in figure 2 are biased in saturation region for proper operation and bias current is proportional to square of the overdrive voltage. The dc operating conditions such as overdrive voltage and saturation margin of every MOS device may get deviated with bias current change. The higher deviation of bias conditions of MOS transistors may affect the operating region of MOS devices

which may alter the terminal relationship. With change in the bias current, the currents of every branch show similar change due to inherent current mirror strategy. It can therefore be concluded that bias current change gives significant change in total power consumption.

3. Proposed DO-RTCCCII

To overcome the outlined drawbacks a novel architecture namely resistance tunable current controlled dual output current conveyor (DO-RTCCCII) is proposed in this section. Figure 3 shows the circuit symbol of proposed DO-RTCCCII and its implementation is depicted in figure 4. It uses basic DO-CCCII of figure 2 along with an externally driven digitally controlled resistor block. This new architecture will provide two flexibilities to the designer (i) setting of the resistance of X terminal using bias current and (ii) cancelling the offset in results using digitally controlled bits. In this new architecture, R_X can be altered as per the requirement of designer in the running condition which is not easy to implement in case of basic DO-CCCII.

The DO-RTCCCII circuit supports wide range of applications with better accuracy compared to DO-CCCII as the parasitic resistance is technology dependent while in DO-RTCCCII circuit the resistance at X terminal is controlled by digital bits and not purely parasitic resistance.

4. Implementation of proposed DO-RTCCCII

The physical implementation of externally driven digitally controlled resistor block in proposed dual output RTCCCII circuit is depicted in figure 5. In this block X represents external terminal while X_{IN} corresponds to internal node and b_i (i = 0, 1, 2…N) are externally driven digital bit which helps to tune the internal resistance (R_{dig}) of the X terminal. This block is therefore referred as resistor trimming block and is useful to cancel the undesired offset and achieve the outputs desired for applications. The poly resistor may be used in R_{dig} to minimize error in resistance due to variation of process, voltage and temperature (PVT).

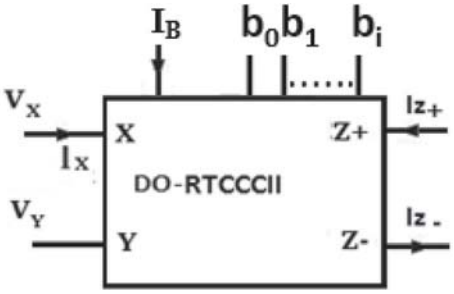

Figure 3. Block diagram of resistance tunable dual output CCCII.

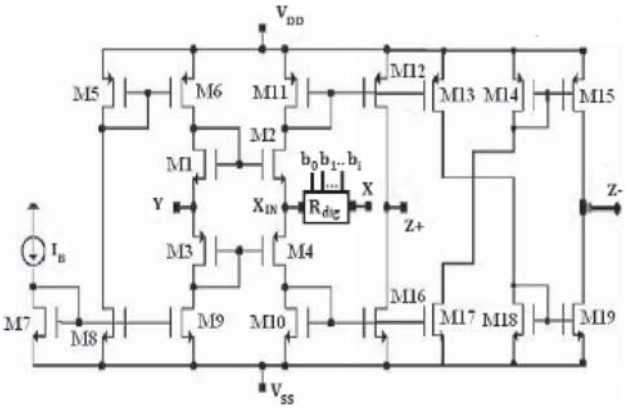

Figure 4. Resistance tunable dual output CCCII.

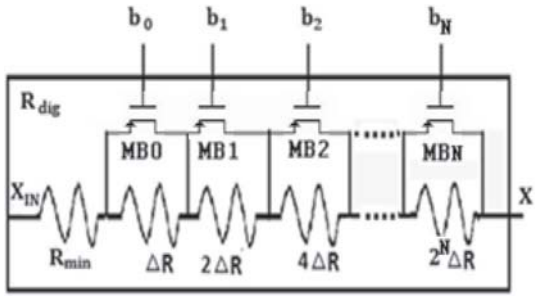

Figure 5. Externally driven digitally controlled resistor block.

Further, the direct interaction of source/drain terminal of MOS device (MBi, i = 0, 1 …N) with external node may damage the MOS device at the time of fluctuation so the resistor devices are used as R_{min} at the node X_{IN}. As the current may continuously flow from MOS switch so PMOS is used as switch to reduce the effect of HCI degradation

The terminal relationship between the voltage and current variables of the proposed DO-RTCCCII can be expressed by the following matrix,

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} R_{X_{dig}} & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (3)$$

where $R_{X_{dig}}$ denotes the resistance at X terminal which includes the variations due to bias current (i.e., intrinsic resistance) and due to setting of digital bits. The impedance at terminal X, $R_{X_{dig}}$ is given by

$$R_{X_{dig}} = R_{X_{IN}} + R_{dig} \quad (4)$$

where $R_{X_{IN}}$ is the intrinsic resistance at X_{IN} terminal which may be controlled by bias current I_B and is given by Equation (2) while R_{dig} corresponds to variable resistance controlled by digital bits. The value of R_{dig} is expressed as

$$R_{dig} = R_{min} + \Delta R \sum_{i=0}^{i=N-1} 2^i b_i \tag{5}$$

where ΔR corresponds to resistance step size of the resistance trimming block and is given by

$$\Delta R = \frac{(R_{max} - R_{min})}{(2N-1)} \tag{6}$$

where N = number of digital bits

$R_{\min}$ = minimum resistance of resistive trimming block with high logic at all digital bits

$R_{\max}$ = maximum resistance of resistive trimming block with high logic at all digital bits

For proper operation of the block, the ON resistance of the MOS device should be very low as compared to resistance of poly resistor ($R_{\min}$, ΔR and 2ΔR … 2iΔR) while the OFF resistance of MOS device should be very high as compared to poly resistor.

Thus the total resistance at terminal X of proposed DP-RTCCCII is given by

$$R_{X_{dig}} = \frac{1}{\sqrt{8\beta I_B}} + R_{dig} \tag{7}$$

where R_{dig} is defined in Equation (5).

5. Analysis and simulation results of DO-RTCCCII

The behavior of the proposed DO-RTCCCII is examined through simulations on ELDO simulator of mentor graphics using 28 nm CMOS bulk technology parameters of ST Microelectronics. Only three control bits are considered for present study. The results may, however, be extended for larger number of control bits. Typical process, voltage and temperature are considered for simulations. Other simulation settings are $_{DD}$ = (−)V_{SS} = 0.75 V and I_B = 5 µA.

Both DC and AC analysis are done to characterize proposed DO-RTCCCII. The DC voltage transfer characteristic from terminal to terminal of the proposed DO-RTCCCII is shown in the figure 6. It is clear that the voltage at terminal follows the voltage at terminal in the range of ± 100 mV. Figure 7 depicts current following action from X terminal to Z terminal. The variation of current at terminal current with reference to terminal current is 600 nA.

To illustrate the digital control of X terminal resistance, simulations have been carried out by varying b0, b1 and b2. The resistance of terminal X for different combinations of digital bits is depicted in figure 8. The current at input terminal X is varied and corresponding resistance variation with respect to control bits is graphically represented in figure 8. It may be noted that the resistance does not vary with input current and changes uniformly for successive

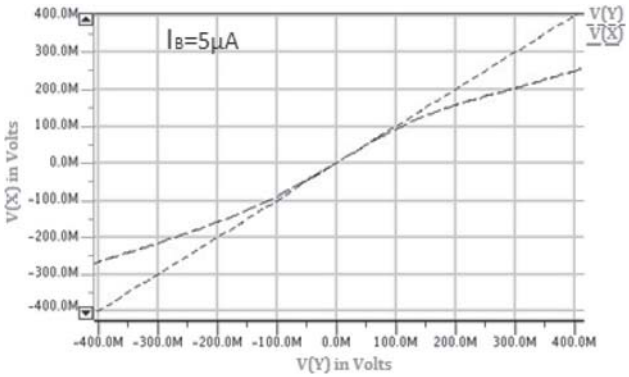

Figure 6. DC analysis for voltage transfer from terminal Y to X.

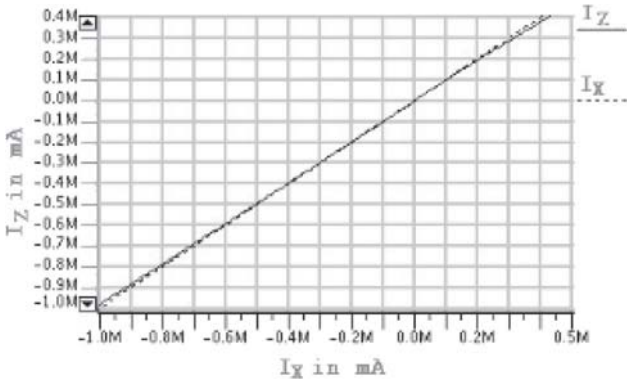

Figure 7. DC analysis for current transfer from terminal X to Z.

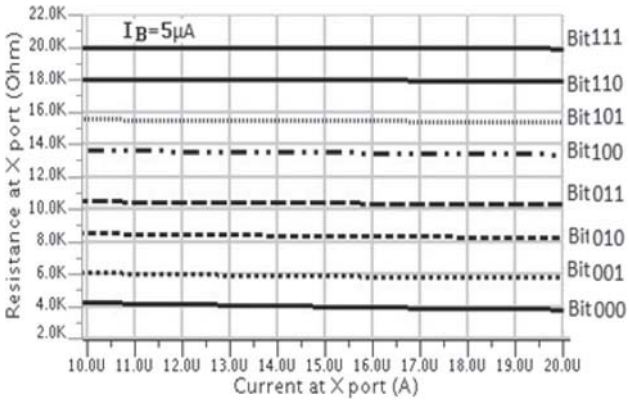

Figure 8. Resistance of X terminal verses (a) X terminal current.

change in control bits. The variation of resistance with control bits is linear as is clear from figure 9. Table 1 enlists the resistance at X port, digital bit combinations for proposed DO-RTCCCII and bias current for existing DO-CCCII and power dissipation for both. By observing the power dissipation values in table 1, it is clear there is

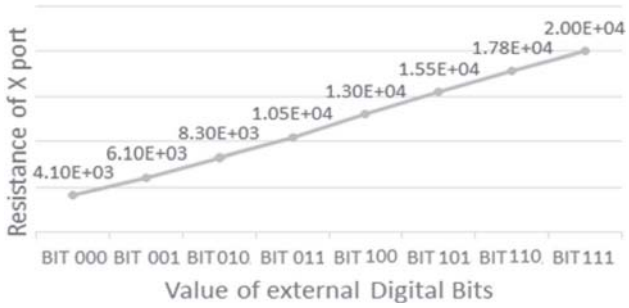

Figure 9. Resistance of X terminal verses different digital bits.

Table 1. Variation of resistance and band width for digital bits.

Proposed DO-RTCCCII			Existing DO-CCCII	
Bits	Resistance at X terminal [kΩ]	Power dissipation [μW]	Bias current [μA]	Power dissipation [μW]
000	4.1	51.5280	2.6	33.96
001	6.1	51.5280	2.86	36.579
010	8.3	51.5280	3.12	39.176
011	10.5	51.5280	3.38	41.751
100	13.0	51.5280	3.64	44.306
101	15.5	51.5280	3.9	46.839
110	17.8	51.5280	4.16	49.351
111	20.0	51.5280	4.5	51.84

variation in power dissipation for existing DO-CCCII while it remains constant for proposed DO-RTCCCII.

The simulations are also carried out to examine the operating region of various transistors in existing DO-CCCII circuit and table 2 summarizes the observations.

It is found that some of the MOS devices have changed their region of operation from sub-threshold region or saturation region into linear region by varying the bias current from lower value to higher values. In the proposed DO-RTCCCII circuit no transistor changed its region of operation in all combinations of digital bits so there will be minimum offset in results. It can therefore be inferred that while tuning the output waveform to achieve the desired frequency total power consumption variation is negligible in proposed DO-RTCCCII while in existing DO-CCCII block there is much variation in power consumption for the same range of variation of frequency and the MOS devices are also changing their region of operation. Thus it can be inferred that power consumption remains constant while tuning the frequency through externally driven digital bits. As these bits are externally driven the outputs can be reshaped while the system in running.

The AC simulations are carried out to find useful frequency range of proposed DO-RTCCCII operation. The plots for voltage and current transfers are depicted in figures 10 and 11 for bias current I_B = 5 μA and bit setting of

Table 2. Region of operation of MOS devices of DO-CCCII.

MOS device	I_B = 1 μA	I_B = 5 μA	I_B = 10 μA
M6	Saturation	Saturation	Linear
M11	Saturation	Saturation	Saturation
M1	Sub-threshold	Saturation	Saturation
M2	Sub-threshold	Saturation	Saturation
M3	Saturation	Saturation	Saturation
M4	Saturation	Saturation	Saturation
M9	Sub-threshold	Saturation	Linear
M10	Sub-threshold	Saturation	Saturation
M14	Saturation	Saturation	Saturation
M17	Saturation	Saturation	Saturation
M16	Saturation	Saturation	Saturation
M12	Saturation	Saturation	Saturation
M5	Saturation	Saturation	Saturation
M19	Sub-threshold	Saturation	Saturation
M17	Sub-threshold	Saturation	Saturation
M18	Sub-threshold	Saturation	Saturation
M13	Sub-threshold	Saturation	Saturation
M7	Sub-threshold	Saturation	Saturation
M8	Sub-threshold	Saturation	Saturation

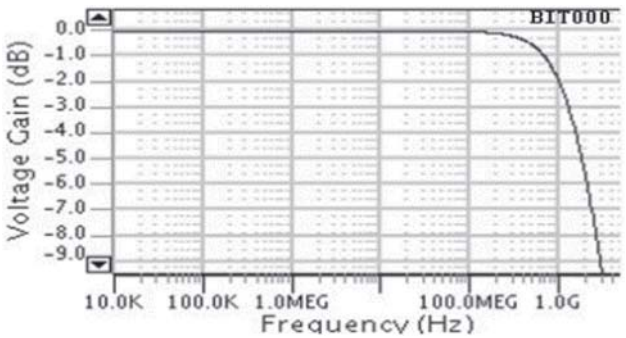

Figure 10. Frequency response for (a) voltage gain at X terminal.

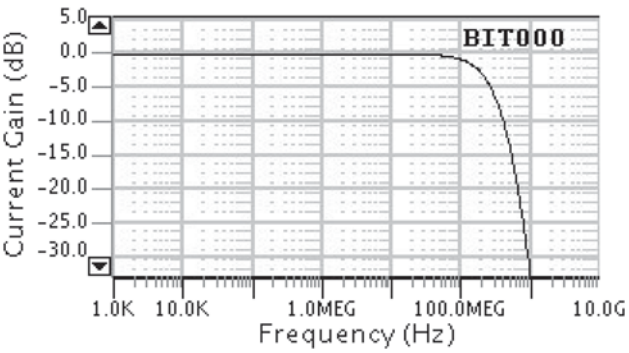

Figure 11. Frequency response for current gain at terminal Z.

Table 3. Characteristics of DO-RTCCCII with ± 0.75 V power supply for digital bits 000.

Parameter	Voltage follower		Current follower	
BIT	000	111	000	111
Gain	0.928	0.928	0.995	0.995
Input impedance	R_Y = 150 kΩ, C_Y = 11.7 fF	R_Y = 150 kΩ, C_Y = 11.7 fF	R_X = 4.1 kΩ, C_X = 40 fF	R_X = 4.1 kΩ, C_X = 40 fF
Offset current at Y	700 nA	700 nA	700 nA	700 nA
Output offset	1.3 mV	1.3 mV	600 nA	600 nA
Bandwidth	527 MHz	341 MHz	448 MHz	351 MHz
Output impedance	0.928	0.928	0.995	0.995

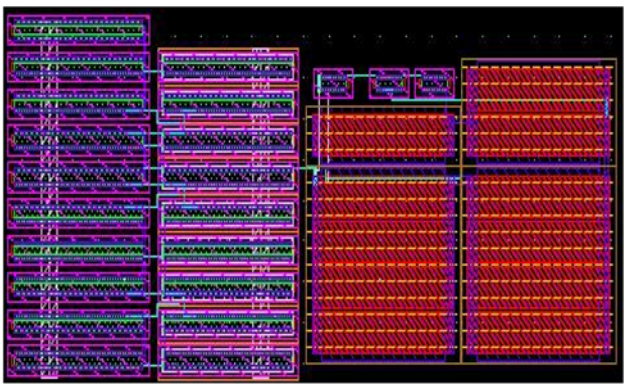

Figure 12. Layout view of proposed DO-RTCCCII.

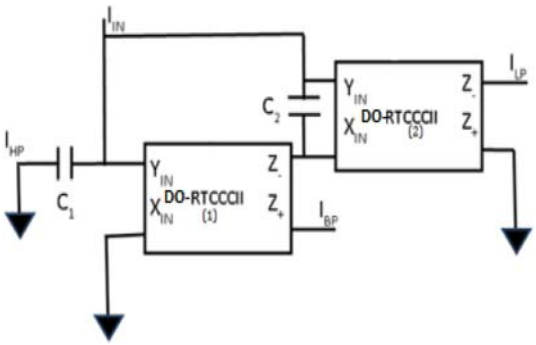

Figure 13. CM SITO current mode filter.

000. The corresponding 3 dB frequencies are found as 527 MHz and 448 MHz respectively. Table 3 enlists the summary of simulation results of AC analysis of proposed DO-RTCCCII as current follower as well as voltage follower circuit.

The circuit is laid out using Virtuoso (Cadence) tool with 28 nm CMOS technology and the corresponding layout is shown in figure 12. The area of the layout of the DO-RTCCCII is 206.565 μm^2. Simulations have been performed on post layout net list with ELDO (AMS) tool

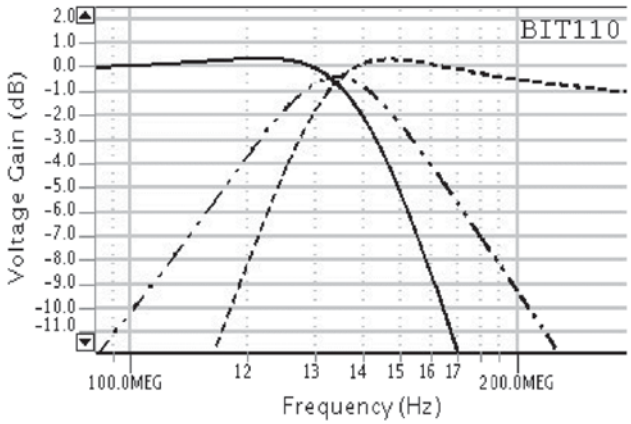

Figure 14. Frequency responses for low pass, high pass and band pass filters.

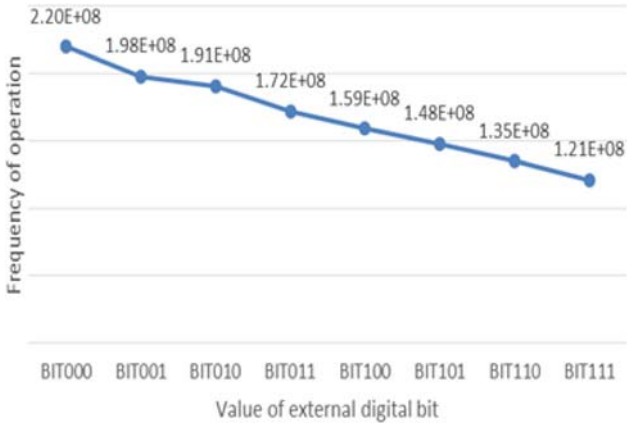

Figure 15. Frequency responses of filter.

of Mentor graphics. The layout is made by taking care of all analog design guidelines to reduce the post layout variations. The deviation between the results of pre layout net list and post layout net list is maximum 1%.

Table 4. 3 dB frequency of low pass and high pass filter.

Sl. no.	Digital programmable bits	3 dB frequency of low pass filter (MHz)	3 dB frequency of high pass filter (MHz)
1	000	220	209
2	001	198	185
3	010	191	173
4	011	172	154
5	100	159	143
6	101	148	132
7	110	135	122
8	111	121	112

6. Application as a universal filter

To illustrate the usability of proposed DO-RTCCCII, a CM single input three output (SITO) filter [31] presented in figure 13 has been implemented. Routine circuit analysis yields the following high pass, band pass and low pass transfer functions:

$$\frac{I_{HP}}{I_{in}} = \frac{-s^2}{s^2 + \frac{s}{R_{x_{dig1}} C_1} + \frac{1}{R_{x_{dig1}} R_{x_{dig2}} C_1 C_2}} \tag{8}$$

$$\frac{I_{LP}}{I_{in}} = \frac{-\frac{1}{R_{x_{dig1}} R_{x_{dig}} C_1 C_2}}{s^2 + \frac{s}{R_{x_{dig1}} C_1} + \frac{1}{R_{x_{dig1}} R_{x_{dig}} C_1 C_2}} \tag{9}$$

$$\frac{I_{BP}}{I_{in}} = \frac{\frac{s}{R_{x_{dig1}} C_1}}{s^2 + \frac{s}{R_{x_{dig1}} C_1} + \frac{1}{R_{x_{dig1}} R_{x_{dig}} C_1 C_2}} \tag{10}$$

Combining high pass and low pass transfer functions, a notch transfer function can be obtained an all pass transfer function is obtained when all three transfer functions (LP, HP, and BP) are pooled together.

By comparing the denominator of filter response with standard second order transfer function, the pole frequency (ω_0), the bandwidth (ω_0/Q) and the Quality factor (Q) are obtained as:

$$\omega_0 = \sqrt{\frac{1}{R_{x_{dig1}} R_{x_{dig2}} C_1 C_2}} \tag{11}$$

$$\frac{\omega_0}{Q} = \frac{1}{R_{x_{dig1}} C_1} \tag{12}$$

$$Q = \sqrt{\frac{R_{x_{dig1}} C_1}{R_{x_{dig2}} C_2}} \tag{13}$$

Equations (11) and (12) clearly indicate that the operating frequency as well as band width can be adjusted by the digital programmable bits of the respective DO-RTCCCII. In our universal filter implementation the values of capacitors are 50 fF while bias current has been fixed at 5 μA.

Figures 14 and 15 are the frequency responses for low pass and high pass filters respectively. Table 4 shows the 3 dB frequency of the low pass and high pass response of filter by trimming the digital bits. The linear frequency response of the different kind of filter shown in figures 14 and 15 indicates good control of bits on outputs for specific frequency of operation. Using these digital bits for trimming the R_{Xdig} parameter the circuit frequency can be directly aligned with the frequency required by the actual application.

7. Conclusion

A CMOS implementation of DO-RTCCCII circuit is presented in 28 nm CMOS technology. The design is based on a ± 0.75 V DC supply and simulated using Virtuoso Cadence tool, achieves good linearity, accuracy, low power dissipation and high bandwidth. As an application a current mode second order universal filter (Low Pass, High Pass and Band Pass) is simulated using two DO-RTCCCII and two capacitors. This Current mode block uses externally driven digital to tune our outputs accurately in between the process application. All Simulations have been performed on post layout net list with simulator eldo (AMS) tool of Mentor graphics. It is found that the deviation of results from pre layout net list and post layout net list is maximum 1%.

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