Sādhanā (2020)45:184
https://doi.org/10.1007/s12046-020-01421-2

Resolution-independent fully differential SCI-based SAR ADC architecture using six unit capacitors

KALPANA G BHAT*, T LAXMINIDHI and M S BHAT

Department of Electronics and Communication Engineering, National Institute of Technology Karnataka, Surathkal 575025, India
e-mail: kalpanabhat_ec@nitk.ac.in; laxminidhi_t@yahoo.com; msbhat_99@yahoo.com

MS received 8 June 2019; revised 19 March 2020; accepted 3 April 2020

Abstract. A resolution-independent successive approximation register (SAR) analog to digital converter (ADC) architecture based on a switched capacitor integrator is presented. Digital to analog converter (DAC) architecture uses charge sharing and integration principle for reference generation, using only six unit capacitors for a fully differential version. A 10-bit, 1.8-V and 0.9-MS/s SAR ADC is designed in 180-nm CMOS process. ADC architecture is area efficient when compared with SAR ADC with a binary weighted capacitor array DAC. The architecture is largely parasitic insensitive, also programmable resolution is possible with no hardware overhead.

Keywords. ADC; SAR; SC; area-efficient SAR; non-binary; OTA.

1. Introduction

Modern instrumentation systems and data acquisition systems demand low to medium resolution, medium speed analogue to digital converters (ADCs). Since most of these systems are portable, there is a stringent requirement on power and area parameter in the ADC specification. Even though the traditional successive approximation register (SAR) ADCs are popular in these applications because of simple structure and few analog blocks, they consume large chip area. The conventional SAR ADC uses binary weighted capacitor charge redistribution digital to analog converter (DAC) [1, 2]. Two major limitations of traditional capacitor charge redistribution DACs are conversion speed and bulky capacitive array. Speed of conversion is limited because of large MSB capacitor. DAC capacitive array used in this architecture becomes very bulky. There are a few novel approaches, found in the literature, proposed to improve the speed of SAR ADCs [3, 4]. A few area-efficient DAC architectures for SAR ADCs have also been proposed [5–7]. Some of these ADCs outperform the rest in terms of figure of merit (FOM) however, area efficiency (AE) parameter is degraded because of the type of DAC architecture used. SAR ADCs in [8, 9] incorporate variability of resolution into a conventional charge redistribution ADC to adapt to multiple signals demanding different resolutions for applications such as bio-medical signal acquisition systems.

This work proposes SAR architecture that uses a few unit size capacitors (non-binary) in the DAC instead of binary weighted capacitor array. In conventional SAR ADC with binary weighted capacitor array DAC, the minimum capacitor size is limited by parasitics and mismatch. Therefore, the total capacitance can be significantly large with increase in ADC resolution. If the total capacitance is restricted, the error due to capacitor mismatch can be quite significant as resolution increases. On the other hand, in ADC with only fixed number of unit capacitors in the DAC irrespective of resolution of ADC, mismatch errors are greatly reduced. Also, there is no need of explicit sample and hold circuit as it can be absorbed into the SC integrator. An SCI-based SAR ADC architecture using 2 unit capacitors on each half of differential OTA is proposed in this work, which requires only a bare minimum control logic apart from the registers required to store the data bits. The design objective is an area-efficient non-binary weighted SAR ADC, with reasonably low power, for data acquisition systems like in [8, 9].

2. Proposed SAR architecture

Figure 1 illustrates the proposed data converter. Pairs of unit capacitors C_1, C_2 and C_3, C_4 generate positive reference voltage V_{top} and negative reference voltage V_{bot}, respectively, using the charge sharing technique, required to decide on the bit under consideration in every clock cycle. The capacitor C_{int} (also a unit capacitor) integrates

*For correspondence
Published online: 20 July 2020

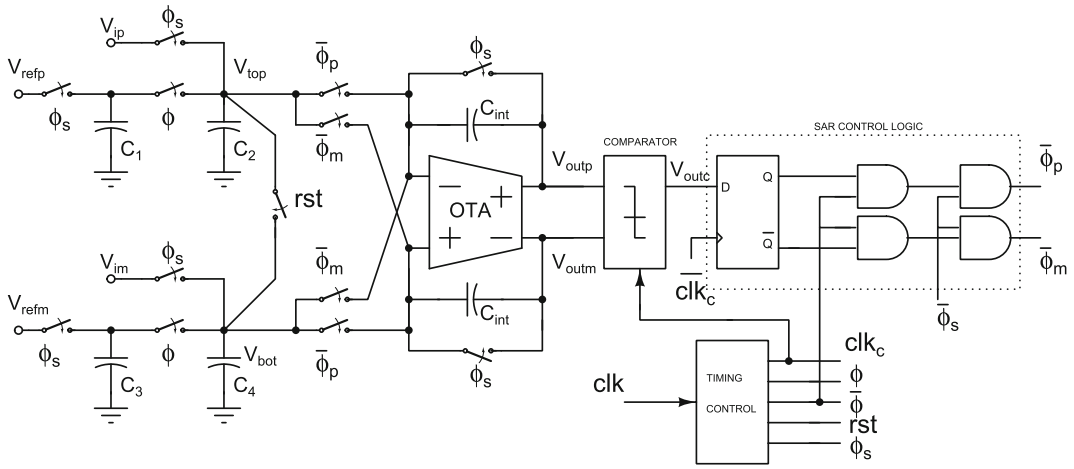

Figure 1. Schematic of proposed SCI-based ADC.

the charges in every cycle depending on the bit decided in the previous cycle. The comparator compares the integrated voltage and makes a decision on the bit under consideration. The SAR control logic generates the control signal for charge integration on C_{int}. The timing and control block generates the necessary timing signals for SCI block and SAR control logic block according to the successive approximation algorithm. The timing signals generated by this block are shown in Figure 2.

The conversion cycle starts with sampling and storing the differential input on the integrating capacitors C_{int}. In the subsequent cycles the binary weighted reference charges (generated by the charge sharing process) are transferred to C_{int} with a polarity so as to continuously reduce the charge on C_{int}. The conversion stops when all the bits are resolved. A detailed operation of the proposed ADC can be found in [10].

The charge sharing process is made parasite insensitive by matching parasitics at the charge sharing nodes by introducing dummy switches wherever necessary. Major building blocks of proposed ADC include an OTA and a comparator. A suitable comparator and fully differential OTA with common mode feedback circuit are designed to support 10-bit ADC operation at sampling rate of 0.9 MS/s.

3. Simulation results

The proposed fully differential SCI-based SAR ADC has been designed in UMC 180-nm CMOS process to operate on 1.8 V supply. The ADC has input voltage swing of 1 V peak to peak with a common mode voltage of 0.9 V. The ADC layout is shown in Figure 3 and area occupied is 0.05 mm^2 (267 μm $\times$ 188 μm).

The simulation results show that ADC achieved a conversion speed of 0.9 MS/s in 10-bit resolution. The total number of capacitors used in the DAC is 6 C where C is a unit capacitor of value 300 fF. The unit capacitor of this order is used to limit the thermal noise at the output of integrator. Compared with the conventional charge redistribution DAC architecture, which requires 1024 C for 10-

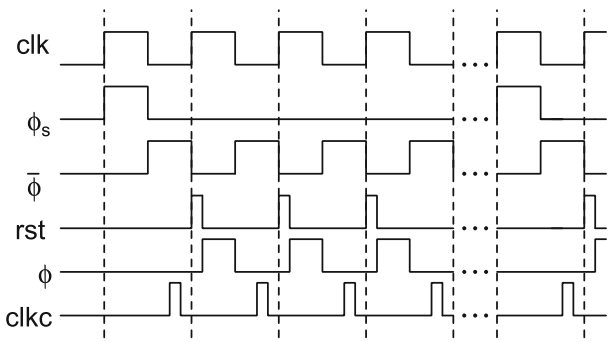

Figure 2. SAR timing control.

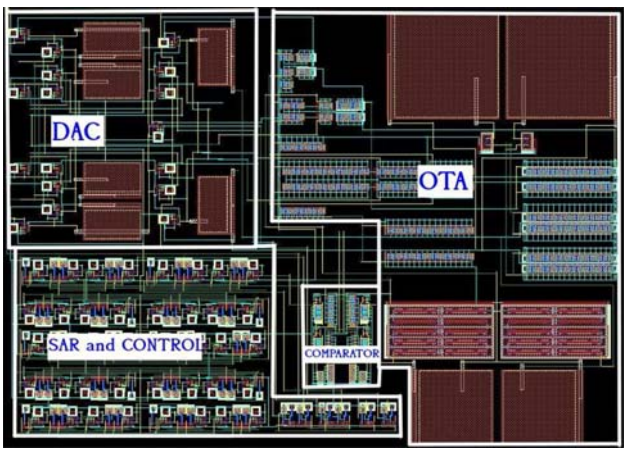

Figure 3. Layout diagram of SCI ADC.

bit resolution, this DAC offers large savings in terms of area, headroom on capacitor mismatch and parasitic requirements. On the other hand, in the conventional SAR ADC, if the total capacitance is taken to be 1.8 pF (i.e. 300 fF $\times$ 6), the unit capacitor required for a 10-bit operation will amount to 1.78 fF. Note that the parasitics at a given node, in the capacitor array, itself can be comparable or more than this value.

Figure 4 illustrates how the output of the OTA converges towards zero during the conversion cycle. The plot is given for an analog input corresponding to an output code of 799. The DNL and INL of the ADC at 0.9-MS/s sampling speed are found to be within 0.3 LSB/–0.6 LSB and 0.7 LSB/–0.1 LSB, respectively.

The output spectrum of the ADC for an input sine wave at full-scale and 450.9 kHz (at Nyquist) is shown in Figure 5. The ADC offered an SNDR of 59.02 dB (ENOB = 9.5).

The SNDR and SFDR performance of the proposed ADC for input in the range DC to Nyquist frequency at 0.9 MS/s is shown in Figure 6. The SNDR is found to be minimum at Nyquist rate. The ENOB is found to vary from 9.5 at Nyquist to 9.9 at near DC.

The total power consumed by the ADC is 734 μW, at 1.8 V supply. The major share of power is taken by OTA, which is 568 μW. The comparator consumes 154 μW and digital circuit consumes 12 μW. However, with a careful design, the OTA power can be reduced further. To verify ADC performance against mismatches in OTA, Monte Carlo simulations of 100 runs are carried on the extracted net list. The mean and sigma values of SNDR are 58.18 and 1.7 dB, respectively.

ADC performance for various process corners is given in Table 1. The ENOB offered by the ADC is found to be 9 or above in all cases.

SNDR performance of the ADC against the supply voltage variation of $\pm$10% over the nominal and temperature variation in the range 0–70°C is shown in Tables 2 and 3, respectively. The ENOB performance is found to be 9 or better.

The proposed SCI-based SAR ADC performance is compared with those of some of the non-binary weighted

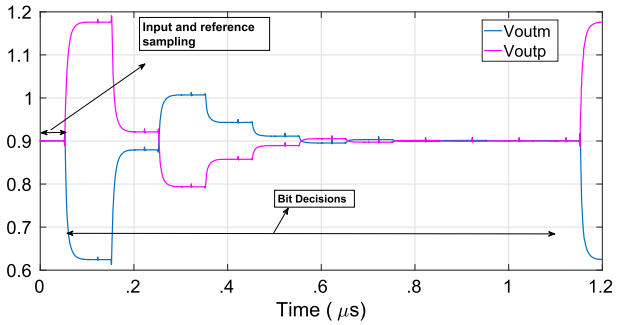

Figure 4. OTA output for analog input corresponding to output code of 799.

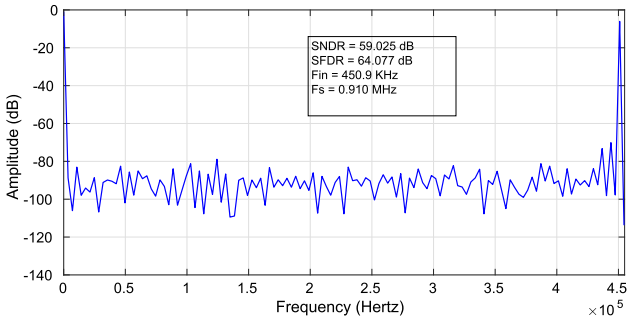

Figure 5. FFT spectrum of 10 b ADC for an input frequency of 450.9 kHz.

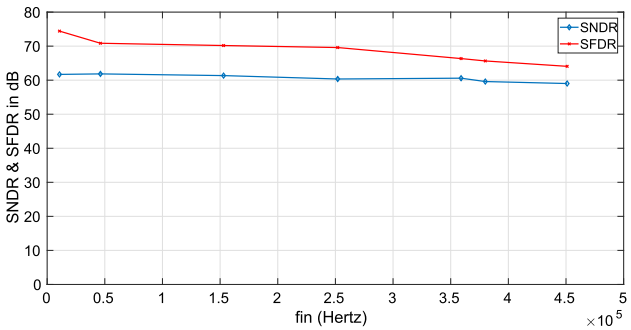

Figure 6. SNDR/SFDR as a function of input frequency @0.9 MHz.

Table 1. SNDR in dB of ADC over different process corners.

SNDR	tt	ff	ss	snfp	fnsp
@DC	61.7	58.15	58.68	59.78	60.2
@Nyq.	59.02	57.22	57.1	58.59	55.75

Table 2. Performance of ADC at different supply voltages.

Parameter	1.62 V	1.8 V	1.98 V
SNDR (dB)@DC	60.29	61.7	59.78
SNDR (dB)@Nyquist	55.24	59.02	58.02

Table 3. Performance of ADC at different temperatures.

Parameter	0°C	27 °C	70 °C
SNDR (dB)@DC	58.86	61.7	59.95
SNDR (dB)@Nyquist	57.83	59.02	58.79

SAR ADCs in the literature and is listed in Table 4. The ADCs are compared using two metrics: FOM and AE. The FOM is computed using (1) [6] and AE is computed using (2) [11]:

Table 4. Comparison with available non-binary SAR ADCs in the literature.

Ref.	Tech. (μm)	V_{dd} (V)	F_s (MS/s)	ENOB (@fin)	P_{diss} (μW)	FOM (fJ/conv.)	Area (mm^2)	AE (μm^2/code)	C_u (fF)	C_{tot} (pF)
[12][2]	0.18	1.5	0.128	12.81	74.2	81.2	0.25	480.08	4000	24
[7][1]	0.18	5	0.1	8.63	2035	256000	0.316	797.62	2000	13
[13][2]	0.045	1.25	1000	6.48	7200	80	0.016	1792.44	5	0.6
This work [1]	*0.18*	*1.8*	*0.91*	*9.5*	*734*	*924.7*	*0.05*	*69.32*	*300*	*1.8*

[1] Simulation results.

[2] Measured results

$$FOM = \frac{P_{diss}}{2^{ENOB} \times 2f_{in}} \quad (1)$$

where P_{diss} is the power dissipation, f_{in} is the input frequency and ENOB is the effective number of bits. It can be seen that the proposed SAR ADC is area efficient.

$$AE = \frac{Area}{2^{ENOB}}. \quad (2)$$

4. Conclusion

An architecture for non-binary capacitor SAR ADC is proposed. The proposed architecture has been validated by designing a 10-bit non-binary weighted SAR ADC in 180-nm CMOS process to operate on 1.8 V supply. The results proved that the ADC is area efficient and it offers ENOB in excess of 9 across the input frequency range, process, voltage and temperature.

Acknowledgements

Authors would like to thank Ministry of Electronics and Information Technology (MeitY), Government of India, for providing EDA tools through SMDP-VLSI Project.

References

[1] McCreary J L and Gray P R 1975 All-MOS charge redistribution analog-to-digital conversion techniques—part I. *IEEE Journal of Solid-State Circuits* 10: 371–379

[2] Sauerbrey J, Schmitt-Landsiedel D and Thewes R 2003 A 0.5-V 1-μW successive approximation ADC. *IEEE Journal of Solid-State Circuits* 10: 1261–1265

[3] Sugiyama N, Noto H, Nishigami Y, Oda R and Waho T 2010 A low-power successive approximation analog-to-digital converter based on 2-bit/step comparison. In: *Proceedings of the 40th IEEE International Symposium on Multiple-Valued Logic (ISMVL)*, pp. 325–330

[4] Wei H, Chan C H, Chio U, Sin S W, Seng-Pan U, Martins R and Maloberti F 2011 A 0.024 mm^2 8 b 400 MS/s SAR ADC with 2 b/cycle and resistive DAC in 65 nm CMOS. In: *Proceedings of the 2018 IEEE International Solid-State Circuits Conference*, pp. 188–190

[5] Ginsburg B P and Chandrakasan A P 2007 500-MS/s 5-bit ADC in 65-nm CMOS with split capacitor array DAC. *IEEE Journal of Solid-State Circuits* 42: 739–747

[6] Kamalinejad P, Mirabbasi S and Leung V 2011 An ultra-low-power SAR ADC with an area-efficient DAC architecture. In: *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 13–16

[7] Yurin J, Seongik C and Minwoong L 2017 Small area DAC using SC integrator for SAR ADC. *WSEAS Transactions on Circuits and Systems*, 16: 74–78

[8] Chaturvedi V, Anand T and Amrutur B 2013 An 8-to-1 bit 1-MS/s SAR ADC with VGA and integrated data compression for neural recording. In: *Proceedings of the 18th International Symposium on VLSI Design and Test* , vol. 21, pp. 2034–2044

[9] Yip M and Chandrakasan A 2013 A resolution-reconfigurable 5-to-10-bit 0.4-to-1-V power scalable SAR ADC for sensor applications. *IEEE Journal of Solid-State Circuits* 48: 1453–1464

[10] Bhat K G, Laxminidhi T and Bhat M S 2019 A compact 10-bit nonbinary weighted switched capacitor integrator based SAR ADC architecture. In: *Proceedings of the IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia)*, pp. 1–4

[11] Xu R, Liu B and Yuan J 2012 Digitally calibrated 768-kS/s 10-b minimum-size SAR ADC array with dithering. *IEEE Journal of Solid-State Circuits* 47(9): 2129–2140

[12] Shi L, Zhang Y, Wang Y, Kareppagoudr M, Sadollahi M and Temes G C 2018 A 13 b-ENOB noise shaping SAR ADC with a two-capacitor DAC. In: *Proceedings of the 2018 61st IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 153–156

[13] Hong H K, Kim W, Kang H W, Park S J, Choi M, Park H and Ryu S T 2015 A decision-error-tolerant 45 nm CMOS 7 b 1 GS/s nonbinary 2 b/cycle SAR ADC. *IEEE Journal of Solid-State Circuits* 50(2): 543–555