Sādhanā (2020)45:181
https://doi.org/10.1007/s12046-020-01407-0

Design of optimal high-frequency CMOS VCOs for automotive application

REKHA YADAV[1,*], PAWAN KUMAR DAHIYA[1] and RAJESH MISHRA[2]

[1]ECE Department, DCR University of Science and Technology, Murthal, India
[2]ECE Department, GBU, Greater Noida, India
e-mail: rekha_7r@yahoo.co.in; pawan.dahiya@gmail.com; rajeshmishra25@rediffmail.com

MS received 21 July 2019; revised 23 February 2020; accepted 2 March 2020

Abstract. In this paper, a design methodology of Voltage-Controlled Oscillator (VCO) for long-range automotive RAdio Detection And Ranging (RADAR) is proposed and simulation analysis is carried out over Virtuoso SpectreRF software on Cadence tool. The frequency ranges of the mm-wave CMOS current-starved ring and LC VCOs for 45-nm CMOS technology are 24 and 76 GHz, respectively. The ring VCO at 25 GHz oscillation frequency demonstrates 2.06% tuning range, phase noise −71.61 dBc/Hz at 1-MHz offset, 3.43 mW power dissipation and layout area of $20 \times 20\,\mu m^2$ whereas cross-coupled LC VCO achieves an oscillation frequency of 76.25 GHz for frequency tuning range of 0.65%, a phase noise of −92.44 dBc/Hz at 1-MHz offset, 8.59 mW power dissipation and $320 \times 320\,\mu m^2$ layout area. The proposed design of efficient VCOs shows an excellent performance for long-range automotive RADAR.

Keywords. CMOS; frequency-modulated continuous wave; periodic steady state; phase noise; RADAR; voltage-controlled oscillator.

1. Introduction

An emerging technology of automotive safety systems, called Advanced Driver Assistance System (ADAS), has been currently introduced, which uses automotive radar sensors for providing safer and more secure driving environment. There are various types of automotive radar sensors used for automotive collision detection, such as short-range radars (range >10 m and 24 GHz frequency band) for parking assistance, mid-range radars (range 10–40 m and 77–79 GHz frequency band) for avoiding side-crash and the long-range radars (range >50 m and 76 GHz frequency band) for collision detection and avoidance systems. The frequency-modulated continuous wave (FMCW) radars are commonly used to detect collision over long range [1]. The basic block diagram of the FMCW radar is shown in figure 1. The Voltage-Controlled Oscillator (VCO) is one of the key components and has its major impact on the automotive radar performance. There are basically two types of VCOs that have been chosen for designing as shown in figure 2.

CMOS-based design ring and LC-tank VCOs are two typical choices used in automotive radar systems. LC VCOs have outstanding jitter and phase noise (PN) performance at high frequency compared with ring VCOs. However, LC VCOs have smaller tuning range and larger layout area than ring VCCOs. For the reasons of cost-effectiveness and design simplicity, ring VCOs are considered first to decide whether they can meet the performance requirements.

This paper discusses the design of ring VCO and LC VCO. In section 2, a design methodology is described for CMOS-based ring and CMOS cross-coupled LC VCOs. It also presents the optimized design of CMOS ring VCO for short-range automotive application operating at nearly 25 GHz frequency. For long-range automotive application, an CMOS cross-coupled VCO model is designed, which is operated at 76–77 GHz frequency. In section 3, both the layout and VCO comparative performance results are discussed, which includes DC, transient, noise analysis, etc. It analyses oscillating waveform at output terminal and frequency control through control voltage in transient analysis. It also discusses layout area, power dissipation and PN on Cadence environment. Finally, these comparative results are concluded in section 4.

2. Design methodology for VCO

2.1 *Ring VCO*

A ring oscillator basically consists of multiple number of gain stages within a loop. This paper considered three-stage ring oscillator architecture. Ring VCO is compatible with digital CMOS technology and occupies small chip area

*For correspondence
Published online: 15 July 2020

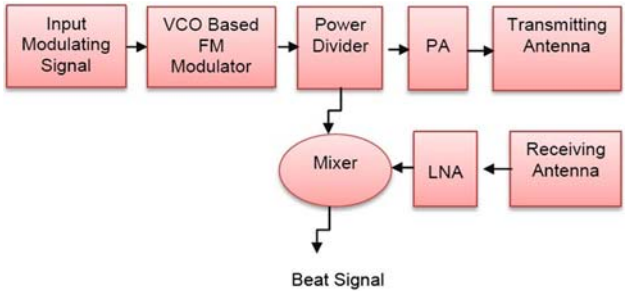

Figure 1. Basic block diagram of FMCW radar.

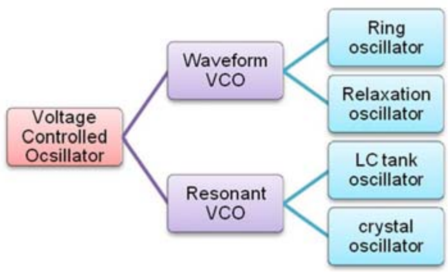

Figure 2. Various types of VCOs.

because it does not have high-frequency components. The PN for ring oscillator is usually larger than that of resonator-based oscillators. The ring oscillator consists of a number of inverters and its frequency depends on total switching delay. If an odd number of inverters are connected, a natural oscillation is obtained with a period that corresponds approximately to the number of fundamental delays per gate. The design methodology for this ring VCO is summarized as follows.

The oscillation frequency of ring oscillator is calculated as

$$f_{osc} = 1/(2NT_d) \tag{1}$$

where N is the number of stages in the ring oscillator and T_d is delay time of each stage. In this equation, the oscillation frequency depends only on stages delay and it is calculated with ideal input and typical output for single-stage inverter [2]. This delay time in each stage determines the input to output propagation delay during input transition from high to low (low to high) and low to high (high to low) transition of the output. For symmetrical inverter stages, average propagation delay is

$$T_d = (T_{PHL} + T_{PLH})/2 \tag{2}$$

and

$$T_{PHL} = t_2 + t_1. \tag{3}$$

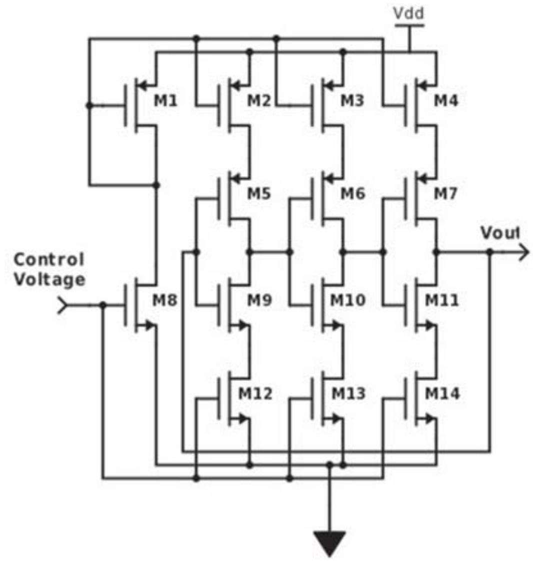

Figure 3. Schematic of ring VCO with an odd number of current-starved inverter stages.

Evaluate t_1 and t_2 when mosfet operates in linear and saturation regions. Hence

$$T_{PHL} = \frac{C_{Load}}{\beta_n(Vdd - V_{tn})}\left[\frac{2V_{tn}}{Vdd - V_{tn}} + \ln\left(\frac{4(Vdd - V_{tn})}{Vdd} - 1\right)\right] \tag{4}$$

and RC circuit delay is

$$T_{dRC} \cong 0.69RC \tag{5}$$

which is negligible. Hence, total delay of basic inverter per stage is $T_d \cong T_{PHL}$.

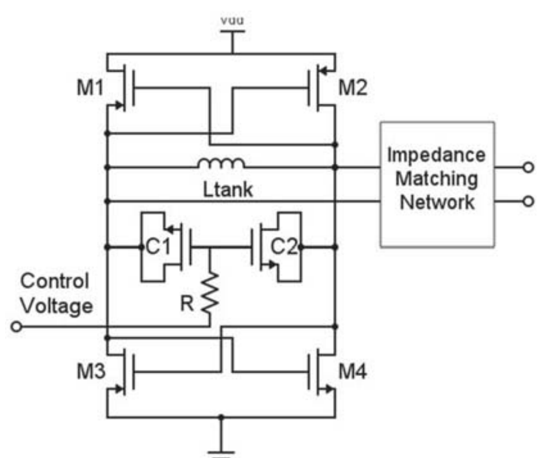

Figure 4. Schematic of CMOS differential cross-coupled LC VCO.

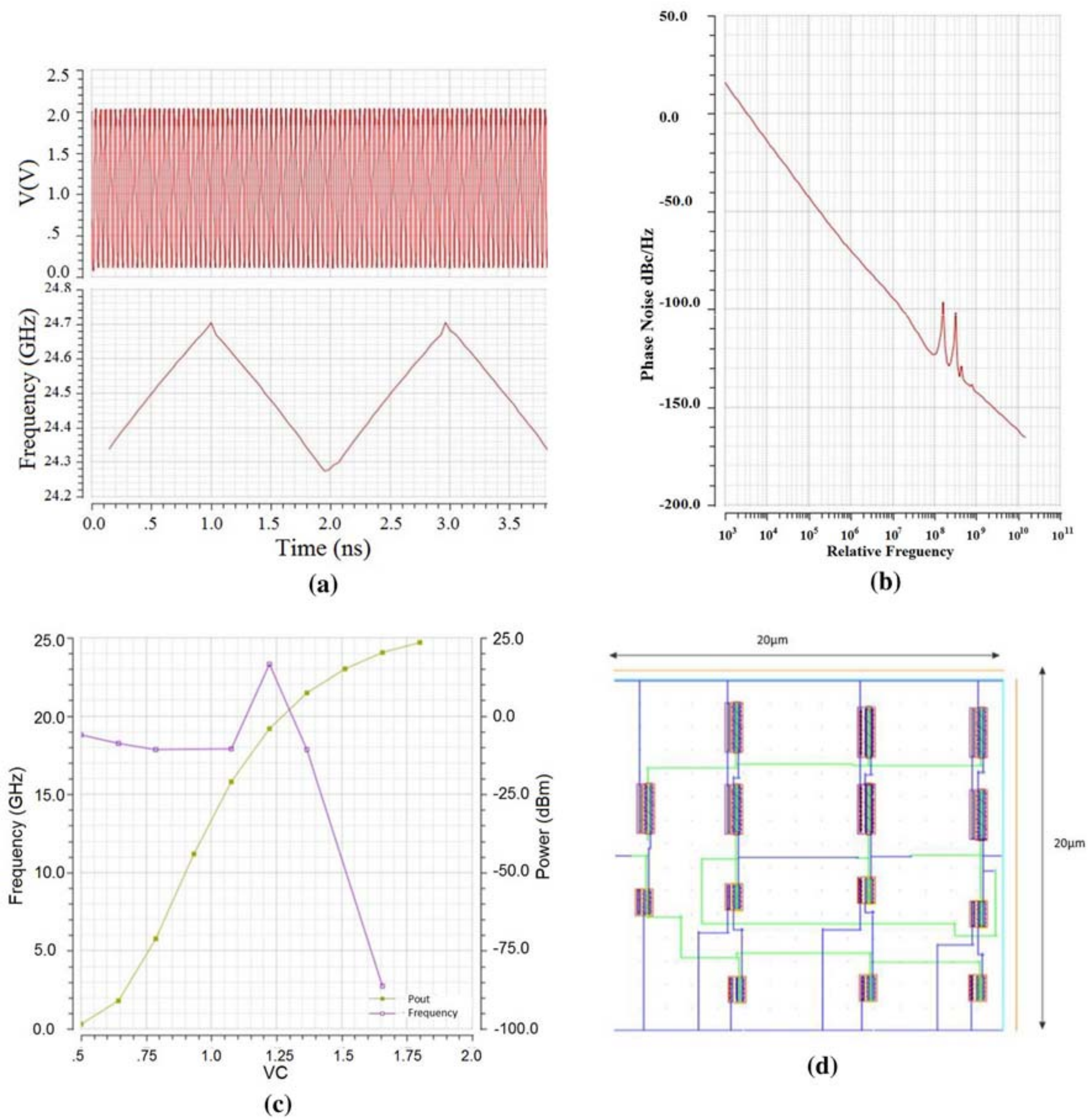

Figure 5. CMOS ring VCO simulation analysis: (**a**) three-stage VCO transient analysis, (**b**) phase noise with respect to relative frequency, (**c**) output power and tuning frequency characteristics as a function of control voltage and (**d**) chip layout area of CMOS ring VCO.

Similarly, for the current-starved ring VCO shown in figure 3, calculated total delay of inverter per stage is [2]

$$T_d = \frac{4C_{Load}V_{tn}}{\beta_n(V_{gs} - V_{tn})^2} + \frac{C_{Load}}{\beta_n(Vdd - V_{tn})}\ln\left(\frac{2(Vdd - V_{tn})}{Vdd} - 1\right). \quad (6)$$

Power dissipation of ring VCO is

$$P_{Ring} \cong 2\eta N q_{max} Vdd f_{osc} \quad (7)$$

where q_{max} is maximum charge at each stage.

2.2 *CMOS cross-coupled LC VCOs*

A schematic of the 76–77 GHz differential CMOS cross-coupled VCO is presented in figure 4. The design methodology for this CMOS differential cross-coupled LC VCO is summarized as follows:

1. Choose L_{tank} parameter according to the design requirement; choose the largest L_{tank} value for less power dissipation and narrow tuning range, and the smallest L_{tank} value for wide tuning range and excellent PN.
2. Calculate C_{eq} for oscillation frequency

$$f_{osc} = \frac{1}{2\Pi\sqrt{(L_{tank}C_{eq})}}. \quad (8)$$

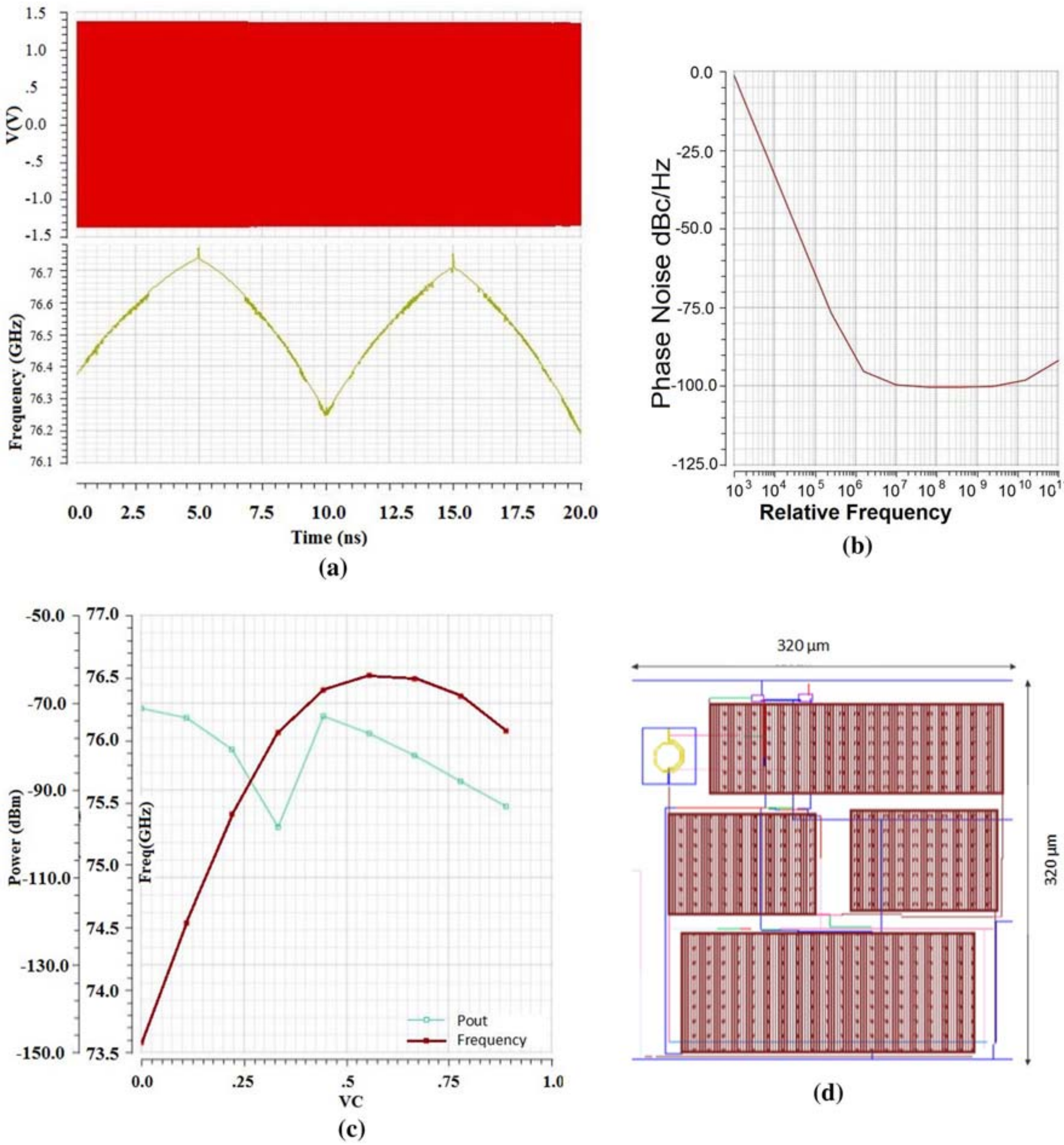

Figure 6. CMOS differential cross-coupled LC-VCO analysis: (**a**) differential output waveforms, (**b**) phase noise analysis, (**c**) output power and tuning frequency characteristics as a function of control voltage and (**d**) chip layout area of cross-coupled LC VCO.

C_{eq} is dependent on variable capacitor and parasitic capacitance of mosfet.

3. Finally, determine each transistor size of oscillator from the Barkhausen oscillation condition, which is total gain ≥ 1, i.e. $(G_m R_p)^2 \geq 1$. Power dissipation for differential LC cross-coupled oscillator is given by the equation [4–6]

$$P_{LC} = \frac{2R_p}{L_{tank}^2 \omega_{osc}^2 V_{peak}^2} \tag{9}$$

where V_{peak} is the peak voltage across inductor and R_p is AC equivalent resistance across the inductor.

3. Results and discussion

To validate this mathematical analysis, CMOS ring and LC cross-coupled VCO have been designed in CMOS 45-nm technology. Specification details of the proposed ring and LC-VCO parameters used for designing are load MOS capacitor (19 fF), load inductor (117 pH), supply voltage (1.5 V) and the size of transistors (nMOS 1 µm × 45 nm, pMOS 2 µm × 45 nm). Initially, a current-starved ring VCO is simulated over the tuning range of 24–25 GHz frequency. Transient analysis is carried out to prove the VCO functionality as shown in figure 5a and calculate its settling time and output frequency. PN analysis is

Table 1. Comparative analysis of the proposed two VCOs with previous work.

Work	Technology (nm)	*Vdd* (V)	Control voltage range for tuning (V)	f_{osc} (GHz)	Tuning range (%)	Phase noise (dBc/Hz)	Total power dissipation (mW)	Max. P_{out}	Layout area (μm × μm)
Tang *et al.* [7]	180	1.5	0.9–1.8	76	2.6	−84.3 @ 10 MHz	10.5	−13.2 dBm	–
Trivedi *et al.* [8]	65	1	0–3.5	77	14.5	−88 @ 1 MHz	190	6.2 dBm	–
Li *et al.* [9]	90	1.5	0–1.5	33	20.2	−103.4 @ 1 MHz	DC 2.9	−12.7 dBm	530 × 470
This work Ring VCO	45	2	1.7–1.8	24.2	2.06	−71.61 @ 1 MHz −94 @ 10 MHz	3.43	29 dBm, 0.8 W	20 × 20 This work
LC VCO	45	1.5	0.3–0.45	76.25	0.65	−92.44 @ 1 MHz −99.4 @ 10 MHz	8.59	19 dBm	320 × 320

conducted at a particular frequency offset shown in figure 5b; it continuously decreases with increase in frequency due to flicker noise components. Here PN is noise introduced into an oscillator by the active transistors and passive elements, and it disturbs both the output signal amplitude and frequency. PN is a random frequency deviation, which can also be viewed as a random deviation of the oscillator waveform at the zero-crossing points.

Ring VCO output tuning characteristics are shown in figure 5c, which implies that its output power and frequency are functions of an input control voltage. The layout of this ring VCO is optimally designed for the 45-nm CMOS process in Cadence Virtuoso environment, as shown in figure 5d. An ideal oscillator is a circuit whose output relative frequency changes linearly with its control voltage (V_{ctrl}):

$$f_{osc} = f_0 + K_{vco} V_{ctrl} \tag{10}$$

where f_0 is the oscillation frequency at $V_{ctrl} = 0$ and K_{vco} is the sensitivity or gain of the circuit. The obtained frequency range, $f_2 - f_1$, is called the frequency tuning range.

The schematic of CMOS cross-coupled LC VCO is designed for tuning frequency range 76.2–76.7 GHz as requirement of a long-range radar system for automotive application. The oscillation frequency of an LC VCO depends only on the inductor and capacitor values, which can be varied to tune the oscillation frequency. As illustrated in figure 6 the 76-GHz CMOS cross-coupled LC VCO can be tuned between 76 and 77 GHz, with a very small PN, i.e. −92.44 dBc/Hz at 1 MHz offset and −99.4dBc/Hz at 10 MHz frequency offset for 1.5 V power supply. The layout of this LC-VCO is designed for the 45-nm CMOS process in Cadence Virtuoso environment, as shown in figure 6d. The total layout sizes of the proposed CMOS ring and LC-VCO are 20 μm × 20 μ m and 320 μm × 320 μm, respectively.

4. Conclusion

A design methodology for CMOS current-starved ring VCOs and CMOS cross-coupled LC VCOs has been presented in this paper. Supply voltage, tuning range, PN, power dissipation, maximum output power and layout area are recorded for 24-GHz current-starved ring VCO and 76-GHz CMOS cross-coupled LC VCO. Table 1 compares these two VCOs with similar VCOs of previous research, and shows that proposed VCOs have lower power dissipation and chip area with competitive PN. For short- and mid-range RADAR applications, one desires low power and wide tuning range; hence, the ring VCO may be of choice. However, automotive long-range RADAR requires high oscillation frequency with narrow tuning range and better PN performance; hence the LC-VCO will be of choice.

References

[1] Yadav R, Dahiya P K and Mishra R 2016 A high performance 76.5 GHz FMCW RADAR for advanced driving assistance system. In: *Proceedings of the 2016 3rd International Conference on Signal Processing and Integrated Networks (SPIN)*, Noida, pp. 383–388

[2] Biabanifard S, Largani M S and Asadi S 2015 Delay time analysis of combined CMOS ring oscillators. *Electr. Electron. Eng. Int. J.* 4(2): 53–64

[3] Yadav R, Dahiya P K and Mishra R 2018 A scalable millimetre-wave differential CMOS cross-coupled VCO for automotive radar application. *J. Circuits Syst. Comput.* 27(10): 1850158

[4] Farahabadi PM, Miar-Naimi H, and Ebrahimzadeh A 2009 A new solution to analysis of CMOS ring oscillators. *Iran. J. Electr. Electron. Eng.* 5(1): 32–41

[5] Soltanian B, Ainspan H, Rhee W, Friedman D and Kinget P R 2007 An ultra-compact differentially tuned 6-GHz CMOS LC-VCO with dynamic common-mode feedback. *IEEE J. Solid-State Circuits* 42(8): 1635–1641

[6] Abuelma A and Muhammad T 2017 Recent developments in current-mode sinusoidal oscillators: circuits and active elements. *Arab. J. Sci. Eng.* 42(7): 2583–2614.

[7] Tang K W., Leung S, Tieu N, Schvan P and Voinigescu S P 2006 Frequency scaling and topology comparison of millimeter-wave CMOS VCOs. In: *Proceedings of the 2006 IEEE Compound Semiconductor Integrated Circuit Symposium*, pp. 55–58

[8] Trivedi V P, To K H and Huang W M 2011 A 77 GHz CMOS VCO with 11.3 GHz tuning range, 6 dBm output power, and competitive phase noise in 65 nm bulk CMOS. In: *Proceedings of the 2011 IEEE Radio Frequency Integrated Circuits Symposium*, pp. 1–4

[9] Li Z, Wang Z, Li Z and Li Q 2015 Design of 33–40 GHz low power VCO in 90-nm CMOS technology. *WSEAS Trans. Circuits Syst.* 14: 119–128