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Low power dynamic voltage scaling and CCGDI based Radix-4 MBW multiplier using parallel HA and FA based counters for on-chip filter applications

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Abstract. In this paper, a new design of low power, high performance Radix-4 MBW multiplier unit has been described. The low power performance has been achieved by dynamic voltage scaling. Based on CCGDI technique which reduces the switching activity and output capacitance, the proposed multiplier unit has been designed by utilizing three different low power methodologies i.e., reduction in output capacitance and switching activity along with biasing voltage reduction. In order to reduce the number of transistor and delay, here GDI based parallel adders are used in the Wallace tree counters. The multiplier has been implemented with constant threshold voltage PTM 45 nm devices technology and simulated in standard CAD tool simulator for 4, 8 and 16 bit operand multiplications. The proposed design consumes 238.98 μw average power and it has a propagation delay of 2.458 ns for 16 × 16 bit multiplications at speed 100 MBps which is 47% better in terms of power-delay-product than counter based GDI Wallace tree multiplier structure.

Keywords. CCGDI; CAD simulation; DVS; GDI technique; level shifter; MBW multiplier.

1. Introduction

In modern days due to rapid growth in multimedia and communication system, real-time on-chip signal processing systems design has become a major topic of interest. Low power, high speed along with small area and less complexity in an on-chip DSP processor is a challenging task for researchers and design engineers. It is well known to the community that multiplication is one of the primary and repetitive tasks performed in all DSP processors. Therefore, to achieve low power and fast performance in DSP processors one has to design an efficient multiplier capable of meeting the desired performance criterion. The problem of designing such an efficient multiplier is two-fold: (i) one has to carefully choose a fast multiplication algorithm and (ii) apply proper low power techniques to achieve desired performance. Among different multiplication algorithms studied in [1–6], Radix-4 MBW algorithm appears to be one of the most efficient methods. The major advantage of MBW multiplier is that it can also provide the signed bits multiplication with reduced number of steps which makes it faster compared to the other algorithms studied so far. On the other hand, Wallace tree structure in MBW method helps to achieve low latency and reduced critical path delay. Therefore a low power MBW multiplier is a suitable choice for on-chip filter applications. Low power circuit design has been a major research area in the past couple of decades [7]. GDI technique in [8], which focuses in reduction of output capacitance of a circuit to achieve low power operation has already been reported in open literature. Compared to other low power techniques, GDI is one of the most recent and efficient approaches, where basic logic gates can be implemented using only two transistors. Very recently, the authors have introduced a new low power technique which is termed as CCGDI technique [9]. This technique reduces the output capacitance and also reduces the switching activity of the circuit to reduce the dynamic power consumption significantly. Another approach of reducing the power consumption is by reducing the biasing voltage studied in [10]. This technique is well known as DVS. However, reduction of biasing voltage requires additional level shifter circuits in order to perform handshaking between high and low bias voltages driven gates. The design of low to high level shifter is complex especially at sub-threshold voltage region [11–15]. Unfortunately, all such sub-threshold level shifters suffer from either poor latency or area burden.

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In this paper, we have addressed the problem of designing a fast radix-4 MBW multiplier unit by sensibly amalgamating two major techniques, i.e., CCGDI and DVS for superior low power performance. However, combining these two techniques is not a straight forward task and poses some serious design challenges. The DVS technique requires additional level shifters which in turn increases the delay in the multiplication process. This delay becomes significant when the biasing voltage is lower than the sub-threshold voltage of the transistors. Moreover, these level shifters also contribute in increasing the implementation area. In order to overcome the problem of inserting the level shifters in the design we have separated the entire Wallace tree block into two circuit islands according to the delay paths. The DVS control has been wisely introduced in the off-critical delay paths to minimize the delay introduced by the level shifters. Instead of using any readily available of the shelf level shifter we have designed a completely new one employing minimum number of transistors. Therefore, the new design is area efficient, high speed and simultaneously takes care of matching the latency of the critical delay path with the DVS controlled off-critical delay path. To the best of our knowledge, such a design has been explored in here for the first time. Detailed performance analysis has been carried out for the proposed level shifter and presented. The proposed level shifter consumes only 91 pw power which is much lower than other state-of-the-art designs and its conversion range is from 0.18 volts to 1 volts. Along with DVS controlled Wallace tree structure we have introduced the CCGDI technique in the encoder block of radix-4 MBW multiplier as the second low power approach for reducing both switching activity and output capacitance. All the other sub-modules of the multiplier have been designed by GDI gates in order to reduce the dynamic power consumption. The novelty of the design is that, it utilizes three ways of low power methodologies i.e., output capacitance, switching activity and voltage reductions together. The next sections are categorized as follows. In section 2, detailed architecture of the proposed multiplier structure and MBW algorithm have been discussed. Section 3 describes about the design of voltage level shifters for dynamic voltage scaling. Section 4 details on dynamic voltage scaled Wallace tree structure and final stage accumulation architecture. CAD tool based simulation and comparison with existing CMOS and GDI based state-of-the-art designs in terms of power, delay and area (transistor count) has been discussed in section 5. Finally, the conclusion and future work have been presented in section 6.

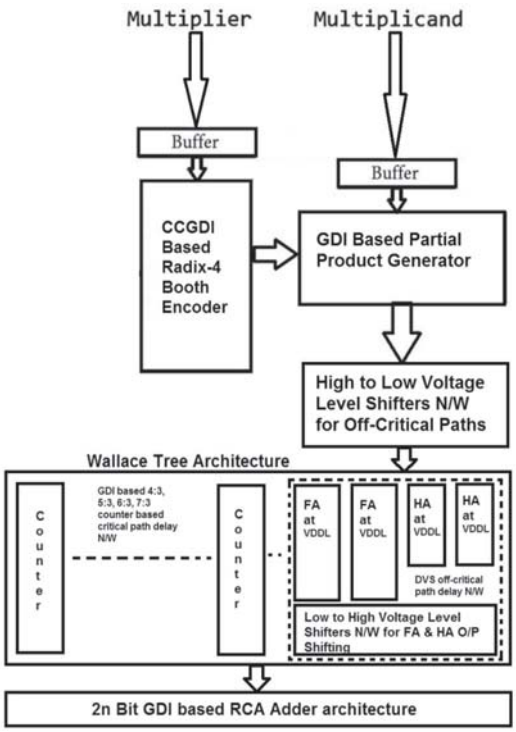

Figure 1. Proposed multiplier architecture.

2. Proposed multiplier design

A parallel binary multiplier generates its partial products by AND operation between corresponding multiplier and multiplicand bits [16]. Such multiplier design is very simple but it loses its efficiency when the number of operand bit increases. Therefore for higher bits of multiplications other multiplication methods like serial, Vedic, Wallace, Booth, etc. algorithms are preferred. Few such approaches based on GDI technique have been presented in recent past by authors [17–19]. In our previous communication, we have proposed a counter based GDI Wallace Tree structure to accumulate the partial products in order to improve the efficiency of real time on-chip multiplication [19]. To improve the design furthermore in the present communication we have modified the design as CCGDI based MBW multiplier. The overall design schematic is shown in figure 1. The design consists of the following sub-modules: The multiplier bits and multiplicand bits are taken as signed bits and passed through n bit buffers, respectively. All buffers are containing two series CMOS inverters and thus built with four transistors. The buffered multiplier bits are grouped into three bits and fed to CCGDI Radix-4 Booth Encoders [20]. The encoded outputs are multiplied with multiplicands by GDI PPG. The same weight PPG outputs are accumulated using Wallace Tree Architecture. The Wallace tree architecture consists of HA, FA and various counters. For two or three numbers of partial products having same weight, the accumulation is performed by HA or FA. When the numbers of same weight partial products are more than three then counter based accumulations are performed. In order to introduce DVS in the design we have

separated the Wallace tree architecture into two circuit islands. The first circuit island is the lower weight partial product accumulator section which consists of single stage FA or HA only and therefore produces lower delay in producing the final stage partial products. Whereas the second circuit island is for higher weight partial products accumulation. For accumulation of higher weight partial products, which generally have more than three partial products of same weight, compressors or counters are used [21–23]. As the counter based accumulation circuits are complex compared to simple FA or HA structure, it produces greater delay compared to lower weight partial products accumulation circuit island. Therefore we have introduced the voltage level shifters in the lower delay or off-critical delay paths circuit island and thus the lower weight partial product accumulation section becomes DVS compatible. The biasing voltage for static supply based circuit island and the DVS controlled section can be managed by external FPGA based processing [24]. Unlike previous communication [19] where the counters were designed with GDI gates here we have introduced eight transistorized parallel full adders and five transistorized half adders based counters which reduce the number of transistors significantly. Finally, 2n bit wide GDI based ripple carry adder structure is used to get the final results. The working and detailed design of each block are described in the following sub-sections.

2.1 *Radix-4 modified booth's algorithm*

In this algorithm multiplier bits are grouped and encoded. Further, those encoded bits are multiplied with multiplicand bits. By using encoding technique the numbers of partial products get reduced. Table 1 shows the radix-4 encoding technique. The input bits are three consecutive multiplier bits as Xi − 1, Xi and Xi + 1. The three binary encoded outputs are X, 2X and NEG, which denotes 0, ± 1 and ± 2 value. These encoded bits are fed to the PPG. PPGs are generating the partial products by taking the encoded bits along with multiplicand bits. The final results are found by addition operation of partial products having same weights in form of Wallace tree structure. As the numbers of partial products are reduced therefore the critical path delay is also low which makes the multiplication faster [4].

Table 1. Booth encoding.

Inputs			Encoded outputs		
Xi+ 1	Xi	Xi−1	X	2X	NEG
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	0	0	1

2.2 *CCGDI based Radix-4 booth encoder*

In the radix-4 encoding process, X is the Multiplier which is encoded with the circuit shown in figure 2. X2j − 1, X2j, X2j + 1 are the three corresponding grouped bits which are encoded to 0, X, 2X, − X, − 2X. In order to reduce the critical path delay, output capacitance and switching activity of the circuit, CCGDI based booth encoder is introduced [20]. The schematic of eight transistorized CCGDI booth encoder circuit is shown in figure 2.

The CCGDI based Radix-4 booth encoder circuit is made of with two numbers of three transistorized XOR gates and one number of two transistorized GDI F1 circuit [20]. The functional response of the CCGDI booth encoder is verified using PTM 45 nm technology simulation. The inputs are set as bit pattern with 10 ns on time. The transient responses of the encoder are shown in figure 3.

Figure 4 shows the average power consumption of the encoder at different technology nodes. Three PVT corners are tested. At 45 nm technology it consumes 1 pw power which is $1/6^{th}$ of power consumption at 250 nm technology.

2.3 *GDI based partial product generator*

Figure 5 shows the schematic of GDI gate based partial product generator. It takes the outputs of the encoder and multiplies with corresponding two bits of multiplicand (Yi and Yi − 1) to form a partial product. The PPG circuit is implemented using GDI 2T AND, 2T OR and 3T XOR gates [19]. Using GDI technique a PPG circuit is built with nine transistors. After obtaining the partial products those values are accumulated by Wallace tree structure [19] for final stage addition purpose.

The transient response of the proposed PPG circuit is shown in figure 6. The CAD simulation is carried out with transistors having PTM 45 nm technology.

Figure 7 shows the average power consumption of the partial product generator for different PVT models using GDI gates at different technology nodes.

3. Voltage level shifters for DVS

A DVS system deals with multiple voltage sources. General biasing voltage sources are treated as high voltage source (VDDH) and sub circuits which are driven by sub-threshold power supply (VDDL) consume much lower power compared to VDDH. The handshaking between VDDL driven signals and VDDH driven signals are made by LS. The high

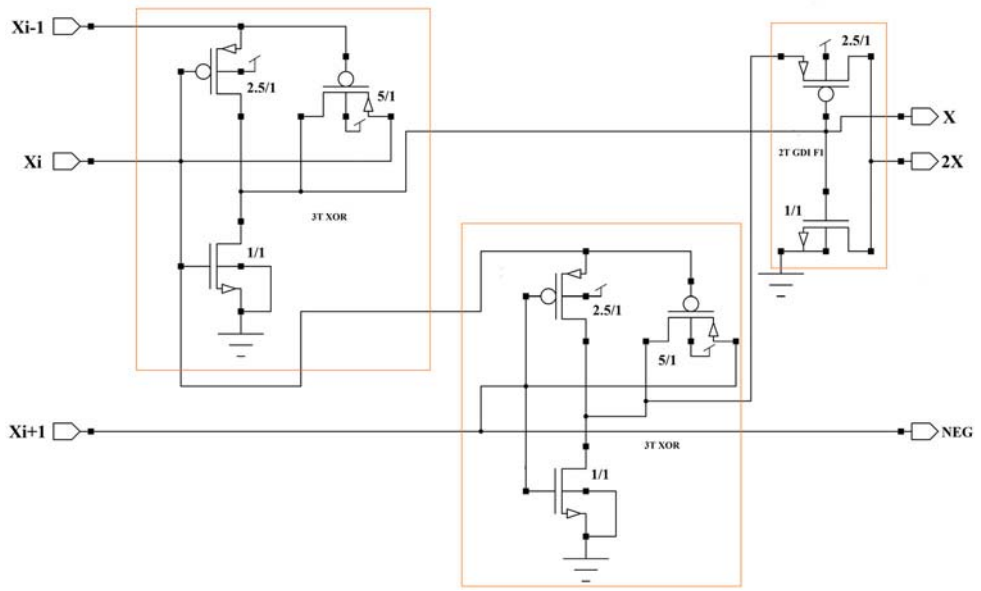

Figure 2. CCGDI based Radix-4 booth encoder (aspect ratios are shown against each transistor).

to low level shifter is described in [10] has very simple design with two series inverters biased with VDDL. The conventional low to high LS can be designed using differential cascade voltage switch and current mirror load. But such designs failed to perform in sub-threshold voltage region. That is why a sub-threshold low to high LS design is always remaining challenge for designers. Few notable designs which have been referred in the introduction section lacks with either area constrain or delay. In the present communication the authors are presenting a new design for sub-threshold LS. The design of the proposed LS in 45 nm technology is shown in figure 8.

The circuit propagates the input signal INL to an inverter comprised of NMOS_1 and PMOS_1 which works over sub-threshold low voltage level. The output of the inverter is fed to a modified Wilson current mirror and a driver inverter. The transistors of the first inverter are working in sub-threshold region which results linear responses as differential fast transition low-voltage input signals for NMOS_2. The NMOS_2 transistor is a narrow width transistor which offers larger on state impedance resulting lower value of drain current through PMOS_2. The transistor PMOS_2 is also a narrow width transistor which controls the gate voltage for PMOS_3. When the transistor PMOS_3 is on, the impedance decreases across it and results a larger drain current to drive through PMOS_4 and NMOS_3. The transistors PMOS_4 and NMOS_3 act like a current output inverter with strong pull up at the shorted drain. Therefore, the low logic is inverted with pull up voltage at VDDH which is being forwarded to final stage inverter. The final stage inverter is the output driver creating INH as the same logic of the low input logic INL. All the transistor geometries at 45 nm technology are shown in figure 8. Figure 9 shows the transient response of the proposed LS at different process corners.

The typical PVT case is simulated with the TT model parameters and the VDDL is set as 0.18 volts (threshold voltage of MOS transistor is taken as 0.19 volts) whereas the VDDH is set as 1 volts analysis. Comparative analysis between the proposed LS and other notable designs have been carried out to reveal the efficiency of the design. Figure 10 is showing the power consumptions at different technology nodes at 1 MHz sub-threshold input. Figure 11 is showing the VDDL verses transient delay characteristics of the proposed LS at 45 nm technology. The delay increases at lower sub-threshold region. At 1 MHz input signal the delay becomes 24 ns for TT model. As the VDDL increases the delay minimizes for all PVT corners. The proposed LS show that for a voltage conversion stage from 0.19 volts to 1 volts, it dissipates 34 fJ per transition. The core area of the proposed level shifter consumes 22 μm^2 area using schematic driven layout. Therefore the PPA overhead for introducing the LS is minimal.

Detailed analysis has been carried out at PTM 45 nm process technology by keeping the same aspect ratios of the devices as mentioned in the articles. The detailed results have been shown in table 2.

The proposed Wallace tree structure is made of with DVS controlled FA and HA structures which adds three and two bits at a time having same weights. The FA and HA are designed using eight transistors (8T FA) and five transistors (5T HA), respectively [16]. As the FA and HA structures contain lower delay path therefore DVS is employed over such non critical paths. The comparison between DVS controlled path and conventional path is shown in table 3.

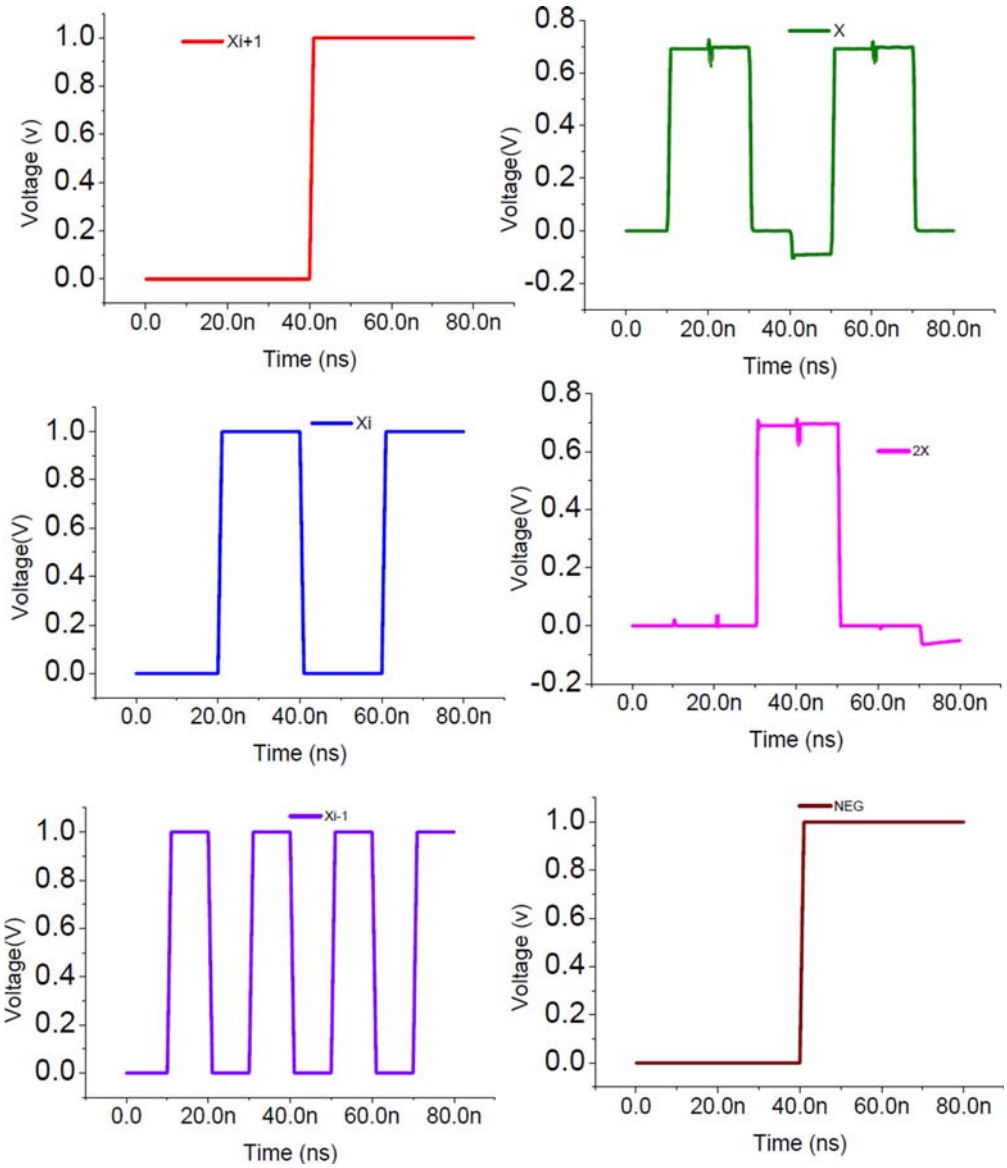

Figure 3. Transient response of CCGDI Radix-4 booth encoder.

From table 3 it has been found that DVS controlled FA and HA structures when driven by sub-threshold voltage, consume 90% lower power consumption than fixed VDD based structures. The latency increased due to insertion of level shifters is analyzed with respect to critical delay path circuit island and has been discussed in section 4. It has been found that the extra latency introduced by the LS in the off-critical delay path won't have any influence over the final latency of the multiplier. When number the partial products having same weight are more than three counter based accumulation is implemented. In the proposed multiplier design the counter based structure is treated as the critical delay path based circuit island.

4. Counter based partial products accumulation

An (m, p) counter takes an m bit input bits from a column and produces a p bits output which detects the number of input 1 bits. Actually it counts the number of input bits set to 1. Partial products can be reduced by compressor circuits also [21]. But in our proposed design counter based reduction technique has been applied as it reduces the number of reduction stages than compressor based technique. Conventional high speed counter designs can be found from [22]. Few modifications have been found in recent article [23]. In the present communication we have implemented higher bit counters using parallel 3:2

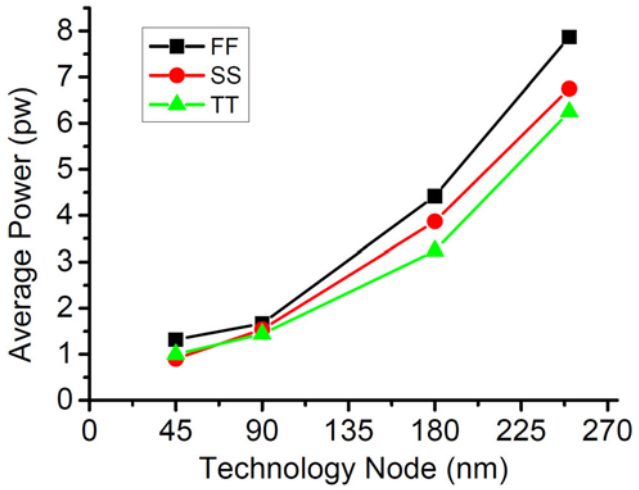

Figure 4. Average power consumption of CCGDI encoder at three PVT corners for different technology nodes.

counters. A 3:2 counter counts number of '1' present in three input lines. Therefore a 3:2 counter has the same circuit configurations as a FA. Thus different types of counters can be designed with the help of 8-T FA are as follows.

4.1 *GDI 7:3 counter*

In Wallace structure a 7:3 counter counts the number of '1' present in seven partial products (e.g., x0–x6) of same weight. As the maximum count can be seven therefore the output can be represented in the form of three bits. The operation is same like addition operation therefore the three outputs (Sum, Cout1, Cout2) can be found as follows,-

$$\begin{aligned} \text{Sum} &= [(\text{X0} \oplus \text{X1}) \oplus (\text{X2} \oplus \text{X3})] \oplus [(\text{X4} \oplus \text{X5}) \oplus \text{X6}] \\ \text{Cout1} &= (\text{m1} \oplus \text{m2}) \oplus \text{m3} \\ \text{Cout2} &= (\text{m1} \,.\, \text{m2}) + ((\text{m1} \oplus \text{m2}) \,.\, \text{m3}) \end{aligned} \tag{1}$$

where

$$\begin{aligned} \text{m1} &= \text{X0} \,.\, \text{X1} + \text{X2} \,.\, \text{X3} + ((\text{X0} + \text{X1}) \,.\, (\text{X2} + \text{X3})) \\ \text{m2} &= [((\text{X4} + \text{X5}) \,.\, \text{X6}) + \text{X4} \,.\, \text{X5}] \\ \text{m3} &= [\text{X0} \,.\, \text{X1} \,.\, \text{X2} \,.\, \text{X3} + ((\text{X0} \oplus \text{X1}) \oplus (\text{X2} \oplus \text{X3}))] \\ & \quad (\text{X4} \oplus \text{X5}) \oplus \text{X6}] \end{aligned}$$

GDI parallel FA based 7:3 counter can be implemented as shown in figure 12(a). It consists of four numbers of

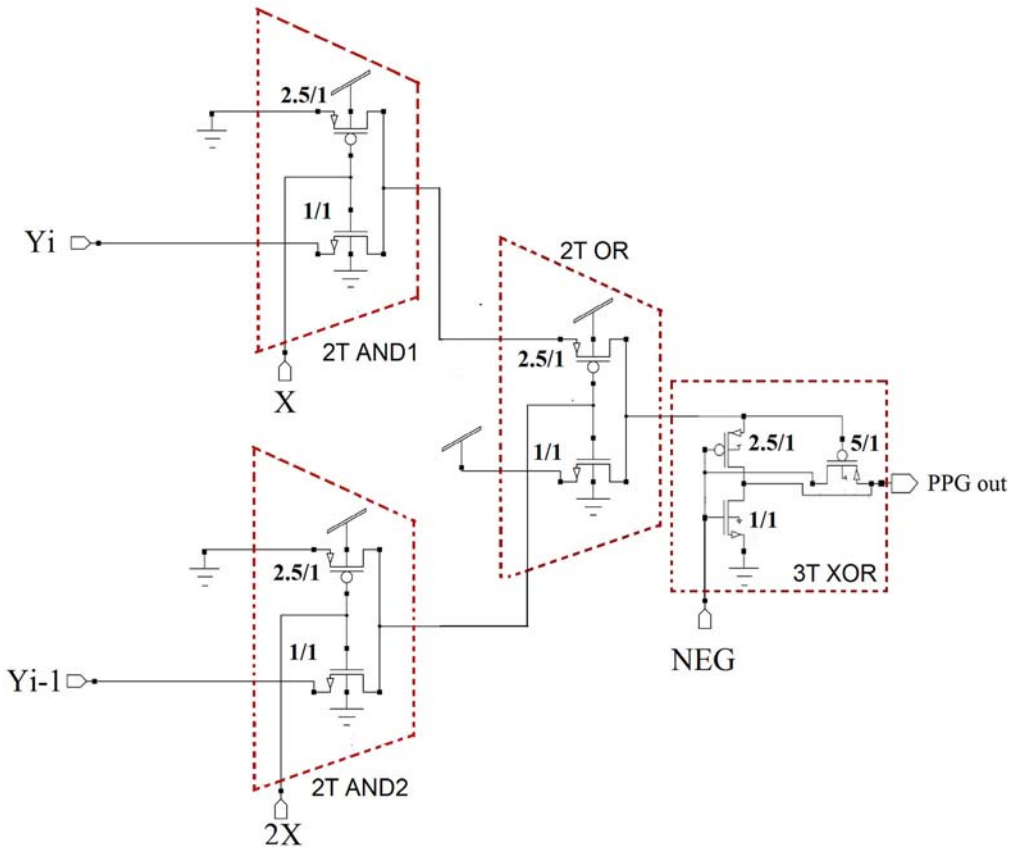

Figure 5. Nine Transistorized GDI PPG Circuit Schematic (aspect ratios are shown against each transistor).

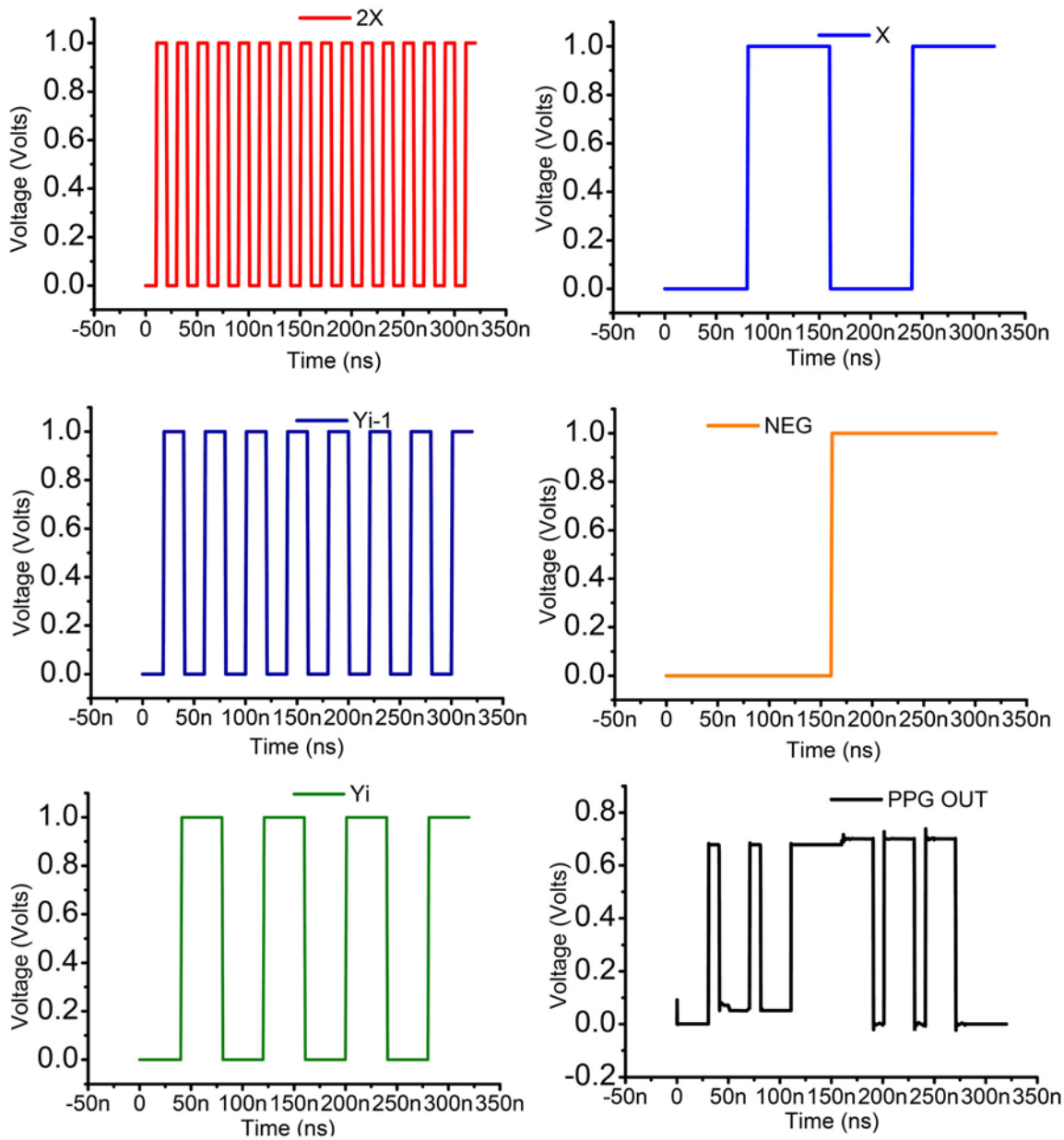

Figure 6. Transient response of the GDI PPG circuit.

eight transistorized FA. Therefore, the total number of transistor count is 32. The maximum delay introduced by single stage 7:3 counter is 2.368 ns.

4.2 *GDI 6:3 counter*

Similar to 7:3 counters, a 6:3 counter counts the number of '1' present in six partial products of same weight (e.g., x0–x5). As the maximum count is six so the counter has three outputs (Sum, Cout1, Cout2) as follows.e

$$\begin{aligned}\text{Sum} &= \text{p0} \oplus \text{p1} \oplus \text{p2}\\ \text{Cout1} &= (\text{p0}\,.\,\text{p1} \oplus \text{p0}\,.\,\text{p2} \oplus \text{p1}\,.\,\text{p2}) \oplus (\text{g0} \oplus \text{g1} \oplus \text{g2})\\ \text{Cout2} &= (\text{g0}\,.\,\text{g1} + \text{g0}\,.\,\text{g2} + \text{g1}\,.\,\text{g2}) + ((\text{p0}\,.\,\text{p1})\text{g2}\\ &\quad + ((\text{p0}\,.\,\text{p2})\,.\,\text{g1}) + ((\text{p1}\,.\,\text{p2})\,.\,\text{g0}\end{aligned} \tag{2}$$

where

$$\text{p0} = \text{X0} \oplus \text{X1}, \text{p1} = \text{X2} \oplus \text{X3}, \text{p2} = \text{X4} \oplus \text{X5}$$
$$\text{g0} = \text{X0}\,.\,\text{X1}, \text{g1} = \text{X2}\,.\,\text{X3}, \text{g2} = \text{X4}\,.\,\text{X5}$$

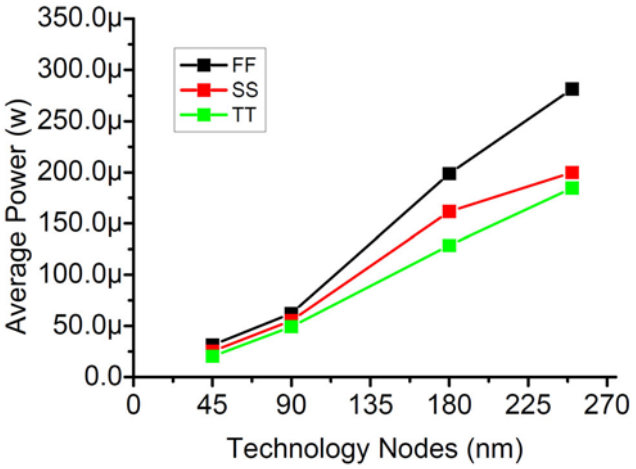

Figure 7. Average power consumption of GDI based PPG at different technology nodes.

The GDI eight transistorized (8T) FA and five transistorized (5T) HA based schematics of 6:3 counter is shown in figure 12(b). The total number of transistor count is 29. The maximum delay introduced by 6:3 counters is same as 7:3 counters.

4.3 *GDI 5:3 counter*

A 5:3 counter counts number of '1' present in five same weighed partial products terms. As the maximum count can be 5 therefore it also has three outputs as follows,-

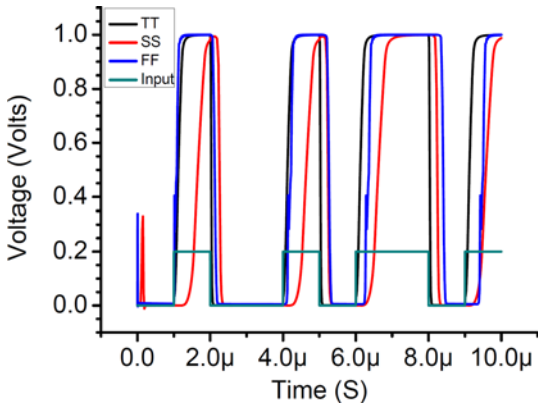

Figure 9. Transient response of the proposed LS: Input (INL) and INH at different process corners at VDDL as 0.18 volts and VDDH as 1 volts.

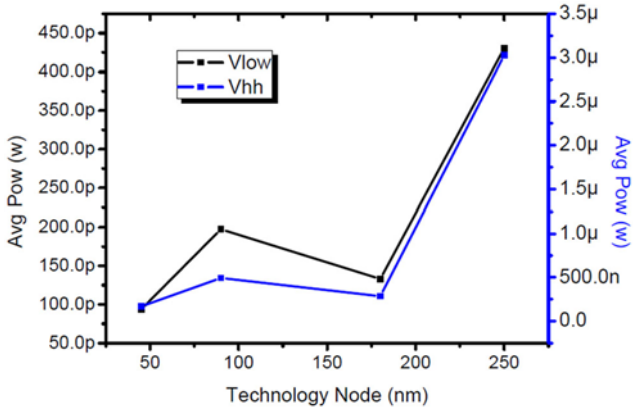

Figure 10. Average power consumption of the proposed LS at different technology nodes.

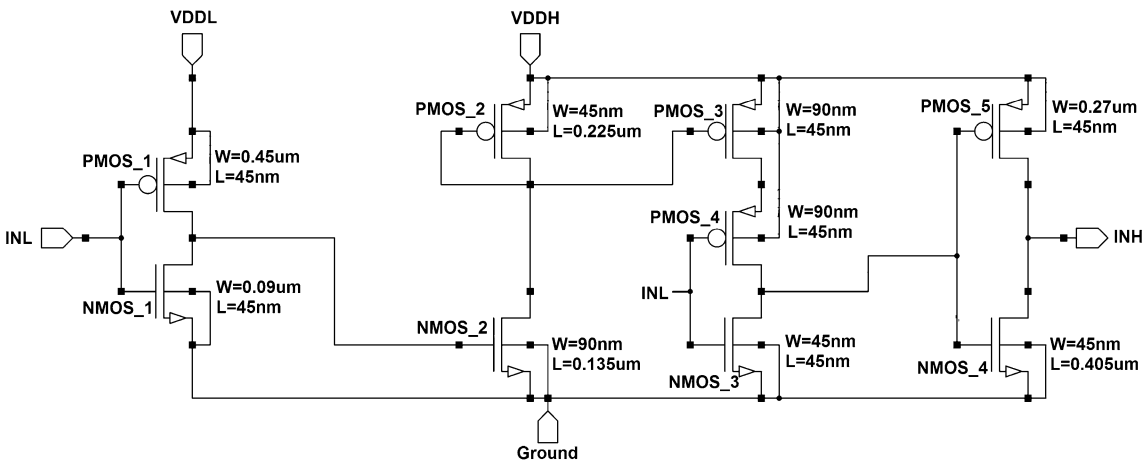

Figure 8. Proposed low to high sub-threshold level shifter at 45 nm technology.

$$\begin{aligned} \text{Sum} &= \text{p0} \oplus \text{p1} \oplus \text{X4} \\ \text{Cout1} &= (\text{g0} \oplus \text{g1} \oplus \text{h0}) \oplus (\text{h1} \oplus \text{h2}) \oplus ((\text{p0} \,.\, \text{p1}) \oplus \text{h3}) \\ \text{Cout2} &= (\text{g0} \,.\, \text{g1} + \text{g0} \,.\, \text{h2}) + (\text{g0} \,.\, \text{h3}) + (\text{g1} \,.\, \text{h0} + \text{g1} \,.\, \text{h1}) \end{aligned} \tag{3}$$

where

$$\text{h0} = \text{X0} \,.\, \text{X4},\ \text{h1} = \text{X1} \,.\, \text{X4},\ \text{h2} = \text{X2} \,.\, \text{X4},\ \text{h3} = \text{X3} \,.\, \text{X4}$$

The GDI 8T FA based 5:3 counter schematic is shown in figure 12(c). Such GDI based 5:3 counter is built with 16 numbers of transistors. The maximum delay introduced by single stage 5:3 counter is 1.912 ns.

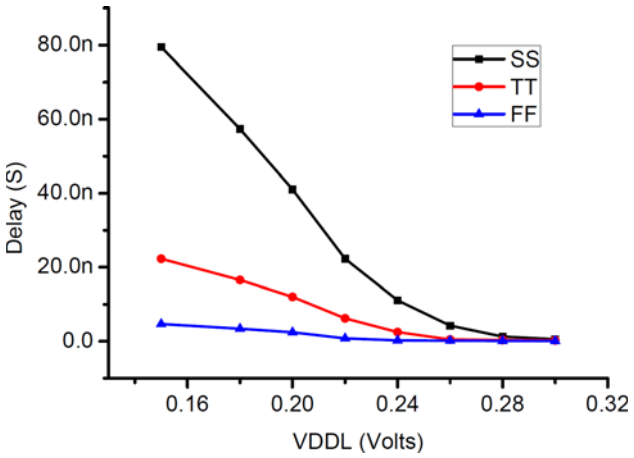

Figure 11. VDDL vs. Transient delay characteristics of the proposed LS at 45 nm technology.

4.4 *GDI 4:3 counter*

In counter based Wallace tree structure a 4:3 counter counts number of '1' present in four partial products of same weight (e.g., x0, x1, x2, x3). It can have the maximum count as four and thus it has three outputs (Sum, Cout1, Cout2) as follows,-

$$\begin{aligned} \text{Sum} &= \text{p0} \oplus \text{p1} \\ \text{Cout1} &= (\text{p0} \,.\, \text{p1}) + (\text{g0} \oplus \text{g1}) \\ \text{Cout2} &= \text{g0} \,.\, \text{g1} \end{aligned} \tag{4}$$

Figure 12(d) shows the schematic of GDI 8T FA and 5T HA based 4:3 counters. It is built with 13 numbers of transistors only. The maximum delay introduced by single stage 4:3 counter is 1.621 ns.

In the Wallace tree structure the off critical delay path circuit island which accumulates the two/three numbers of same weight partial products by HA/FA sub-modules, produces maximum delay of 1.456 ns without introducing level shifters and it produces maximum delay of 2.098 ns after insertion of level shifters for DVS, which is still lower than the minimum delay of single stage 7:3 counter based critical path circuit island. For higher stage of counter circuit based accumulation, the critical path delay is even more than DVS controlled circuit island. Table 4 shows the delay introduced at same weight partial product accumulation stage for different circuit island.

4.5 *Final RCA adder stage*

When the counter based accumulation of partial products are reduced to two rows, RCA adder is used to produce the

Table 2. Simulation results of different LS.

Design	Conversion range	Avg. power (nw)	Delay (ns)	Area (Tr. count)
Conventional Type-I	Above threshold- VDDH	0.215	23.26	8
Conventional Type-II	Above threshold- VDDH	0.158	13.12	6
Lanuzza *et al* 2017 [14]	Sub-Threshold- VDDH	0.0726	38.28	14
Zhao *et al* 2015 [11]	Sub-threshold- VDDH	134.36	13.87	12
Wen *et al* 2016 [13]	Sub-threshold- VDDH	143.52	13.56	11
Hosseini *et al* 2017 [15]	Sub-threshold- VDDH	18.923	37.203	14
Proposed LS	Sub-threshold- VDDH	0.0937	1.728	9

Table 3. Comparison between fixed VDD and DVS structures.

Type	Design	Avg. Power (μw)	Delay (ns)	No. of transistors
Fixed VDD	5T HA	18.35	1.165	5
	8T FA	27.849	1.456	8
Multiple VDD (DVS)	5T HA	0.629	1.945	18
Considering VDDL as sub-threshold voltage	8T FA	1.054	2.098	21

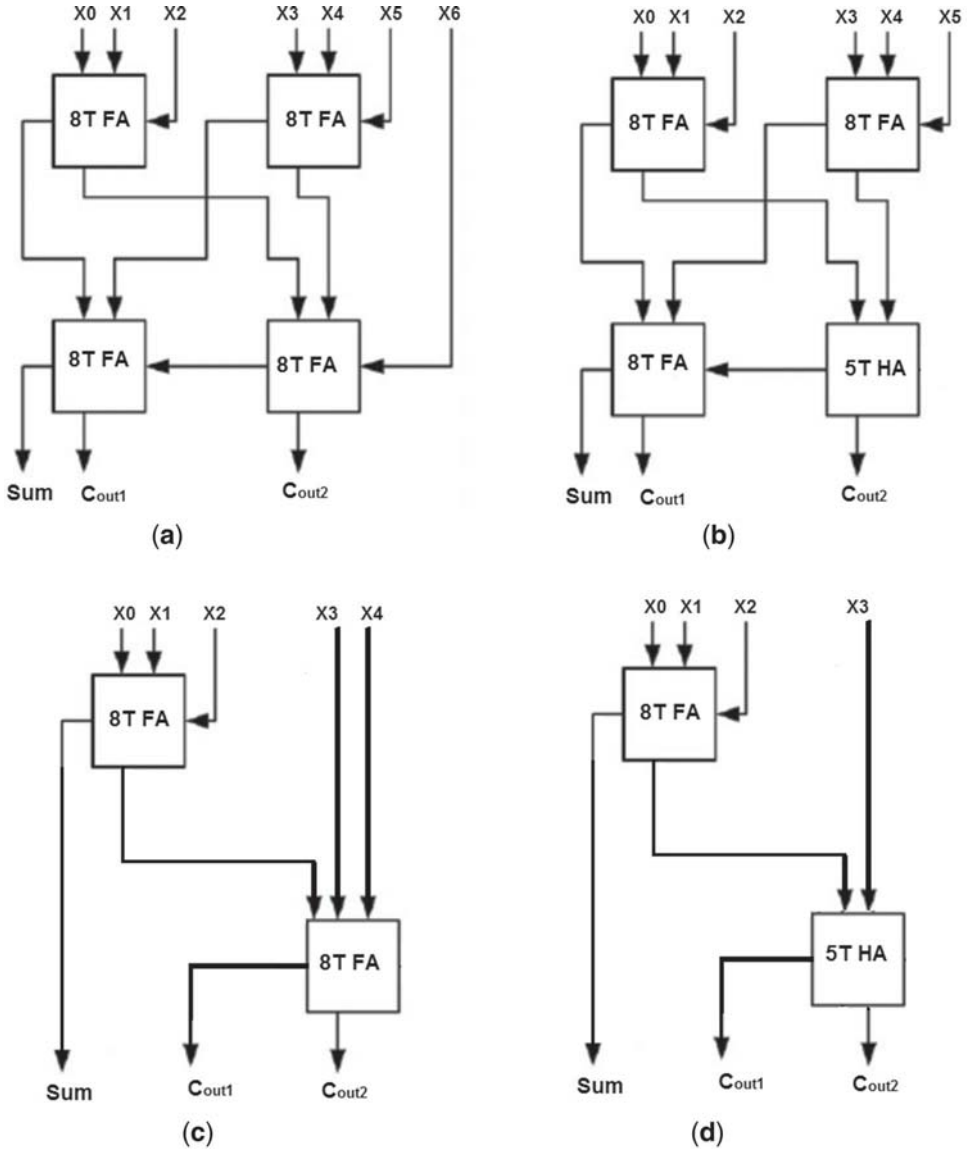

Figure 12. 8-T FA and 5-T HA based counter schematics for critical path circuit island **a** 7:3 counter, **b** 6:3 counter, **c** 5:3 counter and **d** 4:3 counter.

Table 4. Delay introduced at same weight partial product accumulation stage for different circuit island in Wallace tree structure.

Off-critical delay path circuit island		Critical delay path circuit Island	
Sub-circuit module	Delay introduced (ns)	Sub-circuit module	Delay introduced (ns)
HA without LS	1.165	Single Stage 4:3 counter	1.621
FA without LS	1.456	Single Stage 5:3 counter	1.912
HA with LS	1.945	Single Stage 6:3 counter	2.368
FA with LS	2.098	Single Stage 7:3 counter	2.368

final result. For construction of 2 N bit wide RCA adder we have also used eight transistorized full adder and five transistorized half adders. Figure 13 shows the schematic for RCA adder structure.

5. Simulation results and analysis

The proposed methodology based designs are simulated for 4-bit, 8-bit and 16-bit operand multiplications and tested to reveal the benefits. The simulation environment is set with

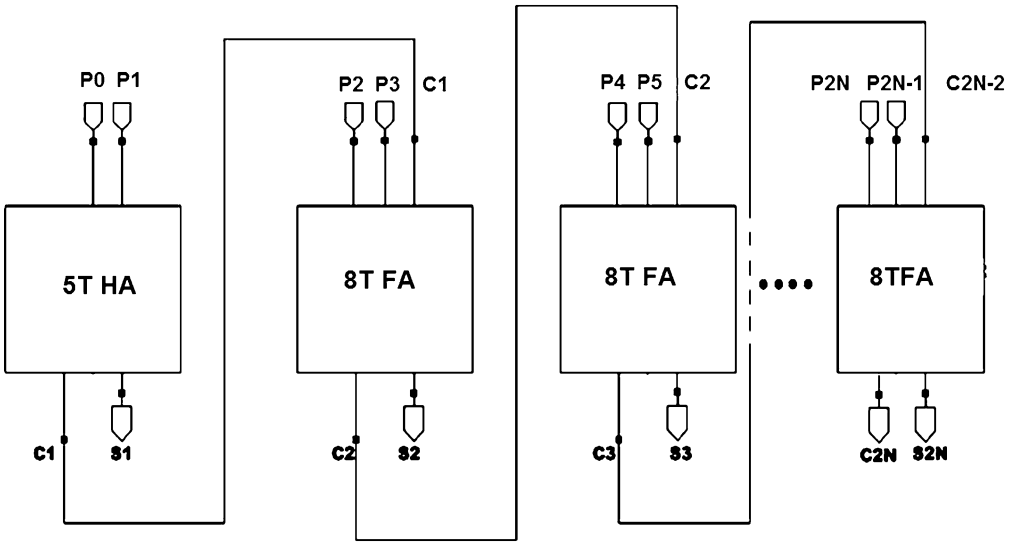

Figure 13. 8T FA and 5T HA based 2N bit wide RCA adder schematic.

Table 5. Input specifications for simulation.

input type	Bit
"Low" logic value	0 v
"High" logic value	1 v
VDDH	1 v
VDDL	0.2 v
Bit rate	100 MBps
Rise and fall time duration	1 ns

standard EDA simulator using PTM 45 nm technology. Table 5 shows the input specifications for functional test of the design.

The simulation results are compared with existing state of art designs of multipliers along with our proposed counter based GDI Wallace tree multiplier. The comparisons are made in terms of timing and power analysis, PDP and transistors counts. The detailed results are given in table 6.

By analyzing the results of the proposed design and comparison with other state-of-the-art designs, it has been

Table 6. Detailed simulation results of various multipliers.

Design	Operand size	Latency (ns)	Power (μw)	PDP (fJ)	Area (Tr. count)
GDI array multiplier [16]	4 bit	1.29	39.98	50.02	160
	8 bit	6.35	168.74	1071.5	640
	16 bit	11.76	6543.98	76957	2.5 k
GDI vedic multiplier [18]	4 bit	0.9115	124.34	85.56	176
	8 bit	1.134	478.98	541.15	698
	16 bit	4.675	2098.56	9797.6	2.8 K
GDI wallace tree multiplier [19]	4 bit	1.22	12.87	13.028	137
	8 bit	1.85	68.96	127.57	543
	16 bit	2.64	423.54	1118.1	2.2 K
Radix-8 booth multiplier [6]	4 bit	0.994	148.87	147.97	564
	8 bit	2.789	408.61	1135.9	2.3 K
	16 bit	3.56	2382.76	8480.9	8.4 K
Radix-4 booth multiplier [4]	4 bit	0.785	86.23	67.667	488
	8 bit	1.94	120.34	233.46	1.4 K
	16 bit	3.25	450.87	1465.3	6.1 K
GDI radix-4 MBW multiplier [17]	4 bit	1.31	18.34	20.555	302
	8 bit	2.09	60.19	125.79	944
	16 bit	3.56	285.98	1018.1	1.5 K
Proposed GDI DVS radix-4 MBW multiplier	4 bit	1.35	6.45	8.707	228
	8 bit	1.76	40.08	70.54	1.1 K
	16 bit	2.45	238.98	585.5	1.6 K

found that the proposed multiplier is 31% faster than [6], 24% faster than [4] for 16-bit case and 15% faster than our previous work [17] for 8x8-bit multiplication. Though by introducing DVS technique in 4 bit operand, the multiplier latency is more than fixed biasing multiplication [19], but for 8 and 16 bit operand, the latencies are improved by 4% and 7%, respectively. This improvement has been found by introducing GDI parallel 8-T FA and 5-T HA based counter circuits. The best results we have found in power consumption of the design. It is also notable that the proposed design is consuming only 238.98 μw average power for 16 bit operation which is 16% lower than [17] and 43% better than our previous communication [19]. Therefore, the figure of merit in terms of power delay product of the proposed design has been improved by more than 42% from [17, 19] and 62% than [4]. The number of transistors for the proposed design is more than simple GDI array multiplier [16, 18] for 4 bit operands. As the operand size increases the proposed multiplier design requires much lower number of transistors than other state of art designs.

6. Conclusion and future scope

From the simulation results, it has been revealed that the proposed dynamic voltage scaling counter based GDI radix-4 modified Booth Wallace tree multiplier shows better results in low power consumption, area concern and delay performance. The improvement will be more for higher number of bits. Such multiplier designs can be useful for implementing modern MAC unit and on-chip FIR filter design. In future work, the authors would like to implement DA based on-chip FIR filter using this multiplier design which will be applicable in MEMS sensor-Microsystems.

List of symbols

CAD	Computer aided design
CCGDI	Cyclic Combinational Gate Diffusion Input
CMOS	Complementary Metal Oxide Semiconductor
DA	Distributive Arithmetic
DSP	Digital Signal Processing
DVS	Dynamic Voltage Scaling
EDA	Electronic Design Automation
FA	Full Adder
FF	Fast nmos Fast pmos
FIR	Finite Impulse Response
FPGA	Field Programmable Gate Array
GDI	Gate Diffusion Input
HA	Half Adder
LS	Level Shifter
MAC	Multiplier and Accumulator
MBW	Modified Booth Wallace
MEMS	Micro Electro Mechanical Systems
PDP	Power Delay Product
PPG	Partial Product Generators
PTM	Predictive Technology Model
PVT	Process Voltage Temperature
SS	Slow nmos Slow pmos
TT	Typical Transistor

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