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# A novel symmetric switched capacitor multilevel inverter using non-isolated power supplies with reduced number of components

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**Abstract.** In this paper, a novel 15 level symmetric switched capacitor multilevel inverter (SCMLI) structure is proposed first. The structure is developed by using 3 non-isolated DC power sources. The capacitors utilized in the structure can be charged to the summation of all the power supplies by turning ON the minimum number of switching devices. After that a generalized structure of the proposed SCMLI is developed. The voltage and current stresses for different switches of the proposed general structure are discussed. The selection procedure of switched capacitors for the proposed 15 level inverter is presented for resistive and resistive-inductive load conditions. A detailed comparison study of the proposed structure with other recently developed structures shows that the proposed structure requires reduced number of components and the number of switches in the conducting path as compared to other SCMLI structures for generating an output voltage level. Further, the overall cost of the proposed and suggested topologies has been compared based on a cost function (*CF*). It has been observed that the proposed structure is more cost effective as compared to others. An extensive experimental study conducted on a 15 level SCMLI laboratory prototype proves the effectiveness and merits of the proposed structure.

**Keywords.** Conducting switches; multilevel inverter; switched capacitor; total harmonic distortion; total standing voltage; voltage balance.

## 1. Introduction

In recent years, multilevel inverter (MLI) has become one of the key elements in different field of applications such as motor drives, electric vehicles, renewable energy conversion systems, FACTS devices, UPS systems, active filtering, distributed generation systems, induction heating systems etc [1–5]. The advantages of MLIs as compared to classic two-level inverters are: (a) generation of better quality output voltage waveform, (b) lower effect of electromagnetic interferences on output voltage, (c) lower voltage stress across switching devices, (d) higher power handling capability and (e) higher efficiency. Generally, MLIs are able to synthesize stepped output voltage waveform with lower harmonic spectrum by utilizing a number of switching devices, capacitors, diodes and DC voltage sources.

In general, MLIs are classified into three conventional topologies: Neutral Point Clamped (NPC), Flying Capacitor (FC) and Cascaded H-Bridge (CHB). The NPC and FC MLIs utilize one DC source and a number of capacitors to realize the multilevel output voltage. However, the capacitor voltage balancing is one of the major challenges of these topologies [6, 7]. Further, the industrial application of these topologies is limited to low level output voltage due to the requirement of large number of capacitors and switching devices for producing high level output voltage. The CHB-MLI requires lower number of switching devices as compared to NPC and FC MLIs. However, each module of CHB-MLI requires isolated DC source. So, for realizing high quality output voltage, CHB-MLI requires a large number of isolated power supplies. Further, the NPC, FC and CHB MLIs do not possess the output voltage boosting ability. They require front-end DC-DC converter or load-end transformer to achieve the boosting ability. Nevertheless, incorporation of DC-DC converter or transformer decreases the efficiency and reliability, and increases the cost, size, weight and complexity of the structure [8, 9].

To mitigate the limitation of large component requirement in conventional MLIs, a number of innovative MLI structures known as "Reduced Device Count (RDC) MLIs" were reported in the literature [10]. However, these RDC-MLIs do not possess the output voltage boosting ability. To overcome the capacitor voltage unbalancing problem in conventional MLIs, auxiliary circuits such as multi output boost converter is incorporated with the inverter structure

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or complex control algorithms based on redundant switching state (RSS) have been developed to mitigate the capacitor voltage unbalancing problem [11, 12]. Nevertheless, these methodologies of solving the capacitor voltage unbalance problem enhance the cost, weight and complexity of the converter structure.

Switched capacitor multilevel inverters (SCMLIs) have been reported in literature to mitigate the aforementioned limitations of conventional MLIs and RDC-MLIs. SCMLIs utilize capacitors as alternate DC power supplies. By charging and discharging the capacitors, SCMLIs are able to produce boosted near sinusoidal multilevel output voltage waveform at load end. Furthermore, SCMLIs do not require any auxiliary circuit or complex control algorithm to balance the capacitor voltages. The first SCMLI was reported in 1998 by the authors of [13]. In [13], a SC basic unit consisted of two power switches, two diodes and a capacitor was proposed. Furthermore, an MLI structure based on a developed H-bridge and SC basic units was developed. However, the topology requires large number of components and complex control algorithm for capacitor voltage balancing. This topology can be considered as the conventional SCMLI structure. Now a days, a number of innovative SCMLIs have been developed to reduce the number of component and complexity of the conventional SCMLI in the literature [14–25].

The authors of [14] proposed a SCMLI structure which can realize multiple voltage levels by using the concept of partial charging of capacitors. This reduces the number of required capacitors for establishing the same number of output voltage level as compared to conventional SCMLI. However, for achieving the partial charging of capacitors, extra switches and drivers are required which increases the cost, weight and complexity of the converter structure. A SCMLI structure based on series/parallel mode of capacitors was developed by [15]. The structure requires lower number of switches as compared to conventional SCMLI. However, the structure requires significantly large number of switches and capacitors when high level output voltage is needed to generate. Further, the structure sustains high total standing voltage (*TSV*) due to the presence of H-bridge circuit at the load end. A novel SC basic unit consisting of two active switches, one capacitor and one diode was proposed in [16]. Furthermore, two cascaded MLI structures based on the basic units were developed. However, the structures require isolated DC sources and H-bridge circuit. In [17], the authors proposed a SCMLI with an objective to reduce the number of required switches as compared to [16]. However, the structure needs large number of diodes for generating high level output voltage. Further, the structure uses H-bridge as polarity generation circuit. Based on the same SC basic unit as proposed in [16], the authors of [18] proposed a cascaded SCMLI structure for high frequency AC applications. However, the structure uses isolated DC source and H-bridge circuit for each module. An extended step-up SCMLI structure based on developed H-bridge and SC basic units as proposed in [16] was implemented by the authors of [19]. The structure needs large number of switches, capacitors and diodes for generating a high quality output voltage waveform. Furthermore, the number of conducting switches in the charging path of capacitors increases significantly as the output voltage level increases. This degrades the capacitor voltages and decreases the quality of the output voltage waveform. A novel switched capacitor converter (SCC) structure was developed in [20]. The structure can realize the multistep output voltage by charging and discharging the capacitors with respect to the input source. However, the SCC structure requires an H-bridge circuit at the load end. Further, with increasing the output voltage level, the structure requires significantly large number of switches and capacitors. A cascaded SCMLI structure was developed by the authors of [21]. The developed structure does not use H-bridge circuit. However, each module of the structure requires two isolated DC sources. This enhances the number of DC source requirement as the output voltage level increases. A quasi-resonant SCMLI for high-frequency AC micro-grid application was proposed in [22]. The objective of developing this topology is to limit the capacitor charging current. However, the structure does not possess the boosting capability and requires large number of switches and capacitors for producing high quality output voltage waveform. In addition, the structure needs H-bridge circuit. Based on the SC technique, a novel symmetric SCMLI structure was proposed by the authors of [23]. The structure eliminates the H-bridge circuit to reduce the *TSV*. However, the number of conducting switches in the capacitor charging path increases significantly as the output voltage level enhances. By integrating SC technique in hybrid MLI, a novel SCMLI structure was developed in [24]. The structure requires lesser switches as compared to other structures for generating same output voltage level. However, the number of conducting switches in the capacitor charging current path, required capacitors and diodes enhance significantly as the output voltage level increases. A cascaded MLI based on single stage SC modules was proposed by the author of [25]. The structure eliminates the H-bridge circuit. The structure sustains lower *TSV* as compared to others. However, the structure requires significantly large number of switches, capacitors and DC sources for generating high level output voltage.

In this paper, a novel SCMLI structure based on three equal magnitude non-isolated DC sources is presented. The structure possesses the self-capacitor voltage balancing and output voltage boosting abilities. The proposed structure uses lesser number of switches, drivers and capacitors as compared to other SCMLI topologies. The organization of this paper is as follows: section 2 presents the circuit, operating principle and important features of proposed 15 level SCMLI. The generalized (extended) structure of proposed SCMLI is developed in section 3. The analysis of voltage and current stresses of switches are discussed in

section 4. Section 5 presents the detail procedure of selection of capacitance for utilized capacitors in 15 level SCMLI. An extensive comparison study of proposed topology with other recently published SCMLI topologies is discussed in section 6. The experimental study of proposed 15 level SCMLI is presented in section 7. The conclusions are provided in section 8.

## 2. Proposed 15 level SCMLI structure

Figure 1 shows the proposed 15 level SCMLI structure. It consists of 2 sub-modules: sub-module 1 (SM 1) and sub-module 2 (SM 2). SM 1 comprises of 3 equal DC sources ($V_{dc,U}$, $V_{dc,M}$ and $V_{dc,L}$), 6 unidirectional switches ($S_p$, $S_p$', $S_{11}$, $S_{11}$', $S_{12}$ and $S_{12}$'), 2 bi-directional switches ($S_{1b}$ and $S_{1b}$') and 1 capacitor ($C_1$). SM 2 comprises of 4 unidirectional switches ($S_{21}$, $S_{21}$', $S_{22}$ and $S_{22}$'), 2 bidirectional switches ($S_{2b}$ and $S_{2b}$') and 1 capacitor ($C_2$). When the switches $S_{1b}$ and $S_{1b}$' are ON in SM 1, the capacitor $C_1$ is connected in parallel with the supplies as shown in figure 2(a) and accumulates energy from the supplies. Under this circuit condition, $C_1$ is charged to ($V_{dc,U} + V_{dc,M} + V_{dc,L}=3V_{dc}$) voltage level. Similarly, when the switches $S_{2b}$ and $S_{2b}$' are ON in SM 2, the capacitor $C_2$ is connected in parallel with the supplies as depicted in figure 2(b). Under this circuit condition, the capacitor $C_2$ stores energy from the supplies and is charged to ($V_{dc,U} + V_{dc,M} + V_{dc,L}=3V_{dc}$) voltage level.

With these capacitor voltages, the proposed structure is able to produce 15 output voltage levels (7 positive voltage levels, 7 negative voltage levels and 1 zero voltage level). Figure 3 shows the equivalent circuits and current flow paths corresponding to different output voltage levels. In figure 3, the load current flow path ($i_L$) is shown in red line whereas the charging current path for the capacitors $C_1$ and $C_2$ (i.e. $i_{C1}$ and $i_{C2}$) are shown in yellow and blue line respectively. Moreover, table 1 shows the list of ON switches and the state of capacitors for each output voltage level. In table 1, C, D and NC stand for charging, discharging and not-connected mode of the utilized capacitors.

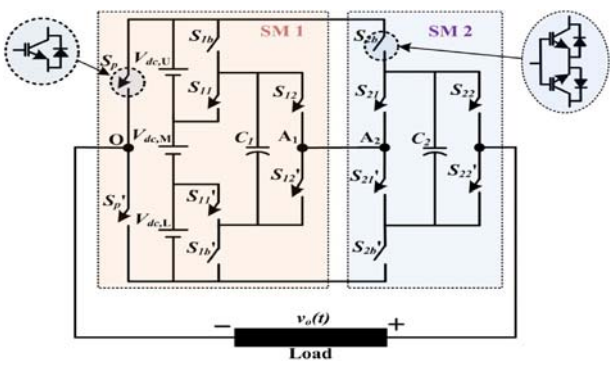


**Figure 1.** Proposed SCMLI structure.

$+1V_{dc}$ voltage level is realized by connecting the supply voltage $V_{dc,L}$ ($V_{dc}$) directly to the load. This can be achieved by turning ON either the switches $S_p$', $S_{11}$', $S_{12}$', $S_{21}$', $S_{22}$' or $S_p$', $S_{11}$', $S_{12}$', $S_{21}$, $S_{22}$ as listed in table 1. Figure 3(a) shows the equivalent circuit and current flow path for $+1V_{dc}$ voltage level when the switches $S_p$', $S_{11}$', $S_{12}$', $S_{21}$', $S_{22}$' are turned ON. Similarly, $-1V_{dc}$ voltage level is developed by connecting $V_{dc,U}$ ($V_{dc}$) directly to the load. As listed in table 1, when the switches $S_p$, $S_{11}$, $S_{12}$, $S_{21}$, $S_{22}$ or $S_p$, $S_{11}$, $S_{12}$, $S_{21}$', $S_{22}$' are turned ON, $-1V_{dc}$ voltage level is produced to the load. The equivalent circuit and current flow path for $-1V_{dc}$ voltage level are depicted in figure 3(b) when the switches $S_p$, $S_{11}$, $S_{12}$, $S_{21}$, $S_{22}$ are in ON state. It can be noted that during these voltage levels, the capacitors $C_1$ and $C_2$ are in NC mode as shown in table 1.

During $\pm 3V_{dc}$ voltage levels, the capacitors $C_1$ and $C_2$ enter into the charging state. Based on table 1 and figure 3(e), it is observed that the capacitor $C_1$ and $C_2$ are connected in parallel with the supply voltages whenever the switches $S_p$', $S_{2b}$, $S_{22}$, $S_{1b}$, $S_{1b}$', $S_{2b}$' are turned ON. Furthermore, the summation of all the supplies (i.e., $V_{dc,L} + V_{dc,M} + V_{dc,U} =3V_{dc}$) is connected across the load terminals and $+3V_{dc}$ voltage level is produced to the load. During this voltage level, the capacitors store energy from supplies and are charged to $3V_{dc}$ voltage level. Similarly, $-3V_{dc}$ voltage level is generated to the load whenever the switches $S_p$, $S_{2b}$', $S_{22}$', $S_{1b}$, $S_{1b}$', $S_{2b}$ are turned ON. With this switching state, the capacitors $C_1$ and $C_2$ are connected in parallel with the supplies and are charged to $3V_{dc}$ voltage level as shown in figure 3(f). Hence, it can be observed that the proposed structure has the ability to generate the desire voltage level as well as charge the capacitors at the desire voltage without incorporating any auxiliary circuit or complex control algorithm.

Similarly, $+5V_{dc}$ voltage level is produced to the load by connecting the capacitor $C_2$ (which is already charged to $3V_{dc}$ in previous level) in series with the summation of supply voltages $V_{dc,L}$ and $V_{dc,M}$ (i.e., $V_{dc,L} + V_{dc,M}$) as shown in figure 3(i). The ON switches for this voltage level are $S_p$', $S_{11}$, $S_{12}$, $S_{21}$', $S_{22}$ as listed in table 1. Similarly, when the switches $S_p$, $S_{11}$', $S_{12}$', $S_{21}$, $S_{22}$' are turned ON, the capacitor $C_2$ is connected in series with the summation of supply voltages $V_{dc,U}$ and $V_{dc,M}$ (i.e. $V_{dc,U} + V_{dc,M}$) as shown in figure 3(j). It can be observed that during these voltage levels, the capacitor $C_2$ discharges its stored energy towards the load whereas the capacitor $C_1$ remains in NC mode as shown in table 1.

The $\pm 7V_{dc}$ voltage levels are the highest voltage levels produced by the proposed structure. During these voltage levels, both the capacitors are in discharging mode as shown in table 1. When the switches $S_p$', $S_{11}$', $S_{12}$, $S_{21}$', $S_{22}$ are turned ON, the capacitors $C_1$ and $C_2$ are connected in series with the supply voltage $V_{dc,L}$ and is appeared across the load terminals. Hence, $+7V_{dc}$ voltage level is generated to the load as depicted in figure 3(m). Similarly, $-7V_{dc}$ voltage level is produced to the load whenever the switches

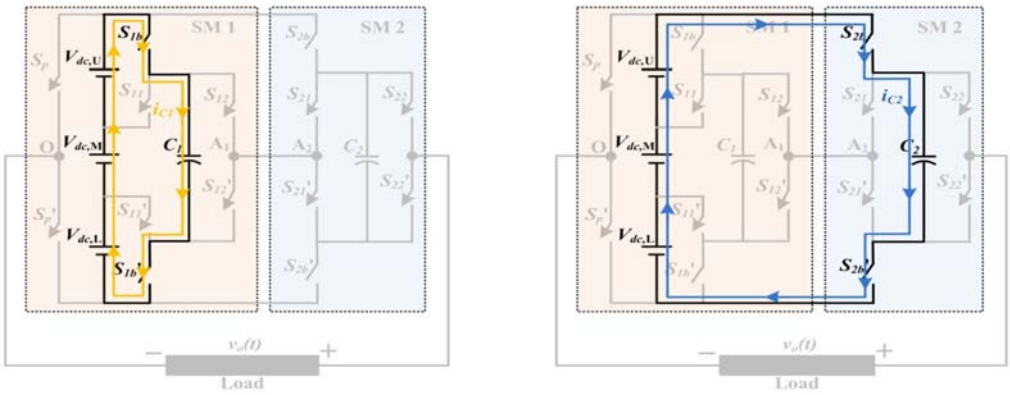


**Figure 2.** Equivalent circuit for (a) charging mode of $C_1$ and (b) charging mode of $C_2$ .

$S_p$, $S_{11}$, $S_{12}$', $S_{21}$, $S_{22}$' are turned ON. With this switching state, the capacitors $C_1$ and $C_2$ are connected in series with the supply voltage $V_{dc,U}$ as shown in figure 3(n). In a similar way, the even voltage levels can be produced.

The important features of proposed structure are as follows.

(1) The proposed structure is able to boost the output voltage by connecting the capacitors in series/parallel with respect to the input voltages. The capacitors in the structure can be charged and discharged simultaneously.

(2) The structure uses non-isolated dc sources as the input dc bus which reduces the cost of the structure with respect to that for isolated dc sources. PV arrays can be utilized as the dc sources for the proposed structure.

(3) The structure is symmetric in nature because all the dc sources are equal in magnitude and both the capacitor voltages are equal.

(4) The capacitors can enter into the charging state by turning ON the minimum number of switches which reduces the voltage drop associated with the charging path of the capacitors and hence improve the capacitor voltage profile.

(5) The proposed structure is simple and can easily be extended for generating higher voltage levels (which is discussed in next section).

(6) The structure does not use H-bridge circuit.

## 3. General structure of proposed SCMLI

This section presents the development of general structure of proposed SCMLI. Figure 4 shows the general structure of the proposed SCMLI. The structure consists of $m$ number of sub-modules (SM 1, SM 2, SM 3,….. SM m) which are connected in cascade form. SM 2 to SM m are similar to SM 2 of the proposed 15 level SCMLI whereas the SM 1 is similar to SM 1 of proposed 15 level SCMLI. All the capacitors ($C_1$, $C_2$, $C_3$, ……..,$C_m$) in the structure are charged to $3V_{dc}$ ($V_{dc,L}$+$V_{dc,M}$+$V_{dc,U}$ =$3V_{dc}$) voltage level whenever the switches $S_{1b}$, $S_{1b}$', $S_{2b}$, $S_{2b}$', $S_{3b}$, $S_{3b}$',……,$S_{mb}$, $S_{mb}$' are turned ON. With this switching state, all the capacitors are connected in parallel with the supply voltages and store energy from the supplies as presented in figure 5. As all the capacitor voltages are same (equal to $3V_{dc}$) and the input supplies are same (equal to $V_{dc}$), the general structure is a symmetric structure. Figure 6 shows the equivalent circuit of proposed structure when all the capacitors are in discharging mode.

The output voltage level ($N_L$), the number of required switches ($N_{sw}$), gate drivers ($N_{dr}$), capacitors ($N_{cap}$), maximum number of switches in the conducting path ($N_p$) for the proposed structure in terms of number of sub-modules $i$ ($i$=1, 2, 3,……m) can be expressed by (1)−(5).

$$N_L = 6i + 3 \tag{1}$$

$$N_{sw} = 8i + 2 \tag{2}$$

$$N_{dr} = 6i + 2 \tag{3}$$

$$N_{cap} = i \tag{4}$$

$$N_p = 2i + 1 \tag{5}$$

## 4. Analysis of voltage and current stresses of switches

The analysis of voltage and current stresses of switches are presented in this section. In the general form of proposed structure, all the capacitors are charged to equal voltage level, hence the stress voltage for the switches $S_{i1}$, $S_{i1}$', $S_{i2}$, $S_{i2}$' ($i$ = 2, 3, 4,……..,$m$) are same as presented by (6).

$$V_{Si1} = V'_{Si1} = V_{Si2} = V'_{Si2} = 3V_{dc} \quad \text{where } i = 2, 3, 4, \ldots, m \tag{6}$$

The maximum stress voltage for bidirectional switches $S_{ib}$, $S_{ib}$' ($i$ = 2, 3, 4,……..,$m$) of SM 2 to SM m can be represented by (7).

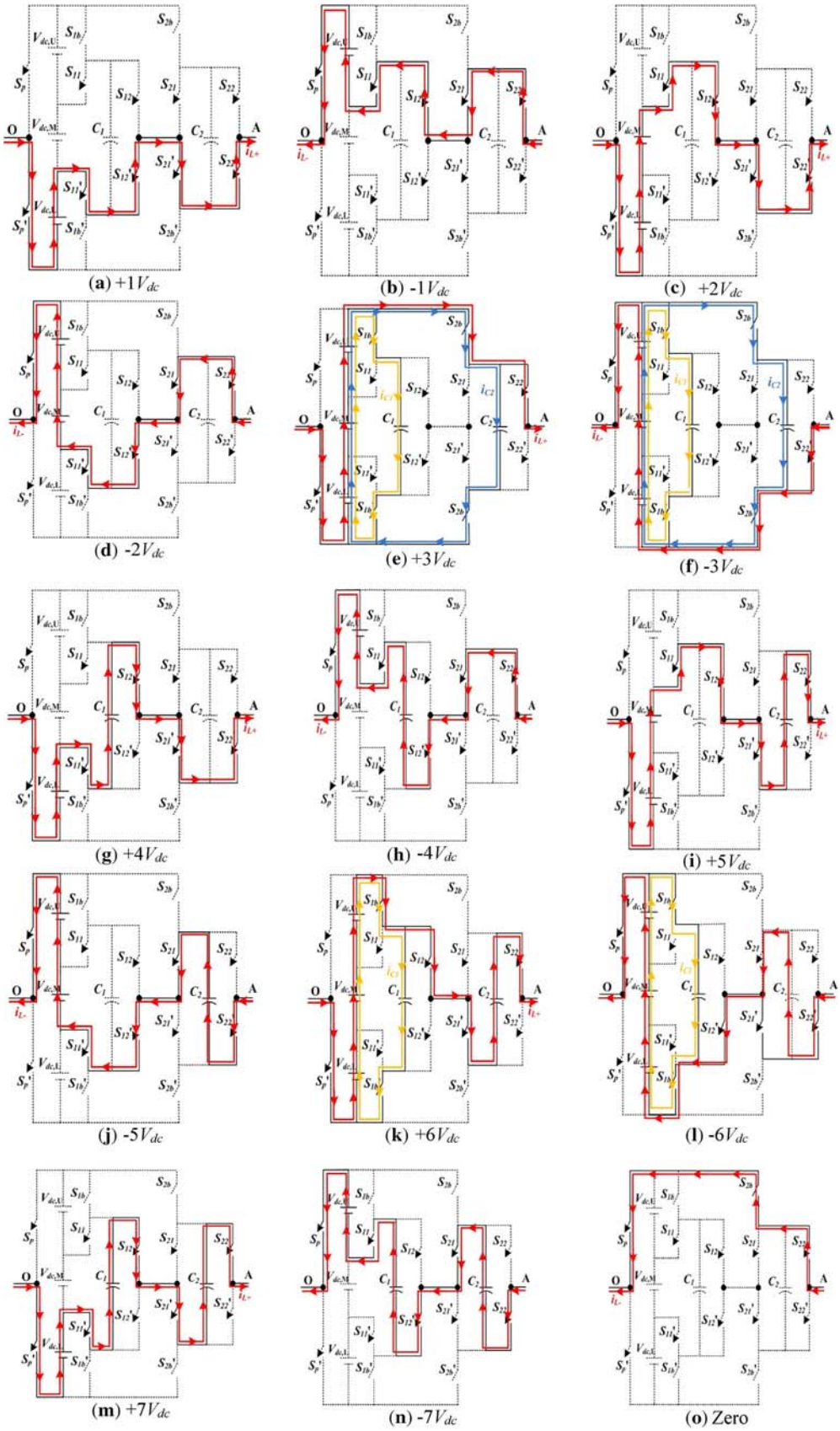


**Figure 3.** Equivalent circuit and current flow path for different voltage levels of proposed SCMLI structure.

**Table 1.** List of ON switches and capacitor states for different voltage levels produced by the proposed 15 level SCMLI.

| Output voltage level | ON switches | Capacitor states $C_1$ | Capacitor states $C_2$ |
|---|---|---|---|
| $+7V_{dc}$ | $S_p$', $S_{11}$', $S_{12}$, $S_{21}$', $S_{22}$ | D | D |
| $+6V_{dc}$ | $S_p$', $S_{1b}$, $S_{12}$, $S_{21}$', $S_{22}$, $S_{1b}$' | C | D |
| $+5V_{dc}$ | $S_p$', $S_{11}$, $S_{12}$, $S_{21}$', $S_{22}$ | NC | D |
| $+4V_{dc}$ | $S_p$', $S_{11}$', $S_{12}$, $S_{21}$', $S_{22}$' | D | NC |
| | $S_p$', $S_{11}$', $S_{12}$, $S_{21}$, $S_{22}$ | D | NC |
| $+3V_{dc}$ | $S_p$', $S_{2b}$, $S_{22}$, $S_{1b}$, $S_{1b}$', $S_{2b}$' | C | C |
| $+2V_{dc}$ | $S_p$', $S_{11}$, $S_{12}$, $S_{21}$', $S_{22}$' | NC | NC |
| | $S_p$', $S_{11}$, $S_{12}$, $S_{21}$, $S_{22}$ | NC | NC |
| $+1V_{dc}$ | $S_p$', $S_{11}$', $S_{12}$', $S_{21}$', $S_{22}$' | NC | NC |
| | $S_p$', $S_{11}$', $S_{12}$', $S_{21}$, $S_{22}$ | NC | NC |
| 0 | $S_p$', $S_2$', $S_{22}$' | NC | NC |
| | $S_p$, $S_2$, $S_{22}$ | NC | NC |
| $-1V_{dc}$ | $S_p$, $S_{11}$, $S_{12}$, $S_{21}$, $S_{22}$ | NC | NC |
| | $S_p$, $S_{11}$, $S_{12}$, $S_{21}$', $S_{22}$' | NC | NC |
| $-2V_{dc}$ | $S_p$, $S_{11}$', $S_{12}$', $S_{21}$, $S_{22}$ | NC | NC |
| | $S_p$, $S_{11}$', $S_{12}$', $S_{21}$', $S_{22}$' | NC | NC |
| $-3V_{dc}$ | $S_p$, $S_{2b}$', $S_{22}$', $S_{1b}$, $S_{1b}$', $S_{2b}$ | C | C |
| $-4V_{dc}$ | $S_p$, $S_{11}$, $S_{12}$', $S_{21}$, $S_{22}$ | D | NC |
| | $S_p$, $S_{11}$, $S_{12}$', $S_{21}$', $S_{22}$' | D | NC |
| $-5V_{dc}$ | $S_p$, $S_{11}$', $S_{12}$', $S_{21}$, $S_{22}$' | NC | D |
| $-6V_{dc}$ | $S_p$, $S_{1b}$', $S_{12}$', $S_{21}$, $S_{22}$', $S_{1b}$ | C | D |
| $-7V_{dc}$ | $S_p$, $S_{11}$, $S_{12}$', $S_{21}$, $S_{22}$' | D | D |

$$V_{Sib} = V'_{Sib} = [(3 \times i) - 2]V_{dc} \quad \text{where } i = 2, 3, 4, \ldots, m \tag{7}$$

For SM 1, the maximum stress voltage of different switches are given by (8)-(10)

$$V_{Sp} = V'_{Sp} = V_{S12} = V'_{S12} = 3V_{dc} \tag{8}$$

$$V_{S11} = V'_{S11} = 2V_{dc} \tag{9}$$

$$V_{S1b} = V'_{S1b} = V_{dc} \tag{10}$$

*TSV* of SM 1 ($i = 1$) is $18V_{dc}$. The *TSV* of the proposed structure when the number of connected modules is more than 1, can be expressed by (11).

$$TSV = [(18 \times i) + 2]V_{dc} \quad \text{where } i = 2, 3, 4, \ldots, m \tag{11}$$

The current stress for the switches $S_{ib}$, $S_{ib}$' ($i$=1, 3, 4,……..,$m$) are equal to the summation of load current and capacitor charging current. Under charging mode of capacitors, the equivalent circuit of the proposed structure can be redrawn by figure 7. From this figure, the maximum current flowing through the bidirectional switches can be represented by (12). Where $V_{Ci}$ is the voltage across $i^{th}$ capacitor, $V_{di}$ is the forward voltage drop in the antiparallel diode associated with the $i^{th}$ bidirectional switch, $r_{oi}$ is the summation of on state resistance of the switch and the resistance of antiparallel diode, $r_{ci}$ is the ESR of $i^{th}$ capacitor. From figures 3 and 6, it can be noted that the maximum current stress of the other switches are lower than/equal to the maximum load current of the circuit.

$$i_{Sib} = i'_{Sib} = \frac{3V_{dc} - V_{Ci} - 2V_{di}}{2r_{oi} + r_{ci}} + i_L \quad \text{where } i = 1, 2, 3, \ldots, m \tag{12}$$

## 5. Selection procedure for switched capacitor

This section presents the selection procedure for SCs in the proposed SCMLI structure. The capacitance value for the SCs will determine the voltage ripple across the capacitors. When the capacitors are in discharging mode, the charge stored in the capacitors discharge towards the load. Consequently, the voltage across the capacitors will drop from their previous value.

For evaluating the capacitance for SCs, it is required to find the longest discharging time ((LDT) for SCs over a fundamental output cycle. As the switching of positive and

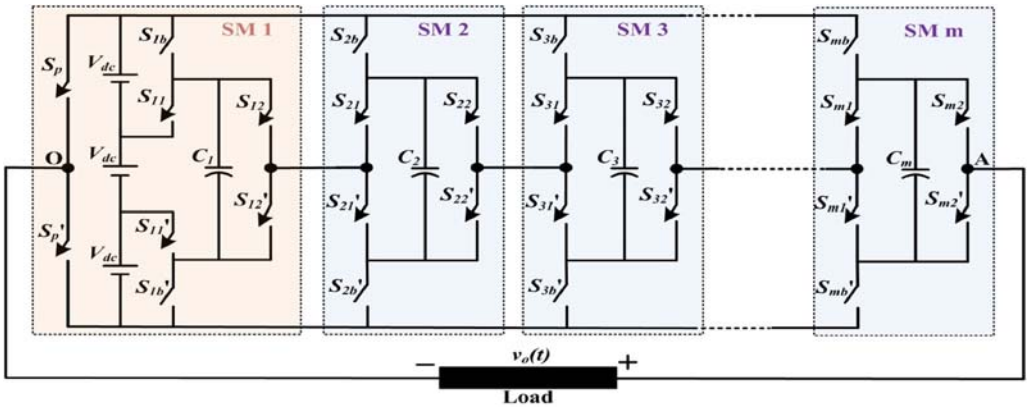


**Figure 4.** General structure of proposed SCMLI.

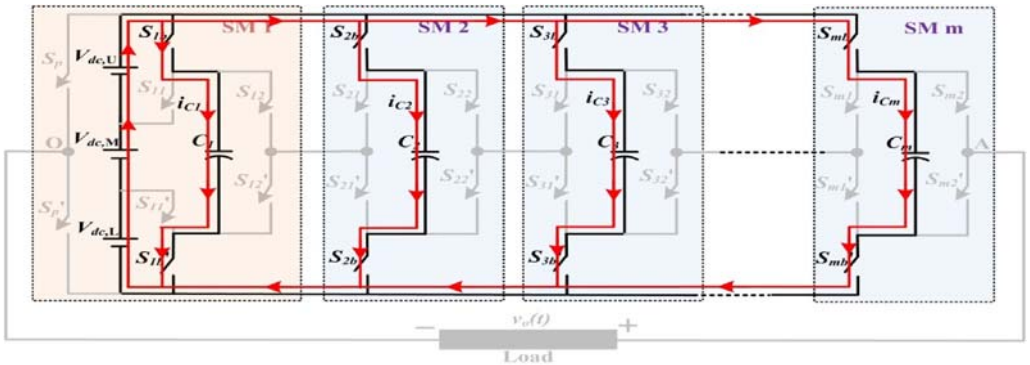


**Figure 5.** Equivalent circuit for charging mode of all the capacitors.

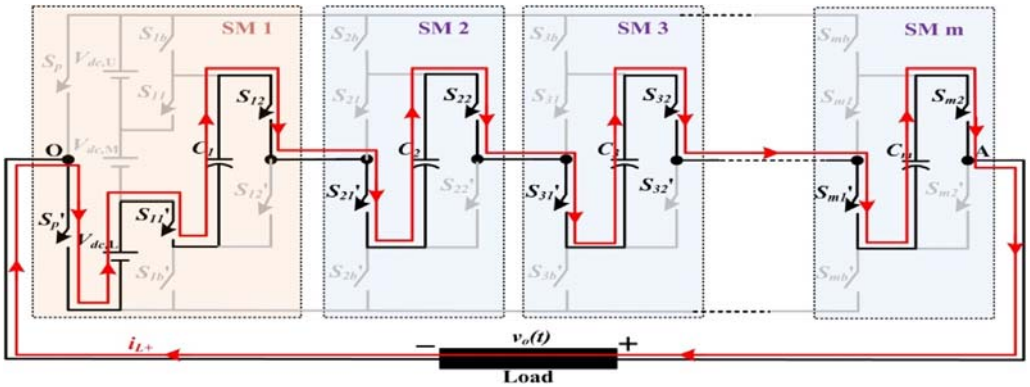


**Figure 6.** Equivalent circuit for discharging mode of all the capacitors.

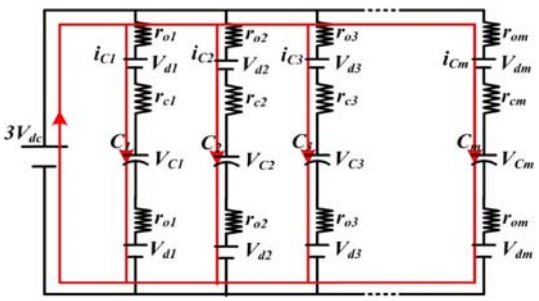

**Figure 7.** Equivalent circuit for charging mode of all the capacitors.

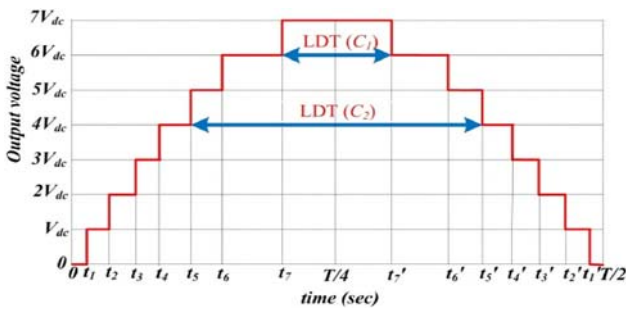


**Figure 8.** LDT of SCs in proposed SCMLI.

negative cycles are symmetrical to each other, figure 8 shows the LDT for SCs for proposed SCMLI for fundamental switching frequency scheme.

$$q_{C1} = 2 \times \int_{t_7}^{T/4} i_L(t)dt \tag{13}$$

$$q_{C2} = 2 \times \int_{t_5}^{T/4} i_L(t)dt \tag{14}$$

$$C_{1opt} \geq \frac{q_{C1}}{k \times 3V_{dc}} \tag{15}$$

$$C_{2opt} \geq \frac{q_{C2}}{k \times 3V_{dc}} \tag{16}$$

The maximum amount of charge discharged during the LDT of SCMLI are presented in (13) and (14) respectively. Where $i_L(t)$ is the load current. The optimum capacitance value for SCs for proposed 15 level SCMLI are evaluated by (15) and (16). Where $k$ is the capacitor ripple voltage for $C_1$ and $C_2$.

$$i_L(t) = \begin{cases} \frac{5V_{dc}}{R_L} & \text{for } t_5 \leq t < t_6 \\ \frac{6V_{dc}}{R_L} & \text{for } t_6 \leq t < t_7 \\ \frac{7V_{dc}}{R_L} & \text{for } t_7 \leq t < \frac{T}{4} \end{cases} \tag{17}$$

$$\left.\begin{aligned} t_5 &= \frac{\mathrm{Sin}^{-1}\left(\frac{9}{14}\right)}{2\pi f}\sec \\ t_6 &= \frac{\mathrm{Sin}^{-1}\left(\frac{11}{14}\right)}{2\pi f}\sec \\ t_7 &= \frac{\mathrm{Sin}^{-1}\left(\frac{13}{14}\right)}{2\pi f}\sec \end{aligned}\right\} \tag{18}$$

Under resistive load condition, the load current during the LDT of capacitors can be represented by (17). Further, the time $t_5$, $t_6$ and $t_7$ can be found out by (18) [26]. $T$ is the time period of output fundamental cycle. The optimum value of SCs for resistive load condition can be represented by (19).

$$\left.\begin{aligned} C_{1opt} &\geq \frac{1.77}{2 \times \pi \times f \times R_L \times k} \\ C_{2opt} &\geq \frac{3.61}{2 \times \pi \times f \times R_L \times k} \end{aligned}\right\} \tag{19}$$

## 6. Comparison study

This section presents the comparison study of the proposed SCMLI structure with other recently developed SCMLI structures. The selected structures are a SCMLI using series/parallel conversion with inductive load [15], a cascaded SCMLI structure for high frequency AC distribution [18], a generalized SCMLI structure using novel SCC [20], a new cascaded SCMLI based on SCCs [21], a quasi-resonant SCMLI structure [22], a self-balanced step-up MLI [23], Symmetric/asymmetric hybrid MLIs integrating SC techniques [24] and single stage SC module for cascaded MLI [25].

Figure 9(a) presents the variation of the required semiconductor devices (switches plus diodes) with output voltage level ($N_L$) for proposed as well as the suggested structures. It can be observed that the proposed structure requires least number of semiconductor devices for realizing a $N_L$ as compared to others. The variation of the required driver circuits ($N_{Dr}$) with $N_L$ is depicted in figure 9(b). The proposed structure requires same drivers as that for the topology presented in [22]. However, the proposed structure requires lesser drivers as compared to the other structures. The proposed structure requires least number of capacitors ($N_{Cap}$) for generating a $N_L$ as compared to others as presented in figure 9(c). Figure 9(d) shows the comparison of the required DC sources ($N_S$) for realizing a $N_L$ among the proposed and suggested topologies. It can be observed that the proposed structure requires 3 DC sources whereas the DC source requirement for the structures presented in [18], [21] and [25] increases significantly as the $N_L$ increases. However, the proposed structure requires more number of DC sources as compared to the topologies presented in [15], [20] and [22–24].

The variation of the maximum number of switches conducting in current path ($N_p$) with respect to $N_L$ for proposed and the suggested topologies is shown in figure 9(e). From this figure, it can be noted that the proposed structure requires to conduct the minimum $N_p$ as compared to others. This improves the output voltage quality as compared to others. Further, the proposed structure conducts minimum number of switches (only bidirectional switches) for charging all the capacitors as compared to the other structures. This improves the capacitor voltage profile as well as the quality of the output voltage waveform. The *TSV* of all the structures for producing a $N_L$ is shown in figure 9(f). It can be observed that the proposed structure sustains lower $TSV/V_{dc}$ as compared to the topology presented in [20] and [22].

For a fair comparison among the proposed and suggested topologies, the overall cost of the structures are compared. The *CF* consists of two parts as shown in (20) [20, 21]. The part-I represents the cost component based on the number of required component for generating a specific number of output voltage level ($N_L$). This part is the summation of the number of switch requirement ($N_{sw}$), driver circuits requirement ($N_{dr}$), capacitor requirement ($N_{cap}$), power diodes requirement ($N_{dio}$) and the source requirement ($N_s$) for generating a specific $N_L$.

The part-II of *CF* represents the cost component due to the total standing voltage (*TSV*) of the structure. The *TSV* of the structure means the summation of maximum blocking voltages of all the utilized power switches in the structure. For example, the proposed 15 level structure has a *TSV* of $38V_{dc}$ (see equation (11). *TSV* of the inverter represents the voltage rating of the switches. *TSV* is converted into per unit *TSV* by dividing the *TSV* by the maximum output voltage generated by the inverter structure. As based on the applications such as low voltage or high voltage applications, *TSV* value of inverter will be different. So a weight-age factor $\beta$ is multiplied with the per unit *TSV* in the *CF*. If $\beta$ is less than 1, then the *CF* has more priority on the component cost (that is the number of component requirement) than the *TSV*. If the proposed inverter has lower *CF* value for $\beta$ lower than 1 as compared to other structures, the proposed inverter is cost effective for low voltage applications.

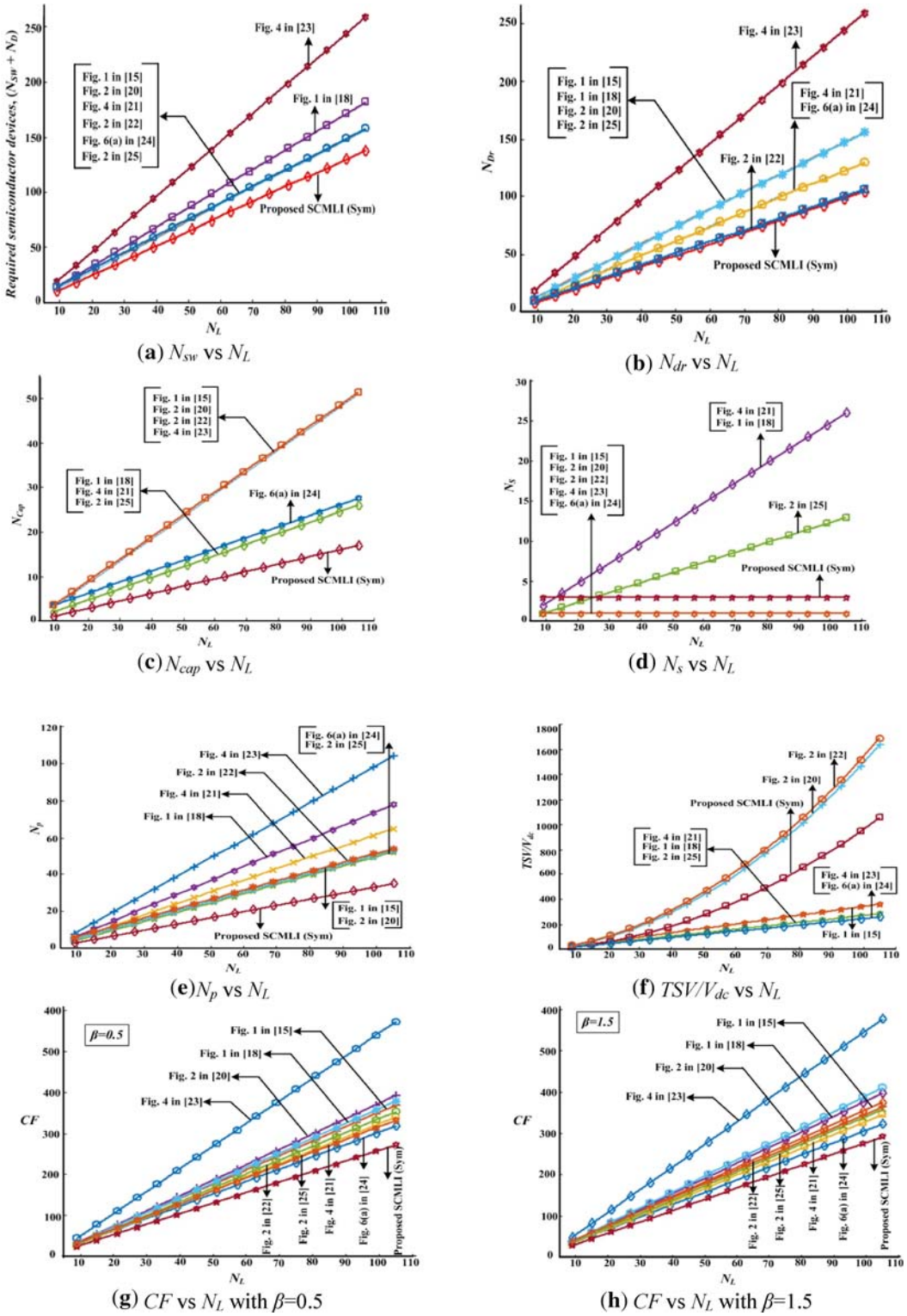


**Figure 9.** Comparison study of proposed structure with other structures.

$$CF = (N_{sw} + N_{dr} + N_{cap} + N_{dio} + N_s + \beta \frac{TSV}{v_{o\max}}) \quad (20)$$

Part-I Part-II

If β is greater than 1, then the *CF* has more priority on the *TSV* of the structure than the component cost. If the inverter structure has lower *CF* for β greater than 1 as compared to other structures, then the inverter is suitable for high voltage applications.

As for a particular voltage level generation, the different topologies requires different number of components and sources, and are sustained by different *TSV*, *CF* is evaluated as a function of number of levels as depicted in figure 9(g) and figure 9(h) for $\beta$=0.5 and $\beta$=1.5, respectively. From these figures, it can be observed that proposed SCMLI provides the lowest *CF* as compared to other structures for both the values of $\beta$. Hence the proposed structure is cost effective as compared to other structures for low as well as high voltage applications.

## 7. Experimental studies

To prove the operating principle and performances of the proposed SCMLI structure, extensive experimental studies are conducted on proposed 15 level SCMLI with *R-L*, *L*, *R* and sudden step change load condition. Figure 10 depicts the experimental testset-up. The switching pulses considering fundamental switching frequency scheme are generated by dSPACE (DS-1104) controller. IRF 640 (n-channel MOSFET) has been selected as the switching device. IR2110 has been employed as gate driver IC.

The proposed 15 level SCMLI is loaded with *R*=110 Ω and *L*=50 mH load. The magnitude of DC sources are selected as 27 V ($V_{dc}$=27 V). For this load condition, the load phase angle $\phi$ = 8.12 degree. The optimum capacitance value of $C_1$ for 2% voltage ripple is selected as 2500 μF. Similarly, for 3% voltage ripple, the selected optimum capacitance of $C_2$ is 3000 μF. Figure 11(a) shows the inverter output voltage and output current under this load condition. It is obvious that the generated output voltage has 15 voltage levels. Further, the output current is near sinusoidal due to the inductive nature of the load.

The FFT analysis of load voltage shows that THD and the magnitude of peak value of fundamental output voltage are 6% and 189 V, respectively. Similarly, the FFT analysis of output current shows that THD and the peak magnitude of fundament load current are 4% and 1.65 A, respectively. The output power of the inverter under this load condition is 154 W. The total losses of the inverter is 14.7 W (conduction losses =13.7 W, ripple losses=1 W and switching losses= 20 mW). The efficiency of the inverter structure is 91.3%.

Under this load condition, the capacitor voltages are shown in figure 11(b). From this figure, the experimental capacitor voltage for $C_1$ and $C_2$ are 78 V and 74 V, respectively. The voltage ripple for $C_1$ and $C_2$ are 1.5 V and 2.4 V, respectively.

The stress voltage for the bidirectional switches $S_{1b}$ and $S_{2b}$ for the proposed structure are shown in figure 12(a). It can be observed that the maximum stress voltage for $S_{1b}$ is equal to 27 V whereas the stress voltage for $S_{2b}$ is equal to 100 V. Stress voltage for the switches $S_{12}$ and $S_{21}$ are shown in figure 12(b). Further, the stress voltage for the switches $S_p$ and $S_{22}$ are depicted in figure 12(c). It can be observed that the maximum stress voltage for $S_{12}$, $S_{21}$, $S_p$ and $S_{22}$ are within 80 V.

The proposed 15 level inverter is tested for inductive load of 275 mH. For this experimental study, the magnitude of DC sources are selected as 20 V each. The output voltage and current waveforms for inductive load condition are shown in figure 13(a). From this figure, it can be observed that the output current is lagging near about 90° with respect to the output voltage waveform.

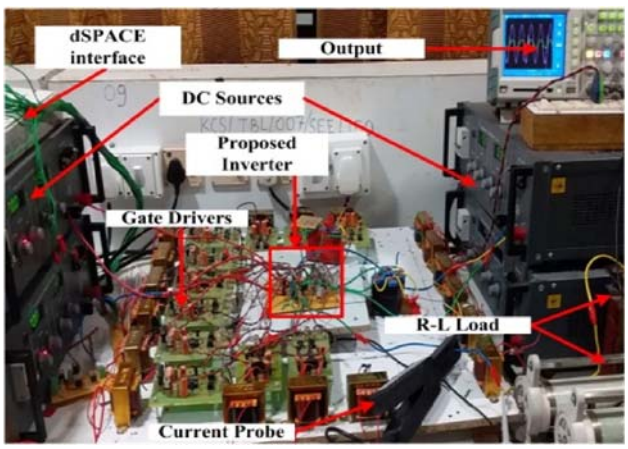


**Figure 10.** Experimental test set-up for proposed 15 level SCMLI.

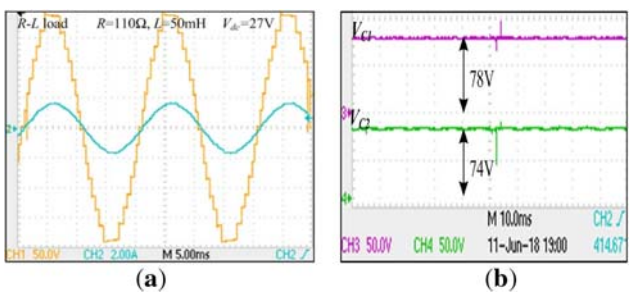


**Figure 11.** Figure presents **(a)** output voltage (50 V/div) and current (2A/div) waveforms, **(b)** capacitor voltages $V_{C1}$ (50 V/div) and $V_{C2}$(50 v/div) under *R-L* (*R*=110 Ω, *L*=50 mH) load condition.

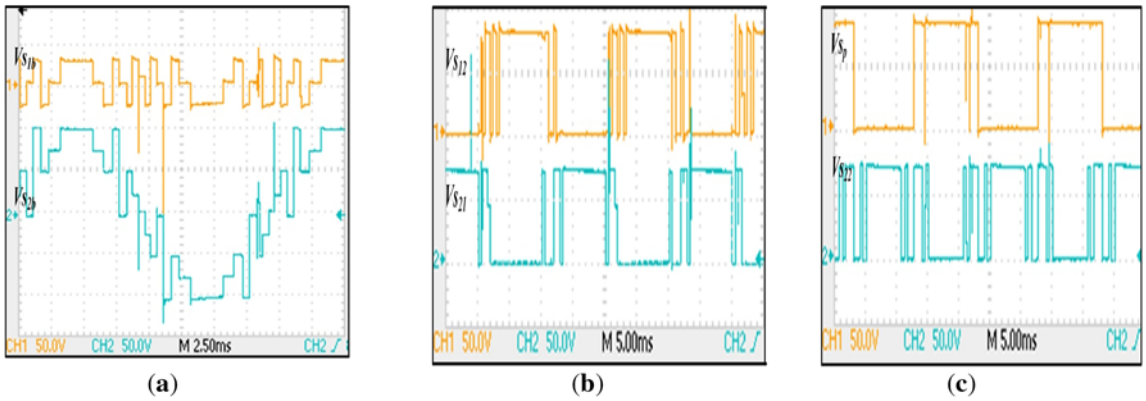


**Figure 12.** Figure presents stress voltage (50 V/div) for the switches **(a)** $S_{1b}$ and $S_{2b}$, **(b)** $S_{12}$ and $S_{21}$, and **(c)** $S_p$ and $S_{22}$ .

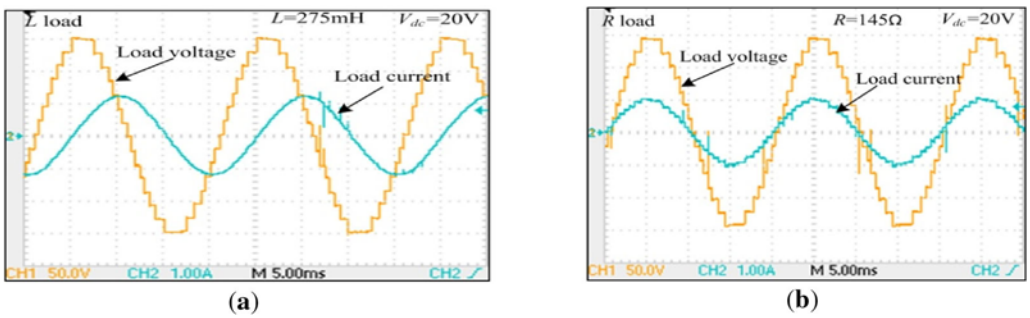


**Figure 13.** Figure presents **(a)** load voltage (50 V/div) and current (1 A/div) for *L* load (*L*=275 mH) and **(b)** load voltage (50 V/div) and current (1 A/div) for *R* load (*R*=145 Ω) for proposed 15 level SCMLI structure.

With input supply voltages of 20 V each, the proposed inverter is tested for resistive load (*R*) condition. The selected *R* value is 145 Ω. The output voltage and current waveforms for this load condition are shown in figure 13(b). From this figure, it is observed that the output current and voltage are in same phase.

From this experimental study, it can be concluded that the proposed structure is able to work for *R-L*, *L* and *R* load conditions.

## 8. Conclusions

In this paper, a novel SCMLI structure has been presented. The structure has the self capacitor voltage balancing and output voltage boosting abilities. The structure is based on 3 non-isolated equal DC sources. The extended version of proposed structure has been developed. Further, the voltage and current stresses of switches have been discussed. An extensive comparison study shows that the proposed structure requires lesser component to realize a output voltage level as compared to other structures. Further, overall cost of all the structures has been compared based on a *CF*. It has been observed that the proposed structure is more cost effective than others. An extensive experimental study of 15 level proposed structure shows the effectiveness of the proposed structure for different load conditions. The proposed structure is suitable for renewable energy conversion systems and motor drive applications.

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