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High slew rate and low output resistance class-AB flipped voltage follower cell with increased current driving capability

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Abstract. The paper proposes a class-AB flipped voltage follower (FVF) cell, in which the bulk-driven transistor is used as an input transistor with a replica-biased scheme to eliminate the DC level shift while a cascoding transistor is used to reduce the output resistance. The proposed FVF cell has several advantages such as low output resistance, approximately unity voltage gain, high symmetrical slew rate, high current sourcing capability, high current sinking capability and wide bandwidth. The proposed FVF cell has been simulated in Cadence Virtuoso Analog Design Environment using BSIM3v3 180 nm CMOS technology with a power supply voltage of 1.2 V.

Keywords. Bulk-driven; CMOS; flipped voltage follower; output resistance; slew rate.

1. Introduction

The increasing demand of less weight and longer battery life for portable electronic equipments has motivated the circuit designers to design analog integrated circuits with low supply voltage and low power consumption. Voltage follower is one of the widely used basic building blocks in analog integrated circuits, where it replicates the voltage from high resistance terminal to low resistance terminal. It is used to drive large capacitive loads and low resistive loads at high speed along with minimum power consumption [1]. So, the voltage follower needs to have high input resistance, low output resistance, approximately unity voltage gain, high slew rate, wide bandwidth and low power consumption. The flipped voltage follower (FVF) cell proposed by Ramirez-Angulo *et al* [2, 3] is an improved version of the conventional voltage follower due to the negative feedback.

FVF cells can be used in place of voltage followers in various analog integrated circuits such as current mirrors, current conveyors, multipliers, differential pairs, comparators, operational transconductance amplifiers, low-dropout voltage regulators, etc. [3]. The conventional FVF cell shows asymmetrical slew rate due to its class-A behavior. Several class-AB FVF cells have been reported in the literature, each of which offers different electrical properties [4]. The output voltage of the FVF cell follows the input voltage with a DC level shift of source-gate voltage according to the relation $V_o = V_{in} + V_{SG}$. Some of the reported class-AB FVF cells show less than unity voltage gain due to DC level shift between input and output [5–7]. The class-AB version of the FVF cell that is free from the DC level shift has been proposed by Ramirez-Angulo *et al* [8]. Another class-AB FVF cell using a replica-biased scheme [9] to remove the DC level shift has been reported by Haga *et al* [10], but it does not show low enough output resistance. In view of this, the paper proposes a modified class-AB FVF cell that offers low output resistance, approximately unity voltage gain, high symmetrical slew rate, high current sourcing capability, high current sinking capability and wide bandwidth. In the proposed FVF cell, the bulk-driven transistor is used to feed the input voltage and the cascoding transistor is used to reduce the output resistance. The DC level shift is eliminated using the replica-biased scheme while preserving all the advantages offered by the proposed FVF cell.

2. Replica-biased scheme

In the bulk-driven MOS transistor, where the input is applied at the bulk terminal, the transconductance (g_{mb}) is dependent on the bulk-to-source voltage (V_{BS}). The expression of g_{mb} is given by

$$g_{mb} = \frac{\gamma\sqrt{2\beta I_D}}{2\sqrt{|2\emptyset_F + V_{BS}|}} \quad (1)$$

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where γ is the body effect coefficient, β is the small-signal transconductance parameter, I_D is the drain current and $2\emptyset_F$ is the surface potential.

Blalock *et al* [9] proposed the replica-biased scheme shown in figure 1 to overcome the dependency of g_{mb} on V_{BS}. In the circuit, PMOS transistors $M_{1\text{-}3}$ are perfectly matched and the current I_b is flowing through each transistor. The input is applied at the bulk terminals of transistors M_1 and M_2, which results in the potential difference between bulk and source terminals. The diode-connected transistor M_3 (replica of transistors M_1 and M_2) with its bulk terminal connected to source terminal is used to bias the gate terminals of transistors M_1 and M_2. Since, $V_{BS3} = 0$ and transistor M_3 is the replica of transistors $M_{1,2}$, $V_{BS1,2} = 0$.

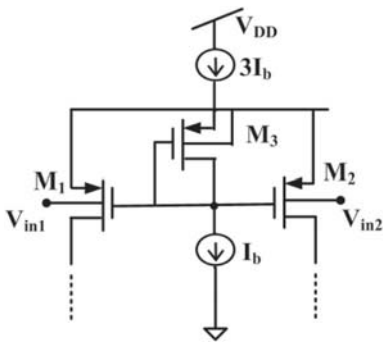

Figure 1. Replica-biased scheme [9].

3. Proposed FVF cell

The proposed FVF cell shown in figure 2 is a modification of conventional FVF cell where transistors M_1, M_3, M_4 form the conventional FVF cell. In the proposed FVF cell, a current source of $2I_b$ is realized by a diode-connected transistor M_4. The gate-to-source voltages of transistors M_4 and M_5 are equal and aspect ratios of both the transistors are kept in such a way that the transistor M_5 copies the current I_b from transistor M_4. In the proposed FVF cell, the input voltage (V_{in}) is applied at the bulk terminal and output voltage (V_o) is drawn from the source terminal of transistor M_1. The diode-connected transistor M_2 (replica of transistor M_1) used to bias the gate of transistor M_1 eliminates the DC level shift between input and output. The bulk terminal of the transistor M_2 is connected to its source terminal, which is the output node of the proposed FVF cell. Since, the transistors M_1 and M_2 are perfectly matched, gate-to-source voltages and the drain currents (I_b) of both the transistors are also equal. The bulk and source terminals of transistor M_1 becomes virtually shorted ($V_{BS1} = 0$), which results in $V_o = V_{in}$. Further, the cascoding transistor M_6 is connected between the gate terminal

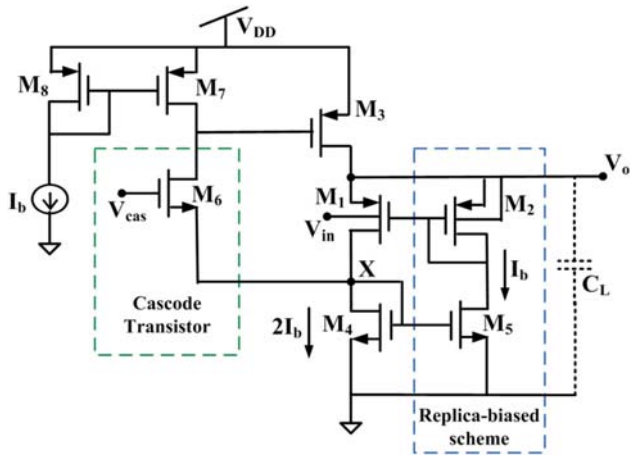

Figure 2. Proposed FVF cell.

of transistor M_3 and the drain terminal of transistor M_4 in the proposed FVF cell. This introduced transistor in the feedback path provides additional gain to the negative feedback loop, which results in low output resistance. Also, due to the inclusion of cascoding transistor in the feedback path, the proposed FVF cell has an additional advantage of very small variations at node 'X' with respect to other existing FVF configurations [10]. The transistor M_6 is biased using the current mirror formed by transistors M_7 and M_8.

3.1 *Small-signal analysis of output resistance (R_o) of proposed FVF cell*

The proposed FVF cell overcomes the limitation of output resistance of FVF cell reported in the literature [10] by introducing cascoding transistor M_6 in the feedback path. So, the small-signal equivalent model shown in figure 3 is used to analyze the output resistance (R_o) of the proposed

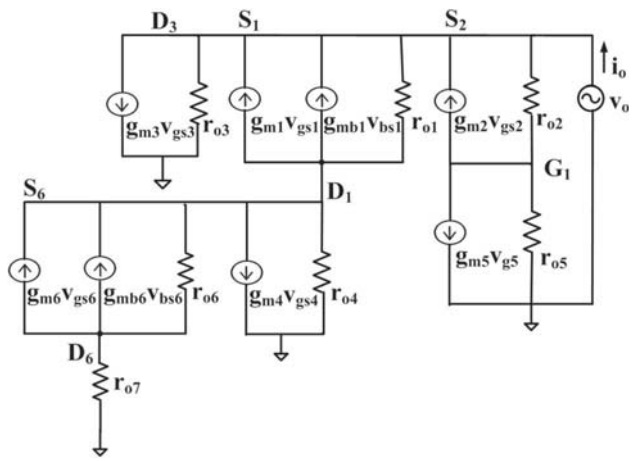

Figure 3. Small-signal equivalent model of proposed FVF cell.

FVF cell. In the model, the output terminal is connected to a voltage source (v_o) which supplies a current (i_o).

The expression of output resistance of the proposed FVF cell is given in Eq. (2).

$$R_{out} = \frac{g_{m2}g_{m4}}{g_{mb1}g_{m2}g_{m4} + g_{mb1}g_{m5}(g_{m1} + g_{m2}) + g_{mb1}g_{m2}g_{m3}(g_{m6} + g_{mb6})r_{o6}} \quad (2)$$

Also, the expression of output resistance of the FVF cell proposed in [10] is given in Eq. (3).

$$R_{out} = \frac{g_{m2}g_{m4}}{g_{mb1}g_{m2}g_{m4} + g_{mb1}g_{m5}(g_{m1} + g_{m2}) + g_{mb1}g_{m2}g_{m3}} \quad (3)$$

From Eqs. (2) and (3), it can be seen that the cascoding transistor M_6 reduces the output resistance with the addition of factor $(g_{m6} + g_{mb6})r_{o6}$ in the denominator of Eq. (2).

4. Simulation results

The proposed FVF cell is designed in Cadence Virtuoso Analog Design Environment using BSIM3v3 180 nm CMOS technology. The value of bias current (I_b) and supply voltage (V_{DD}) are selected as 8 μA and 1.2 V, respectively. The load capacitance (C_L) is chosen as 10 pF.

The transfer characteristic of the proposed FVF cell is shown in figure 4. The plot shows the variations of output voltage when the input voltage is varied in the range of 0.65 V to 1.2 V. From the plot, it is observed that output voltage follows the input voltage varying from 0.65 V to 1.2 V.

The plot of the offset voltage between the output voltage and the input voltage when the input voltage is varied from 0.65 V to 1.2 V is shown in figure 5. From the plot, it is observed that offset voltage of the proposed FVF cell is 19 mV.

The frequency response of the proposed FVF cell is shown in figure 6. From the figure, the gain and bandwidth are obtained as 0.96 and 21.34 MHz, respectively.

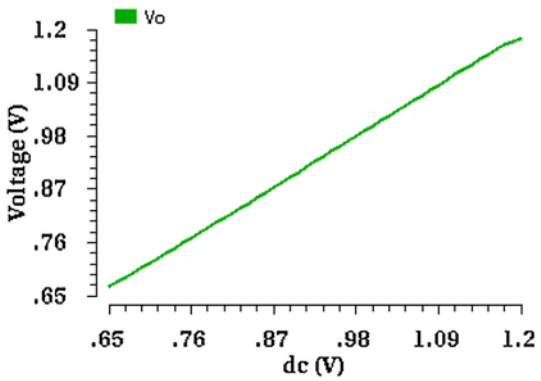

Figure 4. Transfer characteristic of proposed FVF cell.

The output resistance versus frequency plot of the proposed FVF cell is shown in figure 7. From the figure, it can be seen that the output resistance is 221 Ω for the frequency range of 1 Hz to 1 MHz.

Figure 8 shows the transient analysis for a sinusoidal input voltage with 200 mV peak-to-peak amplitude and 500 kHz frequency. From the plot, total harmonic distortion (THD) is calculated as 0.472%.

The transient analysis for a square input voltage of amplitude 0.65 V to 1.2 V at frequency of 1 MHz is shown in figure 9. The symmetrical slew rate (SR+/SR-) is

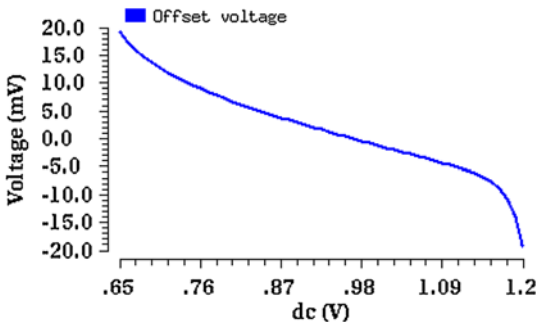

Figure 5. Offset voltage of proposed FVF cell.

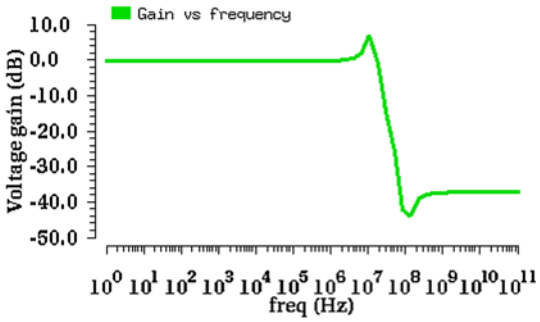

Figure 6. Frequency response of proposed FVF cell.

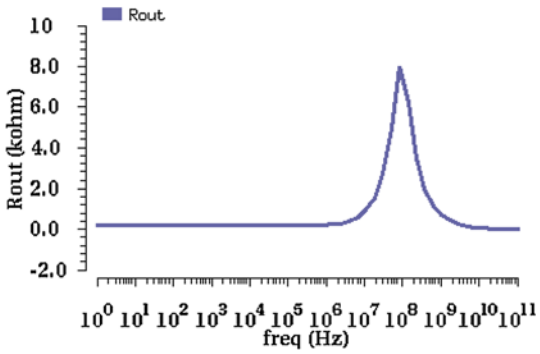

Figure 7. Output resistance of proposed FVF cell.

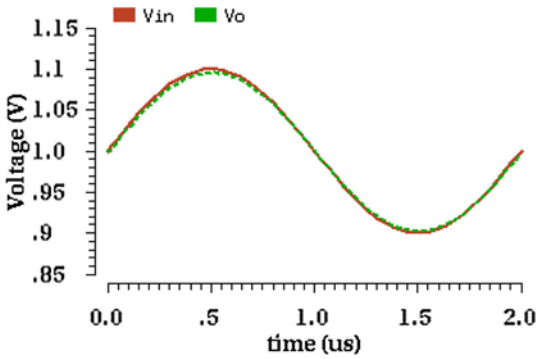

Figure 8. Transient response of proposed FVF cell for sinusoidal input voltage.

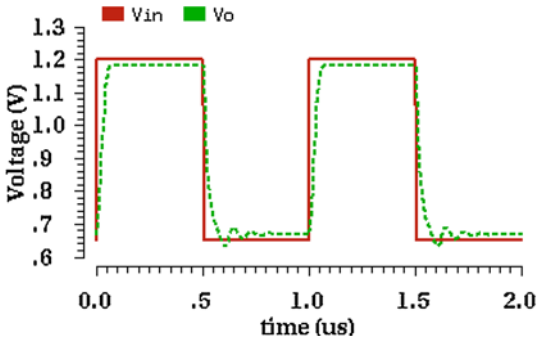

Figure 9. Transient response of proposed FVF cell for square input pulse.

observed as 14.97 V/µs/ 25.4 V/µs. The current sourcing and sinking capabilities of the proposed FVF cell shown in figure 10 are obtained as 18.71 I_b and 31.8 I_b, respectively.

Since, the bulk terminal is used to feed the input voltage, large input current and large input capacitance are not expected to avoid the bulk terminal being forward biased.

Figure 11 shows the plot of input current for the input voltage varying from 0.65 V to 1.2 V. From the plot, it is observed that input current varies from −7.2 pA to 254 fA, which cannot forward bias the bulk terminal.

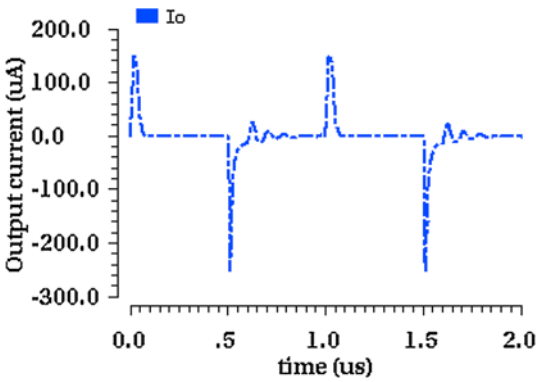

Figure 10. Current sourcing and sinking capabilities of proposed FVF cell.

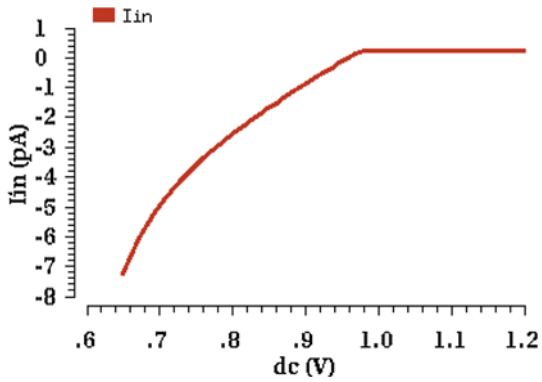

Figure 11. Input current of proposed FVF cell.

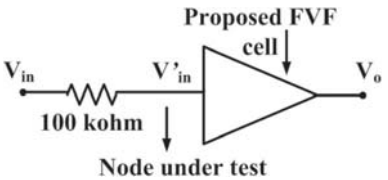

Figure 12. Simulation set up to calculate input capacitance.

To calculate the input capacitance, the set-up shown in figure 12 is considered. The plot of the rise time of voltage (V'_{in}) at node under test is shown in figure 13 when V_{in} is varied from 0.65 V to 1.2 V at 1 MHz. From figure 13, it is observed that the time constant (T = RC) for V'_{in} is 30 ns. So, the input capacitance of the proposed FVF cell is calculated as 300 fF.

The proposed FVF cell is compared with the existing FVF cell [10] in table 1. From the table, it is evident that the proposed FVF cell offers higher slew rate, wider bandwidth, lesser noise, lower THD than the existing FVF cell [10]. Also, it provides low output resistance, high current sourcing capability, high current sinking capability and approximately unity voltage gain.

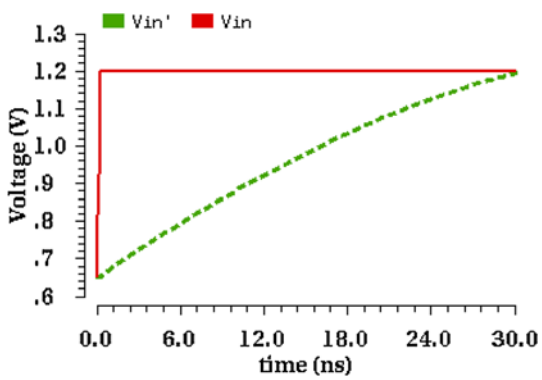

Figure 13. Rise time of voltage (V'_{in}) at node under test.

Table 1. Comparison of the proposed FVF cell with existing FVF cell.

Parameters ↓	[10]	Proposed work
Supply voltage (V)	1.2	1.2
Technology	350 nm	180 nm
Voltage range (V)	1 to 2	0.65 to 1.2
Gain	NA	0.96
Bandwidth (MHz)	2.8	21.34
R_o (Ω)	NA	221
C_L (pF)	10	10
Slew rate (V/μs)	1.9	14.97
Sourcing capability	NA	18.7 I_b
Sinking capability	NA	31.8 I_b
Noise (nV/$\sqrt{Hz}$)	880 @1 kHz	29.4 @1 kHz
PSRR+ (dB)	41.7	26.5
THD (%)	0.0747@1 kHz	0.0537@1 kHz
	0.0794@100 kHz	0.0709@100 kHz
	0.501@500 kHz	0.472@500 kHz

*NA = Not Available

5. Conclusion

The bulk-driven FVF cell with the replica-biased scheme is proposed in this paper. It uses cascoding transistor in the negative feedback path to reduce the output resistance. The advantageous performance parameters of proposed FVF cell such as free from DC level shift, low output resistance, approximately unity voltage gain, high symmetrical slew rate, high current sourcing capability, high current sinking capability and wide bandwidth, make it a suitable building block for low-power and high-speed analog integrated circuits.

Acknowledgement

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