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High-speed, low-power and low-offset fully differential double-tail dynamic comparator using charge sharing technique

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Abstract. To meet the demand for low-voltage/low-power and high speed analog-to-digital convertors, a new fully differential double-tail dynamic comparator is proposed. To reduce the power dissipation and speed up the comparison process, charge sharing technique has been used in the latch stage of the proposed dynamic comparator. In addition, differential pair and double-tail dynamic comparator topologies are combined to minimize the offset voltage. The proposed dynamic comparator has worst case delay of 0.219 ns, power dissipation of 156.3 μW and offset voltage of 0.184 mV with 1σ deviation of 7.65 mV. The proposed dynamic comparator has been simulated in 0.18 μm CMOS technology with supply voltages of ± 0.75 V using Cadence virtuoso analog design environment.

Keywords. CMOS; dynamic comparator; low power; low offset; high speed.

1. Introduction

In the past few decades with increased digitalization, there has been an urgent requirement for efficient and effective analog-to-digital converters (ADCs) to link analog signals to the digital circuitry. For optimal ADC design, a comparator being an essential component of ADCs needs to be improved continuously to meet the standards of high speed ADC design. Comparators are divided into two broad categories namely, static comparators and dynamic comparators. Static comparators give output as either 'logic 1' or 'logic 0' when input signals are applied. Because of its static nature, any change in the input signals is instantly reflected at the output of the comparator. The major limitation of static comparator is high power dissipation. To overcome its limitation dynamic comparators are introduced where clock signal is used to control the output of the comparator at certain intervals which reduces the power dissipation. Dynamic comparators have a strong positive feedback in the latch stage which allows them to make fast decisions [1]. The offset voltage is an important parameter for the dynamic comparator. Due to its dynamic nature, it exhibits large offset voltage unlike static comparator which offers less offset voltage [2]. Various offset cancellation techniques were reported in the literature [3–6] to reduce the offset voltage of dynamic comparators. An offset cancellation technique has been presented in [5, 6] that uses analog control signals to reduce the offset voltage. For high speed comparators it is necessary to use preamplifiers in the input stage of the comparators which amplify the difference between the two input signals applied to it [7]. Later, this difference is applied to latch stage to finally give a decision. This concept is mostly used in single-tail and double-tail structures of dynamic comparators to reduce the power dissipation. The first double-tail dynamic comparator was proposed in [8]. Due to its two-stage structure, it can be operated on lower supply voltage but it dissipates large power and has large offset voltage. To obtain low offset in the double-tail dynamic comparators, aspect ratios of input transistors are increased which lead to large silicon area and high power dissipation. To solve this trade-off, differential pairs are used as the input transistors in [9]. These structures offer low offset voltage but power is slightly increased due to additional transistors. Another structure focuses on increasing the performance of the comparator by using charge sharing technique [10]. Charge sharing technique reduces the delay and power dissipation of the dynamic comparators by resetting the output nodes to some intermediate level instead of V_{DD} and ground. Structure reported in [11] is a single-stage structure which uses differential pairs in input stage and charge sharing technique in latch stage to reduce delay. However, this structure suffers from stacking of transistors during comparison phase which requires large supply voltage headroom for proper operation. To overcome these limitations, a new fully differential double-tail dynamic comparator using charge sharing technique is presented.

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2. Proposed fully differential double-tail dynamic comparator

The proposed fully differential double-tail dynamic comparator using charge sharing technique (FDDCCST) is shown in figure 1. In the proposed FDDCCST structure, differential pair is used in input stage of conventional DTDC [8] to reduce the offset voltage. Further, to minimize the delay and power dissipation of the proposed FDDCCST charge sharing technique suggested in [10] is employed by using pass transistor logic. The proposed FDDCCST operates in two different phases known as reset phase and comparison phase. In reset phase, when clk = 0, transistors M_{TAIL1} and M_{TAIL2} are switched OFF and transistors M_A, M_B and M_C are switched ON and they will charge the nodes 'A' and 'B' to V_{DD} and therefore, transistors M_5 and M_8 get switched ON. Transistor M_C is used to share the charge between output nodes 'out+' and 'out-'. In comparison phase, when clk = V_{DD}, transistors M_{TAIL1} and M_{TAIL2} are switched ON and transistors M_A, M_B and M_C are switched OFF. Now, nodes 'A' and 'B' start discharging through transistors M_1 to M_4 at different discharging rates depending upon the input gate voltages of transistors M_1 and M_4.

When Vin+ > Vin−, node 'B' discharges faster than node 'A' which will turn OFF the transistor M_8 and output node 'out-' stops discharging. The output node 'out+' discharges below the threshold voltage, which will turn ON the transistor M_9. Therefore, output node 'out-' charges to V_{DD} and output node 'out+' discharges to V_{ss}. Similarly, when Vin− > Vin+, output node 'out+' charges to V_{DD} and output node 'out-' discharges to V_{ss}.

3. Simulation result

The proposed FDDCCST has been simulated in 0.18 µm CMOS technology with supply voltage of ± 0.75 V using Cadence virtuoso analog design environment. Figure 2 shows the transient response of the proposed FDDCCST during one clock cycle, when input signals Vin + and Vin- are applied having V_{cm} = 0.5 V, ΔV_{in} = 5 mV, clock (clk) = 1.5 $V_{p\text{-}p}$ and clock frequency (f_{clk}) of 500 MHz. From the figure, it is observed that the delays t_0, t_{latch} and t_{total} are 0.11 ns, 0.109 ns and 0.219 ns, respectively. The delay of the proposed FDDCCST at different common-mode voltages is affected by input differential voltage (ΔV_{in}) as shown in figure 3. For the given values of common-mode voltages, the delay of the proposed comparator decreases as input differential voltage increases. In addition, the delay also depends on the value of common-mode voltage; it decreases as the common-mode voltage increases. Figure 4 shows that how the PDP of the proposed dynamic comparator at different common-mode voltages depends on the input differential voltage (ΔV_{in}). At a constant V_{cm}, the delay and power reduce as input differential voltage increases due to which PDP also reduces. From the figure, it can be seen that as the value of V_{cm} increases PDP decreases.

Figure 5 shows histogram diagram of offset voltage using Monte-Carlo simulation. From the figure, it can be seen that the absolute offset voltage is 0.184 mV with 1σ deviation of 7.6 mV for the run of 500 samples. The proposed FDDCCST can successfully detect the difference of 4 mV between the two inputs which results in 8 bit resolution. The dependency of supply voltage on delay and PDP

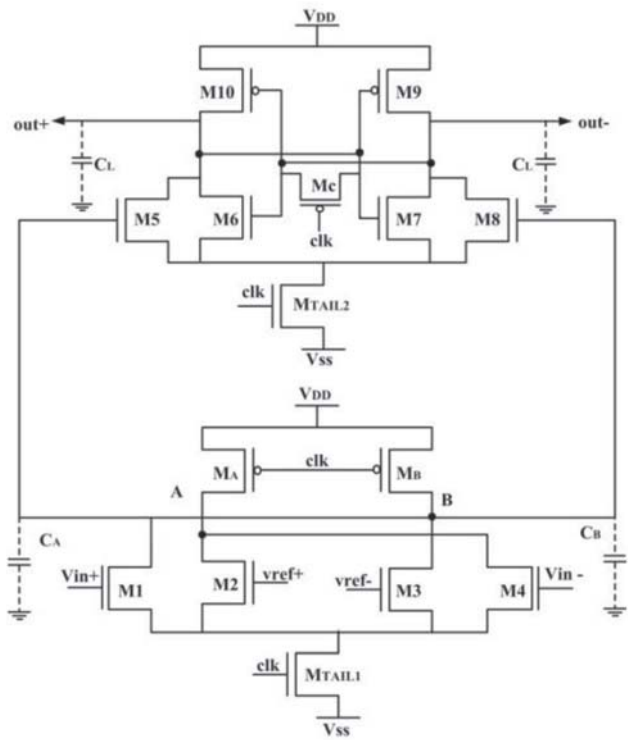

Figure 1. Circuit diagram of proposed FDDCCST.

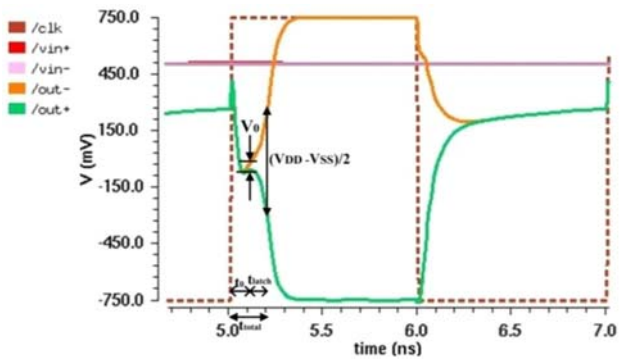

Figure 2. Transient response of proposed FDDCCST.

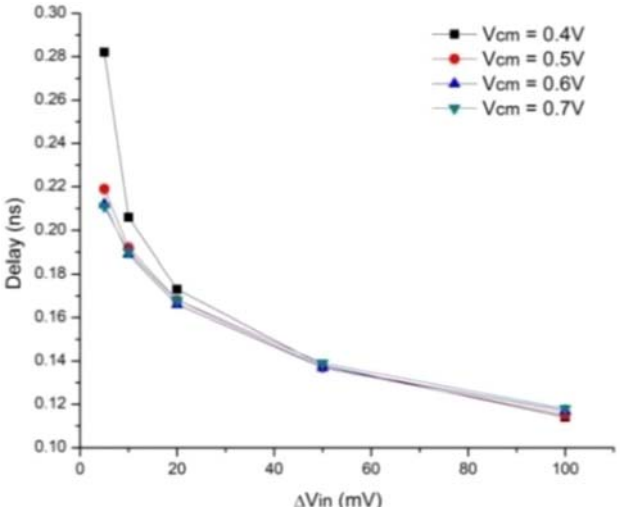

Figure 3. Delay versus input differential voltage (ΔV_{in}).

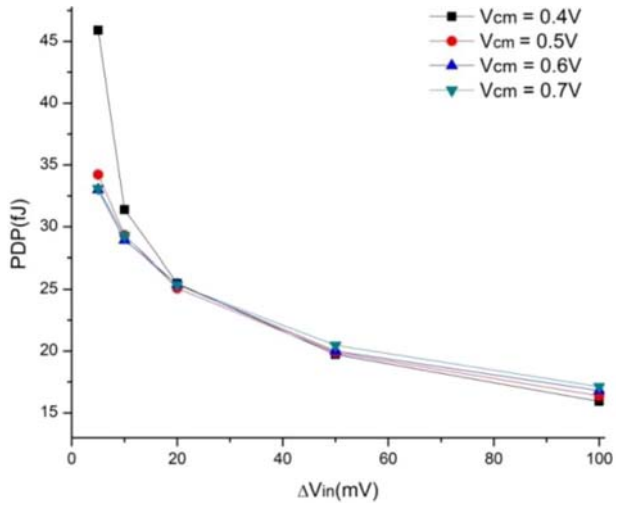

Figure 4. PDP versus input differential voltage (ΔV_{in}).

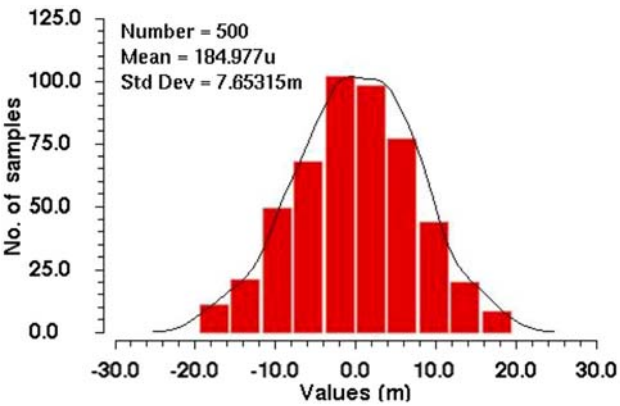

Figure 5. Histogram diagram of offset voltage.

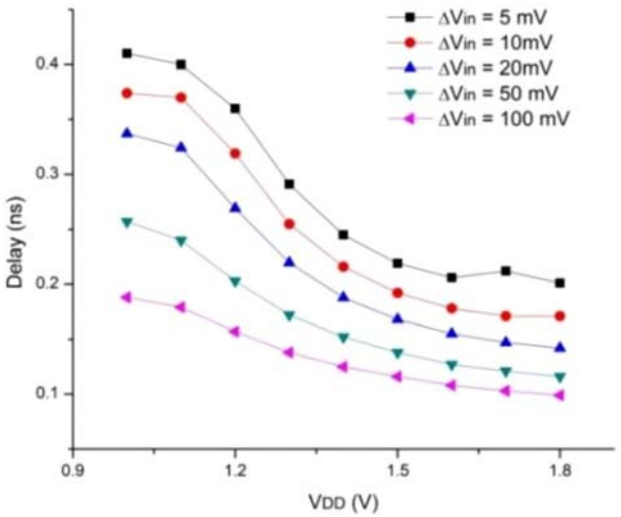

Figure 6. Delay versus supply voltage (V_{DD}).

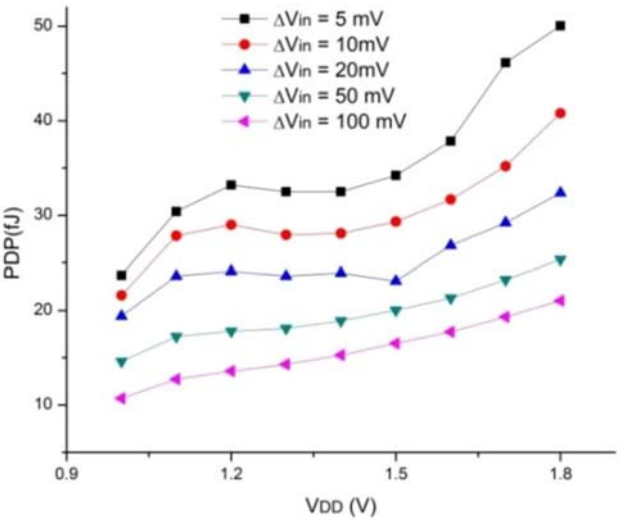

Figure 7. PDP versus supply voltage (V_{DD}).

of the proposed FDDCCST at various input differential voltages are shown in figures 6 and 7, respectively.

From figures 6 and 7, it is evident that the proposed FDDCCST can also be operated at lower supply voltages for all possible values of ΔV_{in}. Finally, Table 1 compares the performance parameters of the proposed FDDCCST with other dynamic comparator structures reported in the literature. From the table, it is evident that the proposed FDDCCST offers reduced delay with low power dissipation and low offset voltage as compared to existing dynamic comparators.

Table 1. Comparison of proposed FDDCCST with dynamic comparators reported in the literature.

Parameters ↓	[12]	[13]	[11]	[5]	[6]	[14]	[9]	[15]	Proposed
Technology (nm)	180	180	180	180	180	180	180	180	180
Supply voltage (V)	1.2	1.2	1.8	–	–	1.8	±0.9	–	± 0.75
Clock Frequency (GHz)	0.5	0.50	0.1	0.8	0.62	0.1	1.3	0.5	0.5
Delay (ns)	0.55	0.273	1.699	–	–	–	0.37	0.30	0.219
Power dissipation (μW)	329	196	460	780	1200	900	265.25	150	156.3
(PDP) (fJ)	181	53.50	736	–	–	–	8.59* 98.14	45	34.22
Offset voltage (mV)	7.8	2.07	–	0.15	0.35	–	0.36	2.4	0.184
Bit resolution	–	–	–	–	9–10	–	10	–	8
Area (μm^2)	–	–	2220.45	–	–	–	256.8	430	465.05

*PDP is calculated using formula PDP = (delay) × (static power). All other PDPs are calculated using formula PDP = (delay) × (avg. power).

4. Conclusion

A new fully differential double-tail dynamic comparator (FDDCCST) is presented in which charge sharing technique is used in the latch stage to reduce delay and power dissipation. The proposed FDDCCST is faster with low power dissipation and low offset voltage than existing dynamic comparators which makes it suitable for low-voltage/low-power high speed mixed signal circuits.

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