Design and application of a novel snubber cell for soft switched pwm dc–dc converters

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Abstract. This paper introduces a novel active snubber cell for soft switching PWM DC–DC converters. In the proposed converter, the main switch is turned on under zero voltage transition (ZVT) and turned off under zero voltage switching (ZVS). The auxiliary switch and all of the other semiconductors in the converter are turned on and off with soft switching (SS). There is no extra voltage stress on the semiconductor devices. Besides, the proposed converter has simple structure and ease of control due to common ground. In this treatise, the theoretical and mathematical analysis of the proposed converter are presented and the design procedure of converters is also provided. The simulation study at 100 kHz switching frequency and 600 W output power are conducted. The experimental prototype of converter is operated under same conditions. Both the simulation and the experimental prototype exhibits similar performances. Ultimately, the efficiency of the proposed converter is 95.7% at nominal power.

Keywords. Active snubber cell; zero voltage transition; zero current transition; hard switching; soft switching.

1. Introduction

The features desired from DC–DC converters with pulse width modulation (PWM) are the high power density, fast dynamic respond, simple structure and control. The converters should be operated at high switching frequencies to achieve these features. However, issues may occur due to hard switching (HS) when conventional PWM DC–DC converters are operated at high switching frequencies. These issues are mainly low power density, switching power losses, electromagnetic interference (EMI), high reverse recovery losses and so on. To eliminate these issues at high switching frequencies, the soft switching (SS) techniques are introduced in the literature [1–4].

Zero voltage transition (ZVT) and zero current transition (ZCT) techniques are called modern switching techniques. Although the main switch is turned on under ZVT and the main diode is turned off under zero current switching (ZCS), the auxiliary switch is turned off under HS in the conventional ZVT converter [5]. To overcome the issue of conventional ZVT converter, a lot of snubber cells are introduced in the literature [6–14].

In [6–8], all semiconductor devices are turned on and off under SS but there is an extra voltage stress on the auxiliary switch. In [9, 10], there is an extra voltage stress on the

auxiliary diode. In [11], the oscillation between parasitic capacitance of the main switch and snubber inductance causes to EMI when the main switch is turned off. In [12], the extra conduction power losses occur since auxiliary element is on the main current line. In [13], the turning on under ZVT for the main switch is poor at light loads. In [14], there are two auxiliary switches in the snubber cell and they do not have common ground, where the control of converter is difficult.

The main switch is turned off under ZCT in the conventional ZCT converter [15]. However, the turning on option of the main switch and the turning off for both the main diode and the auxiliary switch are under HS. Also, the reverse recovery losses of the main diode are high. To overcome these issues, numerous ZCT snubber cells are introduced in the literature [16–26].

In [16], the auxiliary elements are turned off under HS. So, the snubber elements induce extra switching power losses. In [17], the extra voltage stress of the main diode is as much as the output voltage. This particular issue increases the cost. In [18–22], the extra conduction power losses are yielded due to the auxiliary element being on the main current line. In [23], there is the coupled inductance structure in the snubber cell. Therefore, the leakage inductance of the coupled inductance causes the voltage spikes and the power losses. In [24], the extra voltage stress occurs across the main diode and in [25, 26], the auxiliary

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semiconductor elements are exposed on the extra voltage stress.

In this paper, a novel soft switching active snubber cell for PWM DC–DC boost converter is proposed to circumvent the disadvantages of the previously proposed SS converter in the literature. In the proposed converter, the main switch is turned on under ZVT and turned off under zero voltage switching (ZVS). The main diode is turned on under ZVS and turned off under ZCS. The auxiliary switch is turned on under ZCS and turned off under ZCT. Additionally, there is no additional voltage stress on the semiconductor devices. The proposed converter decreases EMI noises and operates a wide load voltage range. So, total efficiency is higher than the conventional ZVT boost converter.

2. Operating intervals

The proposed converter is presented in figure 1. In the main circuit, V_i is input voltage source, V_o is output voltage, L_m is input filter inductance and C_m represents the output filter capacitance. The main diode is indicated by D_m , S_m represents the semiconductor switch and D_{Sm} is its body diode, and also R_L denotes the resistive load. In the snubber cell, the auxiliary switch is denoted by S_a and D_{Sa} is its body diode, the snubber capacitance is indicated by C_s , while the auxiliary diode is indicated by D_a . Finally, L_r and C_r represent the resonance inductance and capacitance, respectively.

In the steady state analysis of the proposed converter, the following assumptions are considered.

- Filter inductance L_m is assumed to be large enough to keep the input current constant and output filter capacitance C_m is assumed to be large enough so that output voltage can be kept constant.
- The resonance circuits and semiconductor components are ideal.
- Reverse recovery time of all the diodes is ignored.

The steady state operation of the converter contains eight operational modes in one switching cycle. The equivalent circuits of these operational modes are presented in figure 2. Furthermore, the key waveforms of the operational modes are described in figure 3.

Figure 1. The basic circuit scheme of the proposed converter.

Mode 1 [$t_0 < t < t_1$: figure 2(a)]

Before $t = t_0$, the main switch is in the off state, the voltage of capacitance C_s is equal to the output voltage and the input current flows through the main diode D_m . At $t = t_0$, the control signal is applied to the gate of the auxiliary switch S_a and this mode is started, where the current of the auxiliary switch increases while the current of the main diode decreases linearly. At $t = t_1$, the current of the auxiliary switch reaches the input current and the current of the main diode arrives at zero. The auxiliary switch is turned on under ZCS since L_r inductance is connected in series. The following equations are provided for this interval:

$$i_{Lr}(t) = \frac{V_o}{Z_1} \sin(\omega_1(t - t_0)) \quad (1)$$

$$v_{Cr}(t) = V_o - V_o \cos(\omega_1(t - t_0)) \quad (2)$$

$$Z_1 = \sqrt{\frac{L_r}{C_r}} \quad (3)$$

$$\omega_1 = \frac{1}{\sqrt{L_r C_r}} \quad (4)$$

Mode 2 [$t_1 < t < t_2$: figure 2(b)]

At $t = t_1$, a resonance starts through $C_s - L_r - C_r$. The current of L_r is increased while the voltage of C_s is decreased in sinusoidal. When the voltage of C_s reaches to zero, this mode is finished. The following equations are derived for this mode:

$$i_{Lr}(t) = \frac{V_1}{Z_2} \sin(\omega_2(t - t_1)) + I_1 \cos(\omega_2(t - t_1)) - I_1 + I_{Lr}(t_1) \quad (5)$$

$$v_{Cr}(t) = \frac{I_{Lm}}{C_r + C_s}(t - t_1) + V_{Cr}(t_1) - \frac{C_{eq}}{C_r} [V_1 \cos(\omega_2(t - t_1)) - I_1 Z_2 \sin(\omega_2(t - t_1)) - V_1] \quad (6)$$

$$v_{Cs}(t) = \frac{I_{Lm}}{C_r + C_s}(t - t_1) + V_o + \frac{C_{eq}}{C_s} [V_1 \cos(\omega_2(t - t_1)) - I_1 Z_2 \sin(\omega_2(t - t_1)) - V_1] \quad (7)$$

In here;

$$I_1 = I_{Lr}(t_1) - \frac{C_{eq}}{C_s} I_{Lm} \quad (8)$$

$$V_1 = V_o - V_{Cr}(t_1) \quad (9)$$

$$C_{eq} = \frac{C_r C_s}{C_r + C_s} \quad (10)$$

$$Z_2 = \sqrt{\frac{L_r}{C_{eq}}} \quad (11)$$

Figure 3. Key waveforms concerning the operation modes in the proposed converter.

$$I_{Lr}(t_2) = \frac{\sqrt{V_1^2 + (I_1 Z_2)^2}}{Z_2} + \frac{C_{eq}}{C_s} I_{Lm} \quad (17)$$

Mode 4 [$t_3 < t < t_4$: figure 2(d)]

At $t = t_3$, a resonance starts between L_r and C_r . The current of L_r is increased when the voltage of C_r is decreased in sinusoidal. The body diode of the auxiliary switch is in the on state during this mode. The control signal of the auxiliary switch is removed and this switch is

turned off under ZCT when its body diode is in the on state. Therefore, the turning off switching losses of the auxiliary switch is completely eliminated. The voltage of C_r reaches zero and this mode is finished.

$$i_{Lr}(t) = -\frac{V_{Crpeak}}{Z_1} \sin(\omega_1(t - t_3)) \quad (18)$$

$$i_{Lr}(t) = V_{Crpeak} \cos(\omega_1(t - t_3)) \quad (19)$$

$$i_{Sm} = I_{Lm} - i_{Lr}(t) \quad (20)$$

In here;

$$V_{Crpeak} = \sqrt{\frac{L_r I_2^2(t_2) + C_r V_2^2(t_2)}{C_r}} \quad (21)$$

Mode 5 [$t_4 < t < t_5$: figure 2(e)]

During this mode, the main inductance L_m stores the energy under the input voltage source, which is expressed in the following equations:

$$i_{Lr}(t) = I_{Lrpeak} = \frac{V_{Crpeak}}{Z_1} \quad (22)$$

$$i_{Sm} = I_{Lm} + I_{Lrpeak} \quad (23)$$

Mode 6 [$t_5 < t < t_6$: figure 2(f)]

At $t = t_5$, the control signal of the main switch is removed, which starts this mode. The switch is turned off under ZVS due to parallel capacitance C_s , which is charged by the sum of the currents I_{Lm} and I_{Lrpeak} . At $t = t_6$, the voltage of C_s reaches the output voltage, which finishes this mode.

$$i_{Lr}(t) = i_{Lm} - (i_{Lm} + i_{Lrpeak}) \cos(\omega_1(t - t_5)) \quad (24)$$

Mode 7 [$t_6 < t < t_7$: figure 2(g)]

At $t = t_6$, the main diode is turned on under ZVS, which starts this mode. During this mode, the current of L_r inductance is reduced linearly and its energy is transferred to the output. At $t = t_7$, the I_{Lr} reaches zero and this mode is finished. The following equations are derived for this mode:

$$i_{Lr}(t) = I_{Lrmax} - \frac{V_o}{L_r}(t - t_6) \quad (25)$$

$$i_{Dm} = I_{Lm} + i_{Lr}(t) \quad (26)$$

Mode 8 [$t_7 < t < t_8$: figure 2(h)]

This mode is the off mode of conventional boost converter. I_{Lm} is transferred to the output side through the main diode during this mode. At the end of this mode, it is returned to the initial conditions by applying control signal to the auxiliary switch. The following equation is provided for this mode:

$$i_{Dm} = I_{Lm} \quad (27)$$

3. Design procedure

In this section, the design procedure of the proposed converter is presented. The parameters values of 200 V input voltage, 400 V output voltage, 100 kHz switching frequency and 600 W output power are utilized in the design procedure.

3.1 The selection of L_r snubber inductance

The reverse recovery time of the main diode t_{rr} is considered to select the L_r inductance. When the auxiliary switch is turned on, the current of switch must reach the input current at most within $3t_{rr}$. The reverse recovery time of the main diode used in the application is 50 ns. The following equation can be written for selecting L_r snubber inductance:

$$\frac{1}{\omega_1} \sin^{-1} \left(\frac{I_{Lm} Z_1}{V_o} \right) \geq 3t_{rr} \quad (28)$$

3.2 The selection of C_r snubber capacitance

The ZVT duration t_{ZVT} is quite important for SS at the turning on instant. Therefore, the t_{ZVT} must be longer than the rise time of the main switch t_r . The t_{ZVT} depending on the snubber capacitance C_r and snubber inductance L_r is shown in figure 4.

3.3 The selection of C_s snubber capacitance

When the switch is turned off, the voltage of switch must reach the output voltage at least within the fall time of the switch t_{f1} . The fall time of the switch used in the application is 125 ns. The following equations can be written for selecting C_s snubber inductance.

$$C_s \geq \frac{I_{Lm} + I_{Lrmax}}{V_o} t_{f1} \quad (29)$$

Figure 4. Variation of ZVT duration depending on resonance inductance L_r for different values of capacitance C_r .

Table 1. The experimental parameters and the device values of the proposed converter.

Parameters	Value
DC input voltage, V_i	200 V
DC output voltage, V_O	400 V
Output power, P_O	600 W
Switching frequency, f_s	100 kHz
Main inductance, L_m	1 mH
Resonance inductance, L_r	2 μ H
Filter capacitance, C_m	470 μ F
Snubber capacitance, C_s	3.3 nF
Resonance capacitance, C_r	33 nF

4. Simulation results

The simulation parameters are presented in table 1. The simulation was performed with a 200 V input voltage and 400 V output voltage under a 100 kHz switching frequency and 600 W output power by POWERSIM 9.1.1 program. Figures 5(a)–(c) illustrate the simulation waveforms of the control signals switches, the voltage and current of the main switch, the main diode and the auxiliary switch, respectively. Figure 5(d) illustrates the simulation waveforms of the voltage of auxiliary diode and the resonance capacitance and the current of resonance inductance, respectively. According to the simulation results, all of the semiconductor elements are turned on and off under SS. Besides, there is no additional voltage stress on any element.

Figure 5. Simulation results of current and voltage waveforms of (a) S_m , (b) D_m , (c) S_a , and (d) voltage waveform of D_a , C_r and current waveform of L_r . **Figure 6.** The experimental circuit of proposed converter.**Table 2.** The experimental parameters and the device values of the proposed converter.

Devices	Part number	V (V)	I (A)	t_r (ns)	t_f (ns)	t_{rr} (ns)
S_m	IXFH30N60P	600	30	20	25	200
S_a	FCP190N60E	600	20	14	15	308
D_m	MUR860	600	8	–	–	60
D_a	DESI8-06	600	8	–	–	50

Figure 7. Experimental results of current and voltage waveforms of (a) S_m , (b) D_m , (c) S_a , and (d) voltage waveform of D_a , C_r and current waveform of L_r (200 V/div, 10 A/div, 2 μ s/div).

Table 3. Switching status of the semiconductor elements.

Devices	Turning on	Turning off
S_m	ZVT	ZVS
D_m	ZVS	ZCS
S_a	ZCS	ZCT
D_a	ZCS	ZCS

5. Experimental results

The experimental prototype of the proposed converter was implemented with reference to the parameters in table 1. The photograph of experimental prototype is illustrated in figure 6. Besides, the semiconductor devices used in the experimental prototype are given in table 2.

Figure 7 shows the experimental results of the proposed converter. These results are compatible with theoretical analysis and simulation results. In figure 7(a), the control signals of the switches, the current and voltage waveforms

of the main switch are illustrated. As shown in figure, the control signal is applied to the main switch after the voltage of main switch is reached zero. So, the main switch is turned on under ZVT without the current and voltage overlapping. Moreover, the main switch is turned off under ZVS. Therefore, the turning on switching power losses is eliminated and the turning off switching power losses is reduced for the main switch by novel snubber cell. Besides, there is no extra voltage stress on the main switch.

In figure 7(b), the control signal of the main switch, the current and voltages waveforms of the main diode are illustrated. The main diode is turned on under ZVS and turned off under ZCS. So, its switching power losses and reverse recovery losses are significantly reduced. Moreover, there is no extra voltage or current stress on the main diode.

In figure 7(c), the control signal, the current and voltage waveforms of the auxiliary switch are illustrated. As shown in figure, the auxiliary switch is turned on under ZCS and turned off under ZCT. Therefore, the turning on switching power losses is reduced and the turning off switching power

Figure 8. The efficiency curves of the proposed converter comparatively.

Table 4. Comparison of different converters in terms of their amount of components.

Topology	Number of snubber circuit components				Commutations		
	Number of inductance	Number of transformer	Number of capacitance	Number of aux. diode	Turning on	Turning off	Leakage inductance issue
<i>Proposed</i>	1	–	2	1	ZVT	ZVS	No
<i>Ref. [2]</i>	–	1	1	3	ZVT	ZCT	Yes
<i>Ref. [3]</i>	1	1	1	3	ZVT	ZCT	No
<i>Ref. [4]</i>	1	–	2	2	ZVT	ZVS	No
<i>Ref. [23]</i>	–	1	1	4	ZVT	ZCT	Yes
<i>Ref. [24]</i>	–	1	2	1	ZVT	ZCT	Yes

losses is eliminated for the auxiliary switch. Additionally, there is no extra voltage stress on the auxiliary switch.

In figure 7(d), the voltage waveforms of the auxiliary diode and the snubber capacitance and the current waveform of the snubber inductance are illustrated. It is clear from figure 7(d) that there is no extra voltage stress on the auxiliary diode and the voltage of snubber capacitance does not exceed the output voltage.

Finally, the switching cases of all semiconductor devices in the proposed converter are presented in table 3. The efficiency graphics of the proposed converter and HS converter are illustrated in figure 8. While the efficiency value of converter is about 91.8% by hard switching, it is measured 95.7% for soft switching at the nominal output power.

6. Features of the proposed converter

The features of the proposed converter are introduced in this section. Besides, the comparative analysis of the proposed novel converter and other SS converters are proposed, where the related results are provided in table 4. The most important features of the proposed converter are follows:

- The main switch is turned on under ZVT and turned off under ZVS.
- The main diode is turned on under ZVS and turned off under ZCS.
- The auxiliary diode is turned on under ZCS and turned off ZCT.
- The auxiliary diode is turned on/off under SS.
- The extra voltage stress does not occur on the main and auxiliary semiconductor devices.
- The duration of transient modes constitutes only a small part of the switching period.
- The control of converter is simple due to the common ground.
- The structure of snubber is comprehensive.
- The proposed snubber cell can be applied into other dc–dc converters.
- The proposed converter does not need a passive snubber cell.
- The cost of converter is considerably low.
- The proposed converter can operate under light load.

As seen in table 4, the proposed converter has less number of auxiliary components. Besides, the proposed converter provides SS for both the main and auxiliary

semiconductor devices with the minimum snubber components. One of the most prominent features of the proposed converter is that there is no issue of inductance leakage. For this particular reason, it does not require a passive snubber cell. Thus, the cost of proposed converter is substantially reduced compared to other converters.

7. Conclusion

In this treatise, a novel active snubber cell PWM DC–DC boost converter is developed. The proposed snubber cell provides ZVT turning on and ZVS turning off for the main switch. Besides, the main diode is turned on under ZVS and turned off under ZCS, whereas all of auxiliary semiconductor devices are soft switched. The proposed converter has simple structure, low cost and ease of application features. Furthermore, theoretical analysis of the converter is performed and a laboratory prototype is implemented. The experimental results are confirmed with both of the theoretical analysis and simulation of a 600 W output power and 100 kHz switching frequency. Additionally, at nominal output power, the converter efficiency reaches 95.7%.

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