Development of an auto-synchronization technique for improving the power stability of copper vapour laser oscillator and amplifier configuration

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Abstract. A technique to synchronize multiple copper vapour laser (CVL) systems in master oscillator power amplifier configuration to obtain long-duration power stability is discussed in this manuscript. The technique utilizes optoelectronic interconversion of the current pulses of CVL oscillator and amplifiers units as a feedback signal. The signal processing of the current pulses was performed using a monostable multivibrator, R–S flip-flop and passive low pass filter. The DC voltage generated corresponding to the quantum of temporal mismatch between the oscillator and the amplifier modules is sampled, averaged and compared to the set point voltage using a Programmable Logic Controller. The timing signal of the respective amplifiers could be accordingly adjusted to synchronize with the CVL oscillator optical pulses to obtain long-duration power stability.

Keywords. High-frequency current transformer (CT); HFBR (optical transmitter and receiver IC series); copper vapour laser; R–S flip-flop.

1. Introduction

Copper vapour laser (CVL) is a pulsed-electric discharge pumped laser. In order to scale the power, the CVL needs to be operated in master oscillator power amplifier (MOPA) configuration. Maximum output power from a MOPA can be obtained when the optical pulse from the oscillator arrives at the amplifier at the time instant when the amplifier has the maximum gain for power extraction. In MOPA configuration, an oscillator provides a good quality seed pulse, which is further amplified using series of amplifiers to extract maximum output optical power. The oscillator and the amplifiers are operated at 9-kHz pulse repetition frequency. Each system has temporal jitter in the range of 8–10 ns. The MOPA is synchronized by varying the timing signal of the pulse generator unit (PGU) of each CVL system. The need for timing synchronization arises due to the difference in the propagation delays of the individual PGU and the optical delay between the MOPA units. The optical delay however remains constant. The variation in the propagation delay of the system results in the de-synchronization of the MOPA. The propagation delay of the system varies due to dynamic nature of the CVL load, variation in the operating pressure, variation in the DC input voltage and thermal drift caused due to the temperature dependence of the several components of the

PGU [1]. The CVL MOPA beam is used for the optical pumping of the dye laser. The de-synchronization and instability of the MOPA output lead to uncertainty in the dye laser operation with reference to the increased amplified spontaneous emission (ASE), line-width fluctuation and decreasing efficiency [2]. The automatic follow-up system is utilized to adjust the timing delay at an optimal point to maintain maximum CVL MOPA output power by Behrouzinia *et al* [3]. The optical signal at the output of the amplifier is sampled by a transistor photocell, which is later used for signal processing [3].

The temporal pulse profile of the CVL oscillator has pulse width of around 25–30 ns (FWHM), while that of the amplifier is around 50 ns (FWHM). The CVL systems are configured in MOPA configuration. In order to extract maximum power at the output of the amplifier, the oscillator seed pulse should enter the amplifier when the maximum gain is available in the amplifier, i.e., maximum population inversion. If the oscillator and the amplifier are not in synchronization, the atoms in the upper energy level of the amplifier medium undergo spontaneous emission due to unavailability of the seed pulse, resulting in increased ASE. Since the gain of the amplifier medium remains underutilized, the output optical power decreases.

The experiment carried out to study the MOPA characteristics in the open loop condition emphasized the need to have an auto-synchronization topology to improve the MOPA performance. The MOPA output was focused using

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Figure 1. Total MOPA optical power vs delay; % change in power before and after the aperture vs delay.

a 2.6-m radius of curvature mirror and passed through a 1-mm aperture to eliminate the ASE in the optical beam of the MOPA [4]. The MOPA optical power was measured before and after the aperture by varying the trigger delay of the amplifier in steps of 5 ns. The delay shown in figure 1 is the relative delay between the oscillator and the amplifier, where the delay '0' indicates trigger position of the amplifier where the maximum average power is obtained. As seen from figure 1, the MOPA power decreases when the amplifier is relatively de-synchronized with respect to the oscillator. The extent of the fall in power increases as we move away from the peak position. Also, the percentage change in power measured before and after the aperture increased with the increase in relative de-synchronization of the MOPA. This phenomenon can be attributed to the increased ASE at the MOPA output. Thus, MOPA optical

power decreases and the ASE content increases with relative de-synchronization of the oscillator and the amplifier. The optical power decrease and increased ASE are undesirable from the point of view of long-duration optical power stability of the CVL MOPA.

The timing delay to the optical output being an open loop system, any change in the operating parameters changes the propagation delay of the final optical pulse. In the open loop system, this drift in propagation delay was found to be in the range of 50–60 ns in 2 h (0.5 ns/min). The long-duration optical power stability of the MOPA can be ensured by controlling the slow propagation delay drift taking place in the system. The topology discussed in the manuscript utilizes the feedback signal from the high-frequency current transformer (CT) connected in the return path of the current pulse. The signal is processed using the R–S flip-flop phase comparator and low pass filter to generate the error signal voltage, which is further compared to the set point voltage to implement the corrective timing action for observed delay.

2. Methodology

Figure 2 shows a schematic of the auto-synchronization topology developed and tested with our system. The figure shows an oscillator and one amplifier system being used for the synchronization. The same is extended to rest of the amplifiers used in the MOPA chain.

Figure 2. Schematic of the auto-synchronization topology.

Figure 3. CVL current pulse waveform (a) and TTL pulse obtained at the receiver end (b).

The current pulse of the CVL drives the optoelectronic pulse transformer. The wide bandwidth CT is terminated with the burden resistance.

The voltage developed across the burden is itself used to drive the optical transmitter, taking proper polarity of the signal into consideration [5, 6]. The on-state conduction voltage of the HFBR transmitter is 1.6–1.7 V. Thus the CT has been designed with the sensitivity ($G = V_{on}/I_t$) of 0.037 V/A. A ferrite toroidal core T6320-CF197 manufactured by Cosmo Ferrites was chosen. The parameters of the chosen core were as follows: outer diameter (O.D.) of 63 mm, internal diameter (I.D.) of 38 mm, height (h) of 20 mm, toroid effective length (L_e) of 152.1 mm, effective core cross-sectional area (A_c) of 244.7 mm², μ_r of 7000, core resistivity (ρ_c) of 0.2 Ω -m and inductance factor (A_l) of 13000 nH/N² where N is the number of turns wound on the toroid. The number of turns in the secondary winding is chosen to be 35 and a burden resistor of 1.3 Ω is used. The CT has been designed with the sensitivity of 0.037 V/A. When the voltage developed across burden resistance crosses the on-state voltage of the HFBR transmitter, the optical signal of the on-time duration, approximately equal to the base to base pulse width of the current signal, is transmitted through the fibre optic link. The optical to electrical signal conversion takes place at the receiver end using the optical receiver HFBR connected in the external pull-up mode. The TTL pulse at the output of the receiver HFBR is used for the signal processing. Figure 3 shows the typical CVL current pulse and the corresponding TTL pulse obtained at the receiver end [5].

The TTL pulse width corresponding to the oscillator and the amplifier needs to be precisely matched for the topology to function reliably. The dynamic nature of the CVL load causes pulse to pulse variation in the pulse width. Hence the

Figure 4. The i/p–o/p conditions of R–S flip flop for oscillator and amplifier pulses.

corresponding TTL pulses will also vary accordingly. The uncertainty is reduced using IC 74123 in the monostable multivibrator mode. The timing resistor and the capacitor are adjusted to obtain the output pulse of 300 ns. As shown in figure 2, the pulses obtained at the output of the IC 74123 corresponding to both oscillator and amplifier are fed to the R–S flip-flop. The TTL pulse corresponding to the oscillator and amplifier is connected to the set and the reset pin of the R–S flip-flop, respectively. The output remains high when the oscillator pulse is high whereas the output remains low when the amplifier pulse is high.

Figure 5. Output of R–S flip-flop (a) and output of low pass filter (b) for the condition shown in figure 3a. X-axis—100 ns/div; Y-axis—2 V/div.

Figure 6. Output of R–S flip-flop (a) and output of low pass filter for the condition shown in figure 3b. X-axis—100 ns/div; Y-axis—2 V/div.

Figure 7. Effect of jitter on the output of R–S flip flop.

Figure 4 shows the input and output conditions of R–S flip-flop where the oscillator is delayed w.r.t. the amplifier in figure 3a. During the time period of 111 μ s, the output remains high for most of the time except 300 ns. The output of the R–S flip-flop is put through the passive low pass filter having RC time constant of 1 s and bandwidth of 0.15 Hz. The output of the low pass filter corresponding to figure 4a is shown in figure 5. The average DC value of the output of the R–S flip-flop comes out to be close to 5 V (i.e., 4.325 V) as shown in figure 5. Figure 4 also shows the input and output conditions of R–S flip-flop where amplifier is delayed w.r.t. oscillator (figure 4b). During the time period of 111 μ s, the output remains low for most of the time except 300 ns. The average DC value of the output of the

R–S flip-flop comes out to be close to 0 V (i.e., 0.167 V) as shown in figure 6.

The higher relative jitter in the two pulses increases the variation of the dc voltage. In order to smoothen the output voltage, the RC time constant should be increased.

However, when the oscillator and the amplifier pulses are close to each other in time, either the oscillator or the amplifier pulse could be delayed w.r.t. each other in a random manner. The average value is a function of the temporal jitter of the oscillator and the amplifier pulses, which is in the range of 8–10 ns. The pulse of either oscillator or amplifier, whichever comes later, dictates the output of the R–S flip-flop for that cycle. When the amplifier, which is connected to R pin, appears later, correspondingly the output will be close to 5 V whereas the output will be close to 0 V when the oscillator appears later. This is illustrated in figure 7. The fast DC voltage variation occurring due to the random nature of the oscillator and the amplifier jitters is averaged using the low pass filtering. Out of 9000 pulses per second, depending upon how many pulses of oscillator are delayed w.r.t. amplifier and vice versa, the average DC voltage at the output of the low pass filter will be in the range of 0–5 V. Figure 8 shows an intermediate voltage between 0 V and 5 V. If the optical path delay of the amplifier is exactly matched w.r.t to the oscillator, the synchronization point would be obtained at the centre of the two extreme voltages, i.e., around 2 V.

Figure 8. The output of R–S flip flop (a) and output of low pass filter (b) when the TTL pulses are close to each other within its temporal jitter range. X-axis—500 ms/div; Y-axis—1 V/div.

A PLC is used for the data processing and corrective feedback action. The average DC voltage received at the input of the PLC is commensurate with the time difference between the two current pulses from oscillator and amplifier. The DC voltage at the output of the filter is read into PLC using an analogue input card. Totally 64 samples are averaged at the PLC scan rate of 50 ms for the data processing. These data correspond to the feedback voltage used for the comparison to the set point voltage. The set point voltage is determined experimentally by optimizing the optical power manually in the open loop system. The direction of delay change and the voltage change are also determined experimentally. In order to arrive at the set point voltage, the time delay of the amplifier was varied w.r.t. the oscillator, and power at the output of the amplifier was measured along with the voltage at the output of the low pass filter. At the delay value at which the maximum power was obtained, the corresponding voltage at the output of filter was the set point voltage.

Figure 9 illustrates the variation of average DC voltage w.r.t. the incremental variation in the time delay given to the amplifier. The set point can be approximately obtained at the centre of the graph, i.e., around 2–2.5 V, by matching the optical delay of the two systems. This optical delay adjustment can be done by relatively increasing the length of the optical fibre of the amplifier w.r.t. the oscillator. The set point thus obtained in the open loop operation is fed to the PLC. If this voltage deviates from the set point voltage, the output action of the PLC varies the delay, which is given to the PGU of the amplifier in the steps of 1 ns every 5 s. The drift in propagation delay measured is found to be in the range of 50–60 ns in 2 h (0.5 ns/min). The response time of this closed loop system is sufficient to correct any change in the slow temporal drift taking place. The topology is able to keep the delay within the temporal delay of 1 ns for reliable MOPA operation. This corrective feedback operation is carried out such that the error voltage between the set point and the average DC voltage is within the band of 100 mV. Figure 10 shows stability of the MOPA power

Figure 9. Variation of average DC voltage w.r.t. the incremental variation in the time delay given to the amplifier.

Figure 10. MOPA power vs time.

during continuous 2-h operation. Thus, the oscillator and the amplifier optical pulses are synchronized to ensure long-term MOPA power stability. The optical isolation provides immunity from electromagnetic interference noise emanating from the CVL discharge, which is due to high-voltage and fast-switching phenomenon.

3. Conclusions

The technique used for the auto-synchronization of the CVL oscillator and the amplifiers corrects the timing instability of the optical pulses caused due to dynamic nature of the CVL load, variation in the pressure, variation in the DC input voltage and thermal drift caused due to the temperature dependence of several components of the PGU. The correction in the timing pulses on continuous basis ensures long-duration MOPA optical power stability. This topology has inherent advantage of optoelectronic inter-conversion at both ends, which provides the electromagnetic interference noise immunity to the system.

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