Design, analysis and application of high set-up ZVT DC–DC converter with direct power transfer

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Abstract. In this paper, a new snubber cell for soft switched high set-up DC–DC converters is introduced. The main switch is turned on by zero-voltage transition and turned off by zero-voltage switching (ZVS). The main diode is turned on by ZVS and turned off by zero-current switching. Besides, all auxiliary semiconductor devices are soft switched. Any semiconductor device does not expose the additional current or voltage stress. The new snubber transfers some of the circulation energy to the output side when it ensures soft switching for main semiconductor devices. Thus, the current stress of auxiliary switch is significantly reduced. Besides, the total efficiency of converter is high due to the direct power transfer feature of new converter. A theoretical and mathematical analysis of the new converter is presented, and also verified with experimental set-up at 500 W and 100 kHz. Finally, the overall efficiency of new converter is 97.4% at nominal output power.

Keywords. Zero voltage transition; active snubber cell; hard switching; soft switching.

1. Introduction

The high set-up converters are prevalently used in battery chargers, hybrid energy storage systems, power factor correction (PFC) and photovoltaic (PV) systems. The reason for this preference is higher power density, fast dynamic response and simple control features of high set-up pulse width modulation (PWM) DC–DC converters [1–4]. These features can be assured more easily at high switching frequencies. Hence, high set-up converters should be operated at as high frequency as possible. Classical high set-up converters operate with hard switching (HS). Because of HS, various problems occur in high set-up converters at high frequencies [5–7]. These problems are the switching power losses, electromagnetic interference (EMI), high reverse recovery losses, etc. In order to overcome these problems at high switching frequencies, the soft switching (SS) techniques are introduced in the literature [8–12].

Zero-voltage switching (ZVS) and zero-current switching (ZCS) techniques are called classical techniques and they are achieved using only passive devices. Zero-voltage transition (ZVT) and zero-current transition (ZCT) techniques are called modern techniques and they are achieved using a combination of active and passive devices. In the first developed high set-up ZVT converter introduced in

[13], the main switch was turned on by ZVT and the main diode was turned off by ZCS. The disadvantage of this converter is that the auxiliary switch is turned off with HS. Additionally, the currents stress of auxiliary switch is high. To overcome the problems of this ZVT converter, many topologies are introduced in the literature [14–32].

In [14], the semiconductor devices are turned on and off with SS but the main switch is exposed to high current stress. In [15], the main switch operates with SS without extra current stress. However, the voltage stress of the main diode is twice the output voltage. In [16, 17], SS depends on load current and hence SS cannot be achieved at light loads. The snubber cell introduced in [18] provides SS operation for the main switches and reduces voltage stress of the main switches. However, the auxiliary devices are operated by HS.

In [19], the auxiliary devices are turned off under HS. Hence, the snubber elements cause extra switching power losses. In [20], the extra voltage stress of the main diode is as much as the output voltage and it increases the converter cost. In [21–25], extra conduction power losses occur since the auxiliary devices are on the main current line. In [26], there is a coupled inductance structure in the snubber cell. Therefore, the leakage inductance of the coupled inductance causes voltage spikes and power losses. In [27], the auxiliary semiconductor devices are exposed to extra voltage stress. In [28, 29], all semiconductor devices are turned on and off with SS without additional

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current/voltage stress. However, there are snubber inductances on the main current line. Hence, additional conduction losses occur in the converter. In [30], SS is achieved using an active snubber cell for all semiconductor devices but turning-on of the main switch has loss due to energy stored in the parasitic capacitor of the switch. In [31], ZVT is achieved for high set-up interleaved switches but there is a transformer in auxiliary circuit. The leakage inductance causes additional losses in this converter. When the converter operates in duty cycles under 0.5, the snubber cell does not achieve SS operation in [32]. Hence, this snubber cell cannot be applied in PFC applications and forward converters.

In this study, a new SS snubber cell for high set-up PWM DC–DC converter is presented. In the new converter, the turning-on is achieved by ZVT for the main switch and by ZVS for the main diode. The turning-off is achieved by ZVS for the main switch and by ZCS for the main diode. For the auxiliary switch, the turning-on by ZCS and the turning-off by ZVS are achieved. Besides, the auxiliary diodes are switched by SS. The proposed converter has an auxiliary transformer and this transformer ensures both SS for main semiconductor devices and increasing the performance of converter. The leakage inductance issues do not occur in the new converter because of its design. The proposed converter transfers some of the circulation energy to the output side by the auxiliary transformer during the ZVT operation. This case is called direct power transfer (DPT) in the literature. Hence, both the current stress of auxiliary switch is reduced and the total efficiency is increased.

This study is organized as follows. In order to obtain the operational cases of the proposed converter, a SS high set-up converter using the new snubber circuit is discussed. Besides, a mathematical analysis of the converter is introduced in section 2. Section 3 presents the design procedure and section 4 provides the features of new converter. To demonstrate the effectiveness of the new converter, an experimental set-up is prepared and related experimental results of a 500-W high set-up converter are presented in section 5.

2. Operational principle and analysis

The proposed new high set-up ZVT-PWM DC–DC converter with DPT is illustrated in figure 1. In the main circuit of proposed converter, V_i is input voltage source, V_o is output voltage, L_F is filter inductance, C_F is output filter capacitance and R is resistive load. D_F represents the main diode, S_1 is the main switch and D_1 is its internal diode; C_P is sum of the parasitic capacitance of the main diode, the main switch and other parasitic capacitance. Therefore, an additional capacitance is not needed for C_P . In the snubber cell of proposed converter, the auxiliary switch is denoted

Figure 1. The circuit scheme of the proposed high set-up ZVT-PWM DC–DC converter.

by S_2 ; C_S is the snubber capacitance, while the auxiliary diodes are represented by D_2 , D_3 and D_4 . Finally, TR is the high-frequency transformer, L_m is its magnetization inductance and L_S is the snubber inductance.

Eight operational cases occur in one switching period. The key converter wave shapes are illustrated in figure 2. Figure 3 shows the equivalent circuits of operational cases. In order to simplify the theoretical analysis of proposed converter, the filter components are assumed to be large enough to hold the input current and output voltage constant.

Case 1 $[t_0 < t < t_1]$: figure 3a)

At $t = t_0$, when the gate signal is the applied to the gate of auxiliary switch S_2 , this case is started. The auxiliary switch S_2 and the auxiliary diode D_2 diode are turned on simultaneously. The auxiliary switch S_2 is turned on by ZCS due to L_S inductance. The auxiliary diode D_2 is turned on by both ZVS and ZCS (ZVZCS). Also, the current of the main diode D_F decreases while the currents of the L_S and L_M inductances increase linearly. At the same time, some of the circulation energy is transferred to the output side by the auxiliary transformer. DPT reduces currents stresses of both the auxiliary switch and snubber inductance. Moreover, the total efficiency of converter is increased since circulation losses are reduced. At $t = t_1$, when the current of snubber inductance L_S arrives at the input current level, the current of main diode D_F drops to zero and this case ends. The following equations can be written at this case:

$$i_{LS}(t) = \frac{V_o}{2(L_S + L_M)}(t - t_0) \quad (1)$$

$$i_{DF}(t) = I_i - i_{LS} = I_i - \frac{V_o}{2(L_S + L_M)}(t - t_0) \quad (2)$$

Case 2 $[t_1 < t < t_2]$: figure 3b)

A resonance begins between the parasitic capacitance C_P and the snubber inductance L_S in this case, which begins

Figure 2. Key wave shapes concerning the operational cases in the proposed converter.

with the turning-off of the main diode D_F . The current of the snubber inductance L_S increases, while the voltage of parasitic capacitance C_P decreases due to resonance. At $t = t_2$, when the voltage of parasitic capacitance C_P drops to zero, the energy transferring to the output side by transformer ends and this case is completed. The auxiliary transformer TR continues the DPT during Case 1 and Case 2. At the end of this case, the current of snubber inductance L_S reaches its maximum value I_{LSmax} . The following equations are valid for this case:

$$i_{LS}(t) = \frac{V_O}{2Z_1} \sin(\omega_1(t - t_0)) + I_i \quad (3)$$

$$v_{CP}(t) = V_o - \frac{V_O}{2} (1 - \cos(\omega_1(t - t_0))) \quad (4)$$

$$i_{LS}(t_2) = I_{LSmax} = \frac{V_O}{2Z_1}, \quad (5)$$

$$W_{LS}(t_2) = W_{LSmax} = \frac{1}{2} L_S I_{LSmax}^2. \quad (6)$$

Here

$$Z_1 = \sqrt{\frac{L_S}{C_P}}, \quad (7)$$

$$\omega_1 = \frac{1}{\sqrt{L_S C_P}}. \quad (8)$$

Case 3 $[t_2 < t < t_3]$: figure 3c]

At $t = t_2$, this case begins when the internal diode of main switch D_1 is turned by ZVS. The internal diode D_1 conducts the current that is above the input current $I_{LSmax} - I_i$. In the middle of this case, called the ZVT case, a control signal is applied to the gate of S_1 . Thus, a lossless turning-on by ZVT for the main switch S_1 is ensured. In terms of reducing circulation losses, it is useful to keep the duration of this case short. At $t = t_3$, this case ends when the gate signal of the auxiliary switch S_2 is interrupted. The following equations are valid for this case:

Figure 3. Equivalent circuit schemes of the operational cases in the new converter. (a) Case 1, (b) Case 2, (c) Case 3, (d) Case 4, (e) Case 5, (f) Case 6, (g) Case 7 and (h) Case 8.

$$i_{LS}(t) = I_{LS\max}, \quad (9)$$

$$i_{D1}(t) = I_{LS\max} - I_i. \quad (10)$$

Case 4 [$t_3 < t < t_4$: figure 3d]

At $t = t_3$, when the gate signal of auxiliary switch S_2 is interrupted, this switch is turned off by ZVS due to snubber capacitance C_s . In this case, the auxiliary diode D_3 is turned on by ZVS and a resonance starts among L_s , L_m and C_s . Thus, the leakage inductance energy of auxiliary transformer TR is recovered. When the currents of inductances

decrease, the voltage of the capacitance increases due to resonance simultaneously. At $t = t_4$, when the voltage of the snubber capacitance C_s reaches the level of the output voltage, the auxiliary diode D_4 is turned on by ZVS and this case is completed. The following equations are valid for this case:

$$i_{LS}(t) = i_{LSM} = i_{D4} = I_{LS3} \cos(\omega_2(t - t_3)), \quad (11)$$

$$v_{CS}(t) = V_o - I_{LS3} Z_2 \sin(\omega_2(t - t_3)). \quad (12)$$

Here

$$Z_2 = \sqrt{\frac{L_S + L_M}{C_S}}, \quad (13)$$

$$\omega_2 = \frac{1}{\sqrt{(L_S + L_M)C_P}}. \quad (14)$$

Case 5 $[t_4 < t < t_5]$: figure 3e]

During this case that starts with the turning-on of auxiliary diode D_4 , the energy accumulating at the snubber inductance L_S and the magnetization inductance L_m is discharged. The currents of these inductances are reduced linearly. At $t = t_5$, when the energies of inductances are exhausted, the auxiliary diodes D_3 and D_4 are turned off by the ZCS and this case ends. The following equations are valid in this case:

$$i_{LS}(t) = i_{LSM} = I_i - \frac{V_o}{L_S + L_M}(t - t_4), \quad (15)$$

$$i_{S1}(t) = \frac{V_o}{L_S + L_M}(t - t_4). \quad (16)$$

Case 6 $[t_5 < t < t_6]$: figure 3f]

This case is the off-case of the conventional high set-up PWM DC–DC converter. During this case, the filter inductance L_F is energized through the input voltage source. In this case, the snubber cell is inactive and the main switch S_1 conducts the input current. The following equation is valid for this case:

$$i_{S1}(t) = I_i. \quad (17)$$

Case 7 $[t_6 < t < t_7]$: figure 3g]

During this case, which starts when the gate signal of the main switch S_1 is interrupted, the parasitic capacitance C_p is charged linearly by constant input current while the snubber capacitance C_S is discharged. In this case, both C_p and C_S together ensure that the main switch S_1 is turned off by ZVS. At $t = t_7$, when the voltage of parasitic capacitance C_p reaches the output voltage, the voltage of snubber capacitance C_S drops to zero and this case ends. The following equation is valid in this case:

$$v_{CP}(t) = V_o - v_{CS} = \frac{I_i}{C_P + C_S}(t - t_6). \quad (18)$$

Case 8 $[t_7 < t < t_8]$: figure 3h]

This case starts when the main diode D_F is turned on by ZVS. The main diode is at on-state and the snubber cell is inactive during this case. When a control signal is applied to the gate of S_2 , it is returned to the initial conditions and the described eight cases are repeated. The following equation is valid for this case:

$$i_{DF}(t) = I_i. \quad (19)$$

3. Design method

Based on the discussion in the literature, design methods of the proposed active snubber cell can be summarized as follows:

- 1) The turning-on by ZCS of the auxiliary switch depends on the value of the snubber inductance L_S . Therewithal, the snubber inductance L_S is a major element to minimize the reverse recovery losses of main diode D_F . For this reason, the value of the snubber inductance is selected according to the following conditions:

$$L_S \geq \frac{V_o}{I_{imax}} 3t_{rr}. \quad (20)$$

Here, t_{rr} is the reverse recovery duration of main diode.

- 2) The magnetization inductance of high-frequency transformer L_m is set to the value of snubber inductance L_S . At the same time, the transformer turns ratio (N_p/N_s) is equal to one. Additionally, for $L_m > L_S$ and $n > 1$, the auxiliary diode D_2 is exposed to additional voltage stress. For $L_m < L_S$ and $n < 1$, the energy transfer capability of the auxiliary transformer is weak. Hence, L_m and L_S inductances are equal to each other:

$$L_S = L_M. \quad (21)$$

- 3) In order to ensure a better ZVS for the main switch, the duration over which the voltage of main switch arrives at the output voltage should be longer than the turning-off duration of the switch. The same conditions are also required for turning off by ZVS of the auxiliary switch. Hence, the snubber capacitance C_S should provide an exact ZVS for both the main switch and the auxiliary switch simultaneously. For this reason, the snubber capacitance C_S should satisfy the following equations:

$$C_S \geq \frac{I_{imax}}{V_o} t_{f-S1}, \quad (22)$$

$$C_S \geq \frac{I_{imax}}{V_o} t_{f-S2}. \quad (23)$$

Here, t_{f-S1} is the fall time of main switch and t_{f-S2} is the fall time of auxiliary switch.

4. Experimental results

The experimental set-up of the proposed converter illustrated in figure 4 is realized at 500 W and 100 kHz. Hence, the theoretical description of the proposed converter is experimentally verified.

In the experimental set-up, the filter capacitance C_F is 470 μ F, the filter inductance L_F is 1.5 mH and the snubber

Figure 4. Experimental set-up scheme of the new converter.

Table 1. The experimental parameters and the device values of proposed converter.

Devices	Part number	V (V)	I (A)	t_r (ns)	t_f (ns)	t_{rr} (ns)
S_1, S_2	STW26NM60N	600	20	25	50	370
D_F, D_3, D_4	QH12TZ600	600	10	–	–	20
D_2	HERAF1007G	800	10	–	–	80

Figure 6. Experimental waveforms of main switch under light load condition (200 V/div, 4 A/div, 1 μ s/div).

inductance L_S is 6 μ H. The snubber capacitance C_S is 4.7 nF and the value of parasitic capacitance is 1 nF. The values of both the magnetization inductance L_m and the secondary inductance are 6 μ H. The semiconductor device parameters used in the proposed converter are presented in table 1.

Figure 5 shows the experimental results of the proposed new converter. In figure 5a, the voltage and current wave shapes of the main switch are illustrated. The main switch is turned on by ZVT without the current and voltage

Figure 5. Experimental waveforms of semiconductor devices: (a) S_1 , (b) S_2 , (c) D_F , (d) voltage of C_S and the currents of L_S and D_2 (200 V/div, 4 A/div, 1 μ s/div).

Table 2. Loss analysis of the semiconductor devices in the HS and SS converters. $V_i = 200$ V, $V_o = 400$ V, $f = 100$ kHz.

I_O (A)	Hard or soft	Power losses (W)						P_i (W)	P_o (W)	η (%)
		S_1+D_1	D_F	S_2	D_2, D_3, D_4	Add.	Tot.			
1.25	HS	24.3	16.4	—	—	12.3	53	553	500	89.3
	SS	5.5	3.9	1.7	0.54	1.36	13	513	500	97.4

Figure 7. Efficiency graphics of the new converter for SS and HS operations.

overlapping and it is turned off by an exact ZVS. Therefore, the switching losses at turning-on are perfectly eliminated. Besides, the switching losses at the turning-off are significantly reduced for the main switch by the new snubber cell. Besides, any voltage or current stress does not happen across the main switch.

In figure 5b, the current and voltage wave shapes of the auxiliary switch are presented. The auxiliary switch is turned on by ZCS and off by ZVS. Therefore, total switching losses are significantly minimized for the auxiliary switch. Additionally, there is no voltage stress across the auxiliary switch. The current stress of auxiliary switch is reduced by DPT feature.

In figure 5c, the voltage and current wave shapes of the main diode are illustrated. The main diode is turned on by ZVS and turned off by ZCS. Hence, its switching power losses and reverse recovery losses are reduced. Moreover, there are no current or voltage stresses across the main diode.

In figure 5d, the voltage of snubber capacitance C_S and the currents of snubber inductance L_S and auxiliary diode D_2 are shown. It is clear from the figure that the voltage of C_S does not exceed the output voltage.

The proposed converter is operated at 150 W to prove that the proposed converter can be operated also at light loads. The current and voltage waveforms of main switch at light load are illustrated in figure 6. Additionally, loss analysis of semiconductor devices used in the proposed converter is made and it is presented in table 2.

The efficiency graphics of the presented new converter for SS and HS are presented in figure 7. The value of

converter efficiency is 89.3% under HS operation; it is measured to be about 97.4% under SS operation at nominal output power of 500 W.

5. Conclusion

In this study, a new high set-up DC–DC converter with active snubber cell is presented. The snubber cell of the proposed converter provides SS fully for main and auxiliary semiconductor devices. Current/voltage stress does not occur across the main semiconductor devices. The most important feature of proposed converter is its DPT. Some part of circulation energy is transferred to output side while SS is ensured for the main semiconductor devices. The current stress of auxiliary switch is significantly reduced. Moreover, the efficiency of converter is increased by DPT feature. Additionally, the proposed converter has simple construction, low cost and ease of application features.

As a result, the proposed new converter has many desired features of SS converters as ZVT and ZVS. Besides, it overcomes many drawbacks of the SS converters presented earlier. The theoretical analysis of the converter is confirmed with a 100 kHz and 500 W experimental set-up. Finally, the converter efficiency reaches 97.4% at nominal output power.

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