A fully integrated high IP1dB CMOS SPDT switch using stacked transistors for 2.4 GHz TDD transceiver applications

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MS received 18 February 2016; revised 5 September 2017; accepted 13 September 2017; published online 7 June 2018

Abstract. A transmit/receive (T/R) switch is an essential module of every modern time division duplex (TDD) transceiver circuit. A T/R switch with high power handling capacity in CMOS process is difficult to design due to capacitive coupling of radio frequency signals to the substrate. This paper proposes a single-pole-double-throw (SPDT) T/R switch designed in a standard Silterra 130 nm CMOS process for high-power applications like RFID readers. The results reveal that, in 2.4 GHz ISM band, the proposed switch exhibits a very high input P1dB of 39 dBm with insertion loss of only 0.34 dB and isolation of 40 dB in transmit mode but 1.08 dB insertion loss and 30 dB isolation in receive mode. Stacked thick-oxide triple-well transistors, resistive body floating and negative control voltages are used to achieve such lucrative performance. Moreover, the chip size of the designed switch is only 0.034 mm² as bulky inductors and capacitors are avoided. The Monte-Carlo and corner analyses confirm that the performance of the switch is also quite stable and reliable.

Keywords. CMOS; ISM band; SPDT; T/R switch; transceiver.

1. Introduction

Radio frequency (RF) switch is an essential module in RF communications systems. In RF transceivers, it is used to switch among different circuits and/or modules as well as to share them to make the design compact and cost-efficient. Because of the widespread mobile communication systems, much attention in RF transceiver research has been focused on high-performance integrated designs. Moreover, the continuous advancement of CMOS process makes it the most promising technology for realizing RF transceivers [1, 2]. As a result, RF switches used in RF communication circuits have evolved from implementations of PIN diode, PHEMTs, MESFETs, GaAs components, etc. to ones using CMOS because of problems like high power consumption, large size and long-term reliability [3, 4].

In a time division duplex (TDD) system, the same antenna is used for the reception as well as for the transmission of signal to improve system portability and reduce cost as shown in figure 1. Therefore, in every TDD transceiver, a transmit/receive (T/R) switch is necessary for its proper functioning. The switch performance is crucial for the performance of the entire system, because it is the first as well as the last stage of the transceiver and directly affects the quality of the transmitted or received signal [5].

In CMOS T/R switch fabrication, the critical design considerations include mainly low insertion loss (IL), high isolation and high power-handling capability (P1dB). However, these performances commonly are trade-offs with each other. Therefore, designing T/R switches with adequate performance becomes more challenging in bulk CMOS technology. To meet the performance requirements of T/R switches in standard CMOS technology, extensive research is going on all over the world [6]. Yamamoto *et al*

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Figure 3. Schematic circuit of the proposed T/R switch.

with large input power can be improved if the gate control voltage of the transistors is increased. Besides, to manage the high gate to channel voltage, thick oxide transistors are used in this switch. Triple-well transistor structure is implemented to realize a better isolation from the silicon substrate to minimize losses at high frequencies due to its low resistance and the parasitic capacitances connecting it with the channel [18].

The optimizations of the number of transistors and their aspect ratios are very important when designing a switch with a certain design goal. The additional transistors used in the transmit shunt arm of the switch (those replacing M3 in figure 2) will cause maximum power handling capability increased. On the other hand, the isolation in the receive mode of the switch (when this shunt arm is supposed to be conducting) is decreased due to a higher on-resistance from TX to ground. Decreasing the on-resistance by increasing the transistor width improves the isolation but it also decreases the P1dB point again. The same trade-off needs to be considered with the shunt transistors (those replacing M4 in figure 2) of the receive side of the switch.

For the transistors in the series part of the transmit side of the switch, a high W/L ratio is necessary to realize a high maximum current and to decrease the IL in the transmit mode. However, big transistor width also causes high drain-source capacitances, which leads to more coupling to undesired ports and hence results in a bad isolation in the receive mode. More transistors in transmit series arm (those replacing M1 in figure 2) of the switch will degrade the performance in the transmit IL to improve the isolation in the receive mode. The reverse is true for receive series arm of the switch.

One accountable problem of such a switch is the off-state current flowing through the shunt transistor, which increases largely if the drain-source voltage of the transistor gets too high [19]. Since the peak voltage of a 40 dBm signal to ground in a 50 Ω environment is equal to more than 30 V, it is useful to stack multiple transistors in series to reduce the drain-source voltage of a single transistor [20]. Therefore the transistors M2 and M3 of (figure 2) have to be replaced by multiple transistors in series, because these transistors need to be able to block the high power signal to ground path, in the transmission mode, to ensure reliability at high voltages. Figure 3 shows a schematic of the proposed switch using large transistor stacks. Table 1 gives the specifications of the transistors used:

For improved power handling capacity, body floating technique is employed to cut down the signal loss through body junctions of the transistors [18]. When the body of a

Table 1. Specifications of the utilized transistors in proposed T/R switch.

Place	Number of transistors in series	Width [μm]	Length [μm]
Transmit series	2	800	0.28
Transmit shunt	4	400	0.28
Receive series	5	300	0.28
Receive shunt	1	100	0.28

transistor is connected to its source, with increased input power, its drain-to-source voltage becomes negative so as to turn on the diode between drain and body and the input impedance of the transistor becomes lower. However, if the body floating technique is adopted, the body of the transistor is tied to the ground with a high resistance, which retains high input impedance of the transistor to maintain better power performance [21].

To handle high-voltage signals with usual MOS devices, device terminals are floated generally. In the CMOS process, substrate floating may degrade the performance due to the low resistivity substrate [18]. To solve the problem, triple-well NMOS devices are used in this design, which consists of a p-well embedded within a deep n-well to create an isolated body for the NMOSs from the p-substrate as shown in figure 4 [22]. Such an architecture detaches the body from the substrate and offers biasing the body of the transistor and deep n-well separately, and hence design robustness is improved. Moreover, higher control voltages can improve the power performance of the switch [17], and therefore a high control voltage of 2.4 V has been used. Negative voltage is applied at the bulk as well as p-well of the MOSs and the parasitic diodes between the channel and the bulk are reverse-biased; therefore the breakdown voltage is reached at higher input voltages, which increase the maximum voltage swing of the switch, i.e., the P1dB point. In addition to the negative p-well bias, the deep n-well is biased at 2.4 V to achieve a reverse biasing of the second diode between the transistor and the silicon substrate as well. This helps improve switch performance. At the gate and bulk of each transistor, large resistances of more than 100 k Ω were used to allow the gate and bulk node to float at RF, which stabilizes the gate to channel voltage and therefore improves the switch performance [23, 24].

3. Results and discussion

The proposed T/R switch is designed and simulated in Silterra 130 nm CMOS process. Design Architect (DA-IC) and IC station tools of Mentor Graphics have been used to

Figure 4. Isolated body triple-well NMOS structure.

Table 2. Effect of the bulk bias on switch parameters.

Parameters	V _{ctrl} = 2.4 V	V _{ctrl} =2.4 V
Bulk bias voltage [V]	−2.4	0
Insertion loss (transmit) [dB]	0.34	0.32
Insertion loss (receive) [dB]	1.08	1.05
Isolation (transmit) [dB]	40.3	39.3
Isolation (receive) [dB]	29.9	29.4
P1dB [dBm]	39	29

measure the performance of the switch. In this study, IL, isolation and power handling capacity of the switch are evaluated. Moreover, statistical analyses are also performed to verify the reliability of the switch.

A high control voltage of 2.4 V is used to improve the power performance of the proposed switch. The bulk nodes of the transistors are biased with a negative voltage. In comparison with connecting the bulk to DC ground, the P1dB point is increased greatly by 10 dB. The isolation is increased as well and although the IL gets slightly worse, the overall performance is better as illustrated in table 2. This is due to the fact that the negative voltage on the p-well as well as the substrate of the MOSs for which the parasitic diodes become reverse-biased and therefore the breakdown voltage is reached at higher input voltages, which elevate the P1dB point.

Figure 5 shows the IL and isolation of the switch over the frequency in both transmit and receive modes. As the operating frequency increases, the switch performance gets worse because of initiation of parasitic capacitances among the transistor terminals, which naturally increase their admittance as well as create unwanted signal paths between the ports or to the bulk node at high frequencies. As a result, for frequencies more than 10 GHz, both the IL and

Figure 5. Insertion loss and isolation performance of the switch.

Figure 6. Power handling performance of the switch.

Figure 7. FEOL corner analysis of the switch.

isolation of the switch, in both modes, are found to degrade rapidly.

Figure 6 shows the power handling capacity of the proposed switch, which is determined by input P1dB point. The switch provides a linear output as the input power is increased. The output power starts to drop at input power of 39 dBm, which is its IP1dB point. Beyond this point, the channel to ground diodes of the MOSs break down and the off-state leakage current of the stacked transistors comes to play, which leads to unwanted signal paths to the ground.

Figures 7 and 8 show the statistical analysis of the proposed switch. The FEOL corner analysis for TT, FF and SS corners is given in figure 7. For all the corners, the P1dB point remains almost stable. The IL is found to be better for FF corner and gets worse in SS corner. On the other hand, the isolation is the best in FF corner and worse in SS corner.

Figure 8. Monte-Carlo analysis of the switch.

In both cases, the mean deviation from TT for both corners is consistent. As all transistors or resistors used are large, a small conductivity variation does not affect the switch parameters strongly.

Figure 8 shows the Monte-Carlo simulation of the transmit IL and isolation of the switch. It can be seen that there is no large variation of the switch parameters of the Monte-Carlo analysis. For a total of 1000 number of runs, most values of the IL were within 0.32–0.36 dB and for isolation the values were within 39.5–41.0 dB. This indicates that the results obtained with Monte-Carlo models do not differ significantly for 1000 runs and the switch performance is quite stable and reliable.

Figure 9 shows the complete layout of the proposed switch. The chip area without pads and charge pumps for the positive and negative control voltages is about $0.16 \text{ mm} \times 0.21 \text{ mm} = 0.0336 \text{ mm}^2$. The core chip area of the proposed switch is kept to a minimum by avoiding inductor and capacitor usage in the design.

Compared with other CMOS switches, the proposed design exhibits the highest IP1dB point, lowest IL and a very competitive chip area. This is because most of the designs used inductors and/or capacitors to improve the performance. However, the capacitors and inductors require very large chip area compared with transistors and resistors. There are designs with low IL [16, 24] or with high isolation [5, 16, 23] but both of them have a much lower P1dB point and lower isolation or a much higher die area, respectively. This shows that the presented design exhibits a good balance between the key parameters for 2.4 GHz ISM band applications. A comparative study on the switch performance in literatures is illustrated in table 3.

Figure 9. Core layout of the proposed switch with area 0.16 mm×0.21 mm.

Table 3. Performance comparison table of the T/R switch.

Ref.	Year	CMOS technology	Isolation [dB]	Transmit IL [dB]	Receive IL [dB]	P1dB [dBm]	Die area [mm ²]	Control voltage [V]
[13]	2006	0.18 μ m	35	0.7	–	21.3	0.03	1.8/0
[19]	2007	0.13 μ m	31	0.8	1.2	28	0.09	3.3/0
[14]	2008	0.50 μ m	–	1.085	1.102	25.33	–	1.2/0
[18]	2008	65 nm	28	0.8	1.6	30.8	0.2	2.5/0
[20]	2009	0.18 μ m	28.4	0.94	1	30	2.25	3/0
[24]	2010	0.18 μ m	23	0.5	1.1	33.8	0.203	–
[5]	2011	0.18 μ m	43	1.1	–	21.5	0.672	–
[16]	2012	0.18 μ m	33	0.62	0.7	29.2	0.125	1.8/0
[23]	2012	32 nm	32	1.3	1.1	34	–	1.8/0
[21]	2014	0.18 μ m	24.5	0.72	1.14	22.4	0.037	1.8/0
This work		0.13 μ m	30	0.34	1.08	39	0.034	2.4/–2.4

4. Conclusions

There is no alternative to a high-performance T/R switch in every RF transceiver for its optimum performance. The proposed switch using stacked transistors with body floated and negative body bias technique shows a good trade-off among IL, isolation and power handling capacity. It exhibits an IL of 0.34 dB in transmit and 1.08 dB in receive mode at 2.4 GHz. At the same time, the isolation is higher than 40 dB in transmit and around 30 dB in receive mode and the input P1dB is 39 dBm. The active layout area is also kept quite

small, only 0.034 mm², because large area components like inductors or capacitors are avoided. Therefore, the production costs are very low. Moreover, the stability and reliability of the switch, determined by statistical analyses, make it very much suitable for 2.4 GHz wireless terminals.

Acknowledgements

This work is supported by the research Grant Economic Transformation Programme (ETP-2013-037) from

Universiti Kebangsaan Malaysia and the Ministry of Science, Technology and Innovation (MOSTI), respectively.

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