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Design and analysis of hybrid optical and electronic buffer based optical packet switch

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Abstract. Optical packet switching has the potential to be used as next generation data transfer technology. This paper, introduces an Arrayed Waveguide Gratings (AWG) switch where hybrid buffer (electronic + optical) is used for the buffering of contending packets. Power budget analysis has been carried out under various switch designs. Comparison of optical and electronic buffering is done in terms of power required for the correct operation of the switch. Energy consumption per bit is also evaluated for both optical and electronic buffers for various buffering time ranges from nano-seconds to milli-seconds. In the switch analysis it has been found that, amplified switch requires five times less power, in comparison to un-amplified switch for correct operation. Energy consumption analysis reveals that for shorter duration storage, optical buffer would be a better choice.

Keywords. Optical packet switch; bit error tate (BER); power consumption.

1. Introduction

In the modern era of telecommunication environment, the need and requirement of internet traffic is increasing in a very rapid pace. The requirement of higher bandwidth is increasing with the time in these developing circumstances. This requirement is raised because of the data centric applications such as video on demand, internet TV, and so on. The fiber optical network has turned out to be the core infrastructure of telecommunication and data networking. One of the significant technologies is the Optical Packet/Burst switching which may be quite valuable at the time of building networks to meet this growing bandwidth requirement. Due to the use of the low latency, high bandwidth and high throughput, the optical packet/burst switching technique is being anticipated as upcoming generation high speed technology of data transferring [1, 2]. This paper concentrates on optical packet switching. The execution of optical network is made out of switches also known as router. Each one of these switches are optical or it may be electronical. The principle goal of switching is routing the incoming packet to its right landing output port. The main problem with the network is the efficient designing of the switch, which can carry out the operation of the switching in a perfect way with high rates of data. The technology used at the present time is a blended methodology. This is due to the non-feasibility of optical processor. In this methodology, data propagates in the optical domain and monitoring functions are completed by the electronics. The above mentioned blended methodology is alluded as the technology of photonic packet switching. In this switching technology, huge photonic packet switches will most likely depend on electronics for the purpose of controlling functions, and the buffering and packet routing is being performed by optical means [3, 4].

One of the major drawbacks of Optical Packet Switching (OPS) technology is the unavailability of optical RAM. Thus, in an alternative approach fiber delay lines (FDLs) are used. In these FDLs storage is very limited due to the physical layer constraints like dispersion, crosstalk and noise [5–8]. In this work, we propose to design a switch where hybrid buffering scheme (both electrical RAMs and FDLs) will be used for the contention resolution of packets.

In optical packet switching, the buffering capacity is limited as the optical equivalent of electronic random access memory is not developed yet. Current optical buffers heavily rely on fiber delay lines to create temporary buffer, which delay the data packets rather than storing them. Fiber delay lines in feed forward, feed backward and in recirculating configurations are used. Recirculating loops based buffer is a preferred choice over other configurations [1, 2]. These fiber delay lines use WDM (Wavelength Division Multiplexing) to hold multiple packets in a single piece of fiber. The recirculating type delay lines provide a large number of choices of delay values. In fiber loop, packets are stored using the WDM, thus additional components like

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splitter, combiner, De(Mux), TWC (Tunable Wavelength Convertor) and SOA (Semiconductor Optical Amplifier) etc. are needed to allow packet-by-packet processing in case of read/write operation. To compensate the loss of these components, generally EDFA (Erbium-Doped Fiber Amplifier) is placed in loop buffer [16]. Thus, buffering time is limited due to the recirculation limits. This recirculation count is a major concern in FDL based buffers. In addition to this, other limitations are:

(i) Random access is not possible, as packet can be retrieved from the buffer at the integral multiple of slots durations.
(ii) Length of the loop should be slightly larger than packet size.
(iii) Large size buffer is not feasible, due to bulky nature and recirculation counts.

In few applications packet loss rate of the order of 10^{-9} is desirable; and to obtain such low loss a buffer of some hundreds of FDLs will be needed which will cause degradation in signal quality. Therefore packets need to be regenerated by either all-optical or by O/E (Optical to Electrical) conversion. Both of these methods will increases the complexity.

In electronic buffering, packet-by-packet electronic buffering has been done using optical serial to parallel (S/P) conversion to match the speed differential between optical fiber transmission and electronic memory read/write operation [9]. However, speed cannot be exactly matched due to the multiplexing limits. Still speed can be enhanced to reduce the speed difference.

This article is organized in five sections. Section 2 of the paper, discusses the related work and pros and cons of the recently published switch designs. In section 3, proposed design is discussed along with mathematical formulation for BER evaluations. Section 4 elaborates the results in terms of BER and power dissipation analysis. Finally, section 5 discusses the major conclusions.

2. Related work

Photonic packet switches are defined as elastic-buffered or passive-buffered. At this point, the word passive-buffered indicates just passive delay lines, implemented in the form of fiber loops. The typical kind of optical buffers also known as recirculating buffer which makes the recirculation of the stored packets rather then holding them stationary or statically in memory. Multiple packets could be stored in a single fiber loop by making use of WDM technology.

Due to the gathering of noise in the fiber loop memory, the depth of the fiber loop memory cannot go more than a fixed number of recirculations. In other words, this means that we are not permitted to store more than a certain number of packets for any specific output. In the fiber loop, the accumulation of noise is proportional to the number of wavelengths that is utilized to save the packets in the event of contention. This results in a restriction on the numeric figure of wavelengths that could be utilized in the fiber loop. These considerations denote that photonic switches will require algorithms that will make use of buffers in an effective manner, as per the inherent switch limitations.

In 2008, Li and Wai proposed the concept of hybrid buffer, by stating the various shortcoming of optical fiber delay lines buffers [9]. They also stated that, for very low packet loss rate, large buffer space would be required, and optical implementation of such buffers will make buffer bulky.

Recently in the LIONS (Low-latency Interconnect Optical Network Switch) project, electronic buffering is proposed as shown in figure 1. Here, Arrayed Waveguide Grating Router (AWGR) is used to handle incoming packets. In case of contention of packets they are put in the buffer by tuning their wavelengths appropriately. AWGR is a WDM based device where more than one wavelengths can appear at one common input/output. Here, the WDM packets approaches to the buffer are first de-multiplexed via 1: *N* demultiplexer, and after O/E conversion packets are stored in shared memory [10]. On the basis of output, queueing structure in the shared memory is organized and hence the packets having same destination should be sent out serially towards the same output ports. While retrieving from the electronic buffer, first E/O (Electrical to Optical) conversion takes place, thereafter they are multiplexed and appear at the input port of the AWGR and depending on the wavelengths of the packets they appear at different output port of the AWGR, from there they can be routed to destined ports.

Recently, Shukla *et al* have investigated AWG-based switch under various design modifications [11–18]. This architecture is very efficient in terms of the buffering of contending packets to resolve contention among packets. In this design, in each fiber delay lines using WDM a

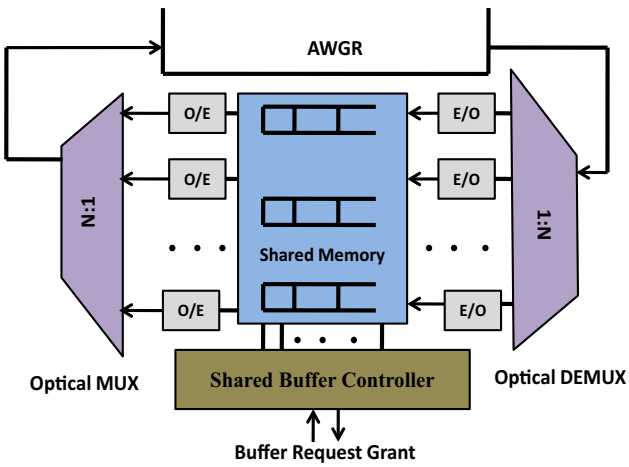

Figure 1. Buffer schematic in LIONS project.

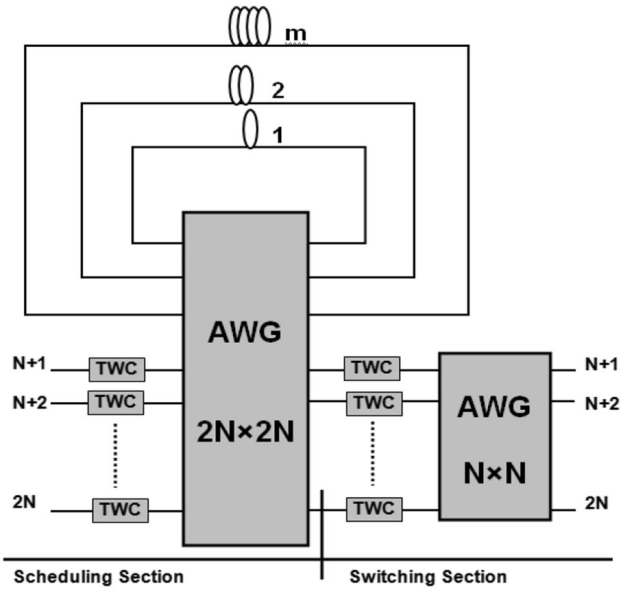

Figure 2. Design of AWG-based switch with optical buffer.

maximum of N packets can be stored one for each output port (figure 2). Moreover, buffer is created using pieces of fiber only without using any additional components. Thus signal quality degradation is very less inside the buffer.

This switch consists of scheduling AWG (2N × 2N) and switching AWG (N × N). Here, it is noticeable that AWG and AWGR are used analogously. AWG is cyclic device, and a packet arriving at input port *'i'* having wavelength λ_k will be routhed to output port $j = (i+k) \text{mod} N$, while N is the inputs/output ports of AWG. Thus by selecting the wavelength of input packets (using TWCs) they can be routed to any output port of the scheduling AWG. In case of contention, by choosing the wavelengths appropriately (following routing pattern of AWG) packets are placed in different buffer modules. In each module at most N packets can stay one for each output. Thus in m module at most mN. Length of module 1 is equal to one slot duration and while for m^{th} module it is of m slots. Thus, depending on the required amount of delays various modules can be selected for buffering of packets.

In this design packets leave the buffer on the wavelength, they were stored, thus they will appear at the various port of the scheduling AWG, form where by tuning their wavelengths appropriately packets can be sent to the destined outputs.

In this architecture low packet loss is possible, and all the packets are stored in FDLs. The drawback of the architecture is its limited storage and packet cannot be stored for longer duration.

To overcome these limitations, researchers have proposed buffering in electronic domain through O/E conversion. In this article, a hybrid optical buffer is being proposed that merges the advantages of both fast electronic buffers and fiber loop optical buffering. Numerous sets of fiber loops and electronic buffering modules are joined and develop the proposed hybrid optical buffer. Incoming packets are initially put in the fiber loops for storing on a temporary basis. In the event that packet can not be sent out after a particular interval of, the conversion of packet will be done and it will be stored in the electronic memory. It is shown that the gradual operations of data conversion and electronic memory read/write will not create any issue if there are many K fiber loop modules implanted, where K is not dependent of the system loading and packet loss rate.

As a result, we can use big electronic memory in order to decrease the loss of packet. The hybrid optical buffers that are proposed will remarkably make the operation of optical packet routing node quite simple by making use of the current technology.

Here, buffer is hybrid i.e., both optical and electronic buffer is used. In the proposed design, first optical buffer is used and if necessary electronic buffer is utilized. Using this technique following advantages can be gained:

(i) Optical storage will allow high speed data transmission.
(ii) It is also assumed that, in electronic buffer data will stay at least for $B+1$ optical slots. During this time, first packet will be electronically stored and will be retrieved from electronic buffer and again E/O conversion will be ready to leave the buffer, thus in terms of speed limitations.

For hybrid buffer, first notable work was proposed by Lim *et al* [19]. In their design hybrid buffer uses fiber delay line (FDL) buffer as the prime buffer and a shared electronic buffer as the supplementary buffer. In the simulation results it has been found that the use of the electronic buffer together with the FDL buffer can significantly reduce the number of FDL required for lower packet loss. In this paper, analysis is concentrated only on network layer parameters in terms of packet loss rate.

In recent work, Samoud *et al* have also considered hybrid buffering based optical switch and they compared their switch with bufferless and all-optical buffer based designs [20]. In performance evaluation, packet quality of service is also included. In simulation study they found that with only a few electronic ports buffer, along with optical buffer can significantly improve the packet loss rates and the sustainable system load when compared to an all-optical bufferless switch and can meet the requirement of different packets classes.

In very recent work, Wang and co-workers also investigated hybrid optical switch where both electronic and optical buffer is used for contention resolution [21]. They carry out simulation study in terms of packet loss rate while considering use of FDL and FDL dimensioning. Finally, power consumption analysis is also carried out to prove the hypothesis of hybrid buffering.

The above mentioned papers discuss the use of hybrid buffer while considering network payer parameter like packet loss rate. However, in any switch design physical layer analysis is also important, and how packet size and bit rate can change the power budget and power dissipation analysis of the switch. In this paper we have made an attempt to address these issues and. shown that for small durations optical buffering is a better choice as it saves O/E/O conversion and even power requirement is lesser. However, in case of larger buffer, hybrid scheme where both optical and electronic buffer will be used. Moreover, it is also shown that size of packet and bit rate must be considered while choosing electronic and optical buffer.

3. Proposed design

In this paper, a hybrid buffer design is proposed, where, '*B'* is fiber delay lines in optical domain and '*E*' electronic buffer will be used for the buffering of contending packets (figure 3). The electronic buffer scheme is same as considered in [10]. In this, switch principle of operation is similar to the switch in figure 2, except in the buffer where in addition to FDL, shared electronic buffering scheme as in figure 1 is also considered. Now in case of contention, both FDL and electronic buffering can be used, depending on the desired delay. Considering figure 3, if buffering of less than 'B' slots is desired then optical buffering is a preferred choice, otherwise electronic buffering will be used.

3.1 *Uncompensated switch*

In the first design of the switch, packets pass through the switch without any amplification (figure 3). Thus, each packet passing through the switch looses its power before arriving at the actual output port of the switch. The losses suffered by packets also depend on paths followed by them. In case of direct transfer of packets loss is lesser in comparison to transfer via buffer.

The analysis of the switch is considered in terms of BER analysis at different power levels and energy dissipated per bit.

3.2 *Power analysis*

In this section, loss and power analysis are proposed. Here the insertion loss of the components is represent by '*L*' with superscript denotes the size and subscript denotes the component type. The total loss is modelled as '*A*', direct path is denoted by suffix '*D*', optical buffered path by suffix '*B*' and electronic buffered path by suffix '*EM*'.

The loss of the signal power passing through directly towards the output is

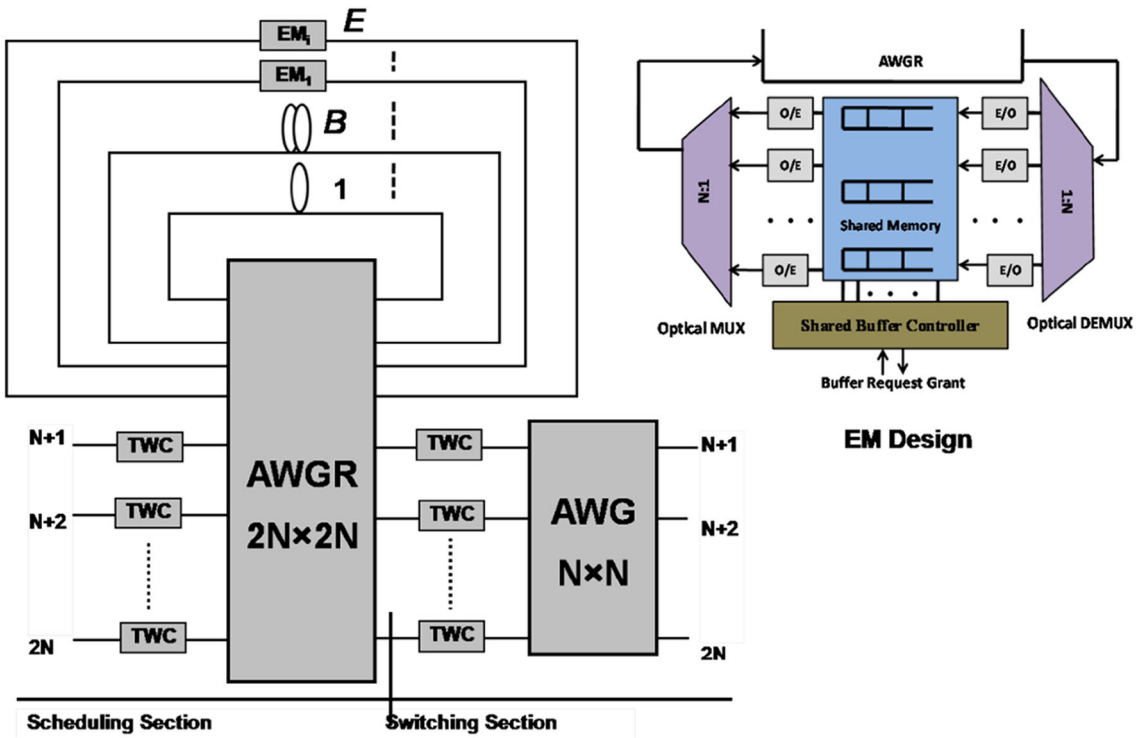

Figure 3. Design of AWG-based switch with hybrid buffer.

$$A_T^D = L_{TWC} L_{AWG}^{2N} L_{TWC} L_{AWG}^N \quad (1)$$

Thus the power available at the output of the switch is

$$P_{out}^D = P_{in} A_T^D \quad (2)$$

Similarly, the loss of the signal power when packet passes through the optical buffer is

$$A_T^B = L_{TWC} L_{AWG}^{2N} L_B L_{AWG}^{2N} L_{TWC} L_{AWG}^N \quad (3)$$

The output power is

$$P_{out}^B = P_{in} A_T^B \quad (4)$$

The loss of the signal power when packet passes through the electronic buffer is

$$A_T^{EM} = L_{TWC} L_{AWG}^{2N} L_{EM} L_{AWG}^{2N} L_{TWC} L_{AWG}^N \quad (5)$$

Where, $L_{EM} = L_{DEMUX} L_{O/E} L_{E/O} L_{MUX}$

$$P_{out}^{EM} = P_{in} A_T^{EM} \quad (6)$$

In case of optical buffering for direct transfer of packets the loss suffered is 10 dB. In case of packet passes through the optical buffer the loss suffered is 13.2 dB, while the suffered loss in case of electronic buffering is 19 dB.

3.3 *Noise analysis*

The generated noise components at the receiver are shot noise and thermal noise variances are denoted by σ_s^2 and σ_{th}^2 respectively [17]. For the bit b the different noise components at the receiver are

$$\sigma_s^2 = 2qRPB_e$$

$$\sigma_{th}^2 = \frac{4K_B T B_e}{R_L} \quad (7)$$

The total noise variance ($\sigma^2(b)$) can be obtained as

$$\sigma^2(b) = \sigma_s^2 + \sigma_{th}^2.$$

Finally BER can be obtained as

$$BER = Q\left[\frac{I(1) - I(0)}{\sigma(1) + \sigma(0)}\right] = Q\left[R\left(\frac{P(1) - P(0)}{\sigma(1) + \sigma(0)}\right)\right] \quad (8)$$

$Q(x)$ is error function. AWG specifications are given in table 1. The description of the above parameters with typical values is detailed in table 2.

3.4 *Compensated switch*

In the second part of the work, physical losses of the packets while traversing through the switch is compensated by using a variable gain amplifier SOA. Thus, depending on the path of the packets (direct/via buffer) losses of different packets can be compensated (figure 4).

Table 1. AWG specifications.

Specification	Value
Number of channels	40
Channel spacing	100 GHz
Operating wavelengths	ITU grid
Insertion loss	3.0 dB
Adjacent channel crosstalk	26 dB

The loss of the signal power passing through directly is

$$A_T^D = L_{TWC} L_{AWG}^{2N} L_{TWC} L_{AWG}^N \quad (9)$$

Thus the power at the output of the switch is

$$P_{out}^D = P_{in} + n_{sp}(G-1)h\nu B_0 A_T^D / L_{TWC} = P_s + P_{sp} \quad (10)$$

Assuming that SOA compensates the loss incurred inside the switch.

The loss of the signal power when packet passes through the optical buffer is

$$A_T^B = L_{TWC} L_{AWG}^{2N} L_B L_{AWG}^{2N} L_{TWC} L_{AWG}^N \quad (11)$$

$$P_{out}^B = P_{in} + n_{sp}(G-1)h\nu B_0 A_T^B / L_{TWC} = P_s + P_{sp} \quad (12)$$

The loss of the signal power when packet passes through the electronic buffer is

$$A_T^{EM} = L_{TWC} L_{AWG}^{2N} L_{EM} L_{AWG}^{2N} L_{TWC} L_{AWG}^N \quad (13)$$

Where, $L_{EM} = L_{DEMUX} L_{O/E} L_{E/O} L_{MUX}$

$$P_{out}^{EM} = P_{in} + n_{sp}(G-1)h\nu B_0 A_T^{EM} / L_{TWC} = P_s + P_{sp} \quad (14)$$

Due to square law detection by the photo detector in the receiver, various noise components are generated. These noise components are shot noise, ASE-ASE (Amplified Spontaneous Emission) beat noise, sig-ASE beat noise, shot-ASE beat noise and thermal noise variances are denoted by σ_s^2, σ_{sp-sp}^2, σ_{sig-sp}^2, σ_{s-sp}^2,and σ_{th}^2, respectively [17]. For the bit b the different noise components in the receiver area

$$\sigma_s^2 = 2qRP_s B_e$$

$$\sigma_{sp-sp}^2 = 2R^2 P_{sp}(2B_0 - B_e)\frac{B_e}{B_0^2}$$

$$\sigma_{sig-sp}^2 = 4R^2 P_s P_{sp}\frac{B_e}{B_0}$$

$$\sigma_{s-sp}^2 = 2qRP_{sp}B_e$$

Table 2. List of parameters and their value [17].

Parameters	Symbol	Value
Size of the switch	N	16
Total buffer space	$B_T = (B+E)$	16
Population inversion factor	n_{sp}	1.1
Gain of the amplifier	G	Varies
Speed of light	c	3×10^8 m/s
Refractive index of fiber	n	1.45
Responsivity	R	1.28 A/W
Electronic charge	e	1.6×10^{-19}C
Electrical bandwidth	B_e	20 GHz
Optical bandwidth	B_o	40 GHz
TWC insertion loss	L_{TWC}	2.0 dB
Loss of scheduling and switching AWG (32 channels)	L_{AWG}	3.0 dB
Loss of the fiber loop	L_{FDL}	0.2 dB/km
Loss of SOA	L_{SOA}	1 dB
Plank constant	h	6.6×10^{-34} Js
Boltzmann constant	K_B	1.38×10^{-23} $m^2kgs^{-2}K^{-1}$
Temperature	T	300 K
Load resistance	R_L	300 Ω
Loss of demux (32×32)	L_{DEMUX}	3.0 dB
Loss during O/E conversion	$L_{O/E}$	1.0 dB
Loss during E/O conversion	$L_{E/O}$	1.0 dB
Loss of mux (32×32)	L_{MUX}	3.0 dB
Input power	P_{in}	0.5–20 μW
Photo-current sampled by bit 1	$I(1)$	μA–nA (varies)
Photo-current sampled by bit 0	$I(0)$	μA–nA (varies)
Standard deviation of noises (bit 1)	$\sigma(1)$	Varies
Standard deviation of noises (bit 0)	$\sigma(0)$	Varies
Power received for bit1	$P(1)$	Varies
Power received for bit 0	$P(0)$	Varies
Noise power	P_{sp}	Varies

$$\sigma_{th}^2 = \frac{4K_BTB_e}{R_L} \tag{15}$$

The total noise variance (σ^2) can be obtained as

$$\sigma^2 = \sigma_s^2 + \sigma_{s-sp}^2 + \sigma_{sp-sp}^2 + \sigma_{sig-sp}^2 + \sigma_{th}^2 \tag{16}$$

The BER again will be obtained from Eq. (8).

4. Results

In this section, various results are presented. Firstly, fiber loop length is evaluated; thereafter BER analysis results are given under various configurations. Finally, energy dissipation analysis is presented.

4.1 *Fiberloop length*

Considering that the packet duration is equal to the slot length. Here the duration of the slot which is equivalent to the length of fiber can be calculated as

$$L_{FDL} = \frac{cb}{nB_r} \tag{17}$$

Here $c = 3\times10^8$ m/s represents the speed of the light, b represents the total number of bits stored in the fiber delay lines, n is the refractive index and B_r is the bit rate. The fiber length L_{FDL} is for loop 1 and $2L_{FDL}$ for loop 2 and so on. Thus the maximum length of the fiber is mL_{FDL}. Considering 1500 bytes packet at the data rates of 40 Gbps, is equivalent to 0.3 μs and for example, considering 10 optical fiber delay lines thus time equivalent to 3 μs. Thus minimum delay provided by electronic buffer will be of 3 μs.

4.2 *BER analysis*

Tables 1 and 2 give the details of parameters and their values used in calculations. In table 3, input signal power vs. BER for a bit is shown, while packet directly passes through the switch, i.e., buffer is not used.

On can clearly verify that, as the power increases BER also improves. In optical networks the acceptable limits for

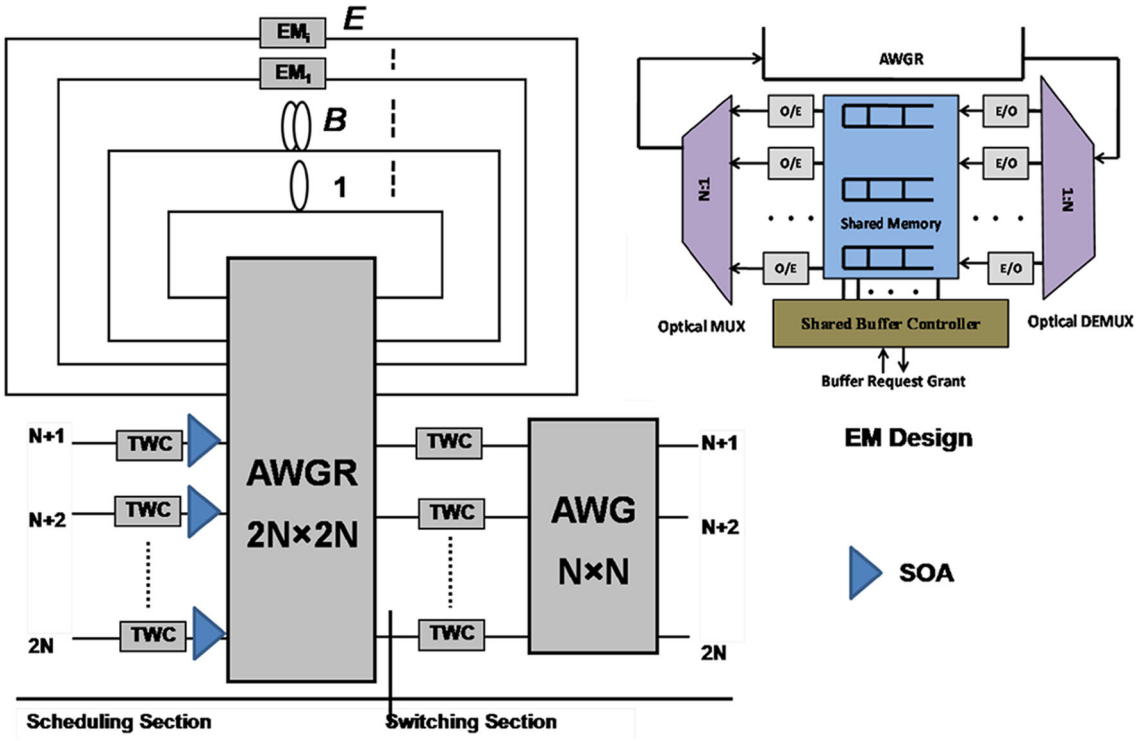

Figure 4. Design of AWG-based switch with hybrid buffer and SOAs.

Table 3. Power vs. BER for direct transfer of packets.

Power (μW)	BER
1	8.49×10^{-6}
1.1	2.13×10^{-6}
1.2	5.27×10^{-7}
1.3	1.27×10^{-7}
1.4	3.04×10^{-8}
1.5	7.11×10^{-9}
1.6	1.64×10^{-9}
1.7	3.73×10^{-10}
1.8	8.39×10^{-11}
1.9	1.86×10^{-11}
2.0	4.1×10^{-12}

Table 4. Power vs. BER for transfer of packets via optical buffer (uncompensated switch).

Power (μW)	BER
2.0	8.21×10^{-6}
2.5	2.49×10^{-7}
3.0	6.75×10^{-9}
3.5	1.66×10^{-10}
4.0	3.81×10^{-12}
4.5	8.18×10^{-14}
5.0	1.66×10^{-15}

BER$\leq10^{-9}$ or in some applications it is considered to be BER$\leq10^{-12}$. To attain a BER of 10^{-9}, the minimum amount of required power is 1.6 μW, and to achieve BER$\leq10^{-12}$, the required amount of power is more than 2 μW. In table 4, Power vs. BER for transfer of packets via optical buffer is shown. For BER$\leq10^{-9}$, the required power is 3.5 μW for BER$\leq10^{-12}$, the required amount of power is more than 4 μW. Thus, it can be summarized that if two packets are given, the same input power and one of them transmitted directly and other one via buffer, then the packets will have different BER at the output of the switch.

In table 5, Power vs. BER for transfer of packets via electronic buffer is shown. For BER$\leq10^{-9}$, the required power is 13 μW for BER$\leq10^{-12}$, the required amount of power is more than 17 μW. Thus with the electronic buffer the required amount of power increases by nearly four times.

In the previous results the loss suffered by the packets is not compensated. In the next part of the work, a SOA is placed at each input port of the switch just after the TWC which will fully compensate the loss suffered by packets.

In table 6, Power vs. BER for transfer of packets via optical buffer is shown. For BER$\leq10^{-9}$, the required power is 0.6 μW and for BER$\leq10^{-12}$, the required amount of power is more than 0.8 μW. Thus, comparing with earlier results (table 4) the required power reduced by more than a factor by 5. Thus an addition of *N* SOAs reduces the power

Table 5. Power vs. BER for transfer of packets via electronic buffer (uncompensated switch).

Power (μW)	BER
10	2.29×10^{-7}
11	3.78×10^{-8}
12	6.09×10^{-9}
13	9.55×10^{-10}
14	1.47×10^{-10}
15	2.22×10^{-11}
16	3.30×10^{-12}
17	4.18×10^{-13}
18	6.93×10^{-14}
19	9.83×10^{-15}
20	1.38×10^{-15}

Table 6. Power vs. BER for transfer of packets via optical buffer (compensated switch).

Power (μW)	BER
0.5	1.80×10^{-8}
0.6	5.32×10^{-10}
0.7	1.55×10^{-11}
0.8	4.48×10^{-13}
0.9	1.28×10^{-14}
1.0	3.64×10^{-16}

Table 7. Power vs. BER for transfer of packets via electronic buffer (compensated switch).

Power (μW)	BER
0.5	2.63×10^{-8}
0.6	8.43×10^{-10}
0.7	2.67×10^{-11}
0.8	8.39×10^{-13}
0.9	2.60×10^{-14}
1.0	8.06×10^{-16}

requirement by 5. However, the cost of the switch is increased by the cost of N SOAs.

In table 7, Power vs. BER for transfer of packets via electronic buffer is shown. For BER$\leq10^{-9}$, the required power is 0.6 μW and for BER$\leq10^{-12}$, the required amount of power is more than 0.8 μW. Thus, both electronic and optical buffer requires same amount of power.

The BER results are summarized in figure 5. It is clear from the graph that the unamplified switch with electronic requires high power in comparison to other configurations. However, the amplified system requires less power and it is same for both optical and electronic buffers. Thus when signal power, is in sub-micro level, then electronic and optical buffer requires same input signal power for the correct operations of switch.

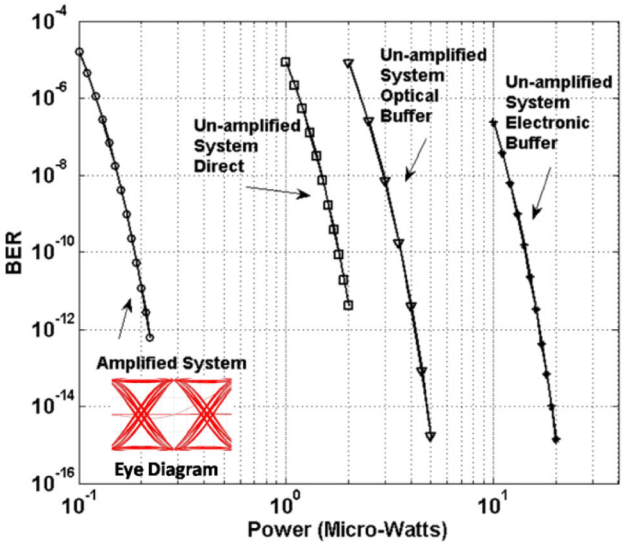

Figure 5. BER vs power for various switch configurations.

4.3 *Energy consumption analysis*

In recent times many studies have been published, regarding the energy required per bit, and in general it has been concluded that electronic systems consume less energy per bit [22–25]. But it is true when in the buffer; both optical and electronic signals are separated out, and processed individually. However, in the considered design optical signals in the buffer are not processed, thus re-investigation is necessary.

The total energy (E_T) consumed per bit in the switch can be written as

$$E_T = NE_{TWC} + E_{AWG}^{2N} + BE_{FDL} + EE_{EM_i} + NE_{TWC} + E_{AWG}^{N} \quad (18)$$

Where,

$$E_{EM_i} = \frac{B_H}{B_P}\left[E_{DE(MUX)} + E_{O/E/O} + E_{CMOS}\right] \quad (19)$$

An optical packet consists of two parts i.e., header and payload, and they are detachable. At each intermediate node, header is separated from the payload and after O/E conversion is sent to the control unit. In general, header is encoded at lower bit-rate (B_H) thus enabling electronic controlling. However, payload bit rate (B_P) is much higher for allowing fast data transfer. However, in case of very fast processing both bit rates can be equal. Thus we have $B_H \leq B_P$. The energy dissipation per bit in various devices is given in table 8. The energy values are in pJ. In table 9, comparison of FDL with CMOS electronic memory in terms of energy dissipation per bit at the data rate of 40 Gbps for various packet sizes is given. It is clear from the table that electronic memory dissipation energy is

Table 8. Energy consumption per bit in various devices [22].

Specification	Symbol	Value (pJ)
Energy consumption in TWC	E_{TWC}	2.1
Energy consumption in AWG	E_{AWG}	10
Energy consumption in $E_{O/E/O}$ process	$E_{O/E/O}$	0.5
Energy consumption in De(mux)	$E_{DE(MUX)}$	10
Conversion factor	B_H/B_P	0.25

independent of packet size, while in case of FDL it is dependent on packet size. This is an expected result because FDL length is dependent on packet size as discussed above.

The above expression can be simplified by considering $N = 16$ and $B_T = 16$, then Eq. (18) can be simplified to,

$$E_T = 32E_{TWC} + E_{AWG}^{2N} + BE_{FDL} + (16 - B)E_{EM_i} + E_{AWG}^{N} \tag{20}$$

After inserting the values of the different components of energy consumption we get:

$$E_T = \begin{cases} 181.6 - 5.275B \text{ for } 100\,\text{ns} \\ 181.6 - 5.275B \text{ for } 10\,\mu\text{s} \\ 181.6 - 4.275B \text{ for } 1\text{ms} \end{cases} \tag{21}$$

Total energy consumption is shown in (Eq. (21)) for different buffer storage of 100 ns, 10 µs and 1 ms. For the various values of optical and electronic buffers results are drawn in figure 6. In case of 100 ns and 10 µs, buffering the energy consumption per bit for all optical buffer i.e., 16, is 97.2 nJ, while for all electronic buffers the energy consumption is 181.6 nJ (figure 6). Thus, energy dissipation in electronic buffer is higher in comparison to optical buffers. In case of buffering of 1 ms, still optical buffers are better, but the energy consumption increased to 113.2 nJ. However, in optical switches (re-circulating type) where individual packets are stored in the buffer for 1 ms duration, electronic buffers is much superior as compared to optical buffers, as the energy consumption in fiber is ten times

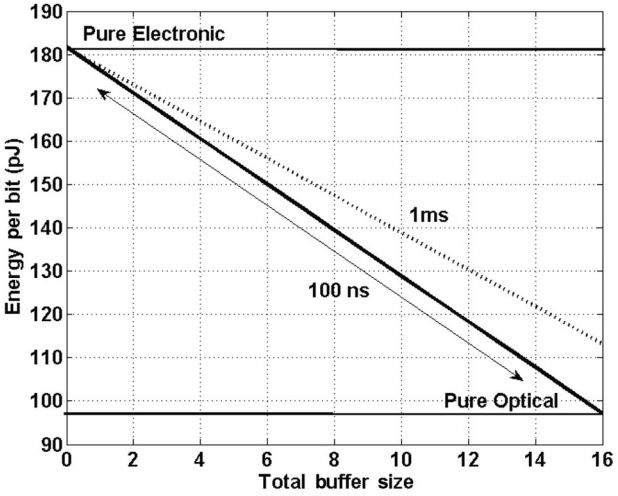

Figure 6. Energy per bit(pJ) vs buffer.

Table 9. Power and energy dissipation for 40 Gbps delay-line buffers [24].

(a)			
		100 ns (4kb)	
	E_{bit}	Power	Area (cm^2)
Fiber	2×10^{-3} fJ	80 nW	20 m (L)
CMOS	0.1 pJ	8 mW	2×10^{-5}
(b)			
		10 µs (400kb)	
	E_{bit}	Power	Area (cm^2)
Fiber	1.1 fJ	44 µW	2 km (L)
CMOS	0.1 pJ	8 mW	2×10^{-3}
(c)			
		1 ms (40Mb)	
	E_{bit}	Power	Area (cm^2)
Fiber	1 pJ	40 mW	200 km (L)
CMOS	0.1 pJ	8 mW	2×10^{-1}

more than the electronic buffers and longer delay of packets in the buffer will lead to quality degradation (due to the accumulation of noises).

However, as storage time increases, the technology demands shift from optical to electrical buffering as in optical data centers. We will look into optical data centers storage issues in our future work.

5. Conclusions

Optical packet switching is considered as technology for the future. This paper investigated an AWG-based optical switch with hybrid (optical +electronic) buffers. Physical layer analysis was performed to obtain BER analysis under various switch configurations. It has been found that, amplified switch required lesser amount of power, and required power was equal in case of optical and electronic buffers. Power consumption analysis was also performed and it was found that electronic buffer would only be needed when longer duration buffering was desirable, otherwise optical buffering was preferable.

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