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Active power decoupling with reduced converter stress for single-phase power conversion and interfacing

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Abstract. Single-phase DC–AC power electronic converters suffer from pulsating power at double the line frequency. The commonest practice to handle the issue is to provide a huge electrolytic capacitor for smoothening out the ripple. However, the electrolytic capacitors having short end of lifetime limit the overall lifetime of the converter. Another way of handling the ripple power is by active power decoupling (APD) using the storage devices and a set of semiconductor switches. Here, a novel topology has been proposed in implementing APD. The topology claims the benefit of (1) reduced stress on converter switches and (2) using smaller capacitance value, thus alleviating the use of electrolytic capacitor and in turn improving the lifetime of the converter. The circuit consists of a third leg, a storage capacitor and a storage inductor. The analysis and the simulation results are shown to prove the effectiveness of the topology.

Keywords. Single phase; double-frequency ripple; active power decoupling; reduced stress; reliability.

1. Introduction

The single-phase power electronic converters interfacing a DC storage system or a DC source have the inherent problem of double-frequency power ripple. The effect of the same is experienced at the DC bus in terms of double-frequency current ripple, leading to double-frequency DC bus voltage ripple in a standard single-phase DC–AC Voltage Source Inverter (VSI). This results in under-utilisation of renewable energy sources (e.g., PV), potential life-shortening for the batteries where the ripple current flows into the battery, thus heating up the battery. Further, this also leads to grid current distortion. The most common practice to counteract this scenario is to use a huge DC bus capacitor to supply the ripple current component. This passive strategy calls for electrolytic capacitors (because of their high capacitance value). However, the electrolytic capacitors have short end of lifetime, which reduces the overall system reliability [1].

In recent times, addressing the ripple power issue in active rather than in passive manner has been reported, the idea being compensation of the ripple power using a set of switches to control the state of the storage element. The main motivations for this approach have been

- increasing the life of converter by eliminating the weakest point, i.e., the electrolytic capacitor from the system and
- using the storage devices more effectively.

The approaches vary in the placement of the ripple power buffer circuitry. The main trends are

- active ripple power compensation in DC side [2–4],
- providing a dedicated energy port to handle ripple power in high-frequency (HF) isolated configurations [5–8] and
- compensating the ripple power in AC side of the converter [9–11].

Among these approaches, DC side buffer has been popular because of its reduced switch count, even though controller bandwidth needs to be very high to track the high-frequency harmonic-rich current. This calls for high switching frequency of the converter, keeping their application limited to low power level.

In the second approach, the buffer circuitry interfaces the line frequency AC side, via a HF transformer either with or without a tertiary winding. Although control variable is of line frequency, this approach demands increase in the number of auxiliary switches in large proportion.

Interestingly, AC side compensation topologies have been reported with only a set of two auxiliary switches and a storage device. By compensating the ripple power in the AC stage, down the line stages process only the average power, hence increasing the overall efficiency of the converter. In this way, the storage devices are utilised most efficiently, leading to 10 times reduction in capacitance compared with passive approach [12].

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With advanced control, the auxiliary switches have been reported to add less than 50% kVA rating to the existing H-bridge [12]. This statement is true for three conditions of load, viz., rectifier (unity power factor (UPF)), inverter (UPF) and STATCOM (zero power factor (ZPF)) with current lagging voltage. The topology can handle the remaining loading condition (ZPF with current leading voltage) but at the cost of increased current stress on the switches.

In this paper, a novel topology is proposed that can handle all loading conditions without further increase in converter kVA rating. In addition, 30% current reduction is achieved in H-bridge legs for UPF operation, leading to reduction in current stress of the switches, improving the overall reliability of the system. These assertions are theoretically shown using the power balance equation and phasor diagrams. Simulation results are presented in further support of the analysis.

The content of the paper has been arranged in the following manner. In section 2, the proposed topology is presented along with its operating principle; section 3 is presented to compare the proposed topology with the existing one; in section 4 the simulation results are presented and finally the conclusion has been drawn in section 5.

2. Proposed topology

In standard grid connected DC/AC H-bridge configuration, V_g, I_g and L_g denotes grid voltage, grid current and filter inductor, respectively. C_{DC}, the DC bus capacitor, is used to filter out the harmonic component of the DC bus current to make I_{DC} fairly constant. O, the mid-point of the DC bus, serves the purpose of a virtual ground for the analysis.

The proposed topology is shown in figure 1. The circuit consists of an AC capacitor (C) with a filter inductor (L_C), a storage inductor (L) and a pair of switches (shown in shaded area) in addition to standard H-bridge configuration. The operation of the circuit is explained later.

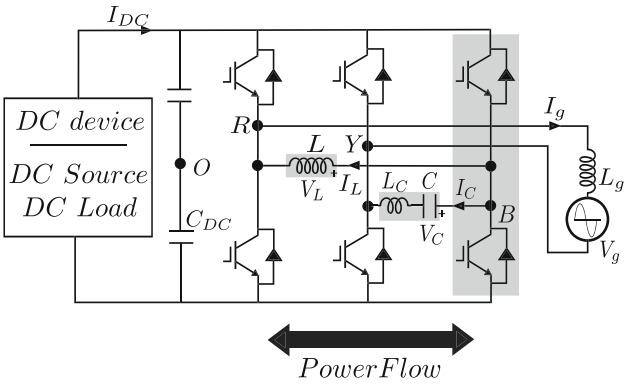


Figure 1. Circuit diagram of the proposed converter.

The R and Y legs of the converter are operated in current control mode in a way same as that of standard single-phase grid connected converter. However, the voltage of the third leg, B, is controlled in order to control the voltage across AC capacitor (C) and inductor (L). These two states together supply the double-frequency power requirement of the grid. Thus, the power drawn from the DC side appears to be a constant one. Hence, the DC bus capacitor does not need to supply the pulsating power. This in effect reduces the DC bus capacitance requirement.

The pole voltage of legs R and Y with respect to DC bus mid-point O are V_{RO} and V_{YO}, respectively. The fundamental components of these two voltages are controlled to be equal and opposite. The difference between the two constitutes the required inverter voltage in order to inject the reference current to grid voltage V_g. The grid current I_g lags V_g by power factor (PF) angle α. The phase (δ) and magnitude of fundamental component of third leg (B) pole voltage V_{BO} are controlled, which in effect controls capacitor voltage V_C and inductor voltage V_L in order to achieve active power decoupling (APD). The relevant voltages and current are shown in phasor diagram figure 2. In the following paragraphs, an analytical expression for magnitude and phase of V_{BO} is derived based on the principle of APD.

The instantaneous power drawn from the DC source is constant with APD (neglecting switching harmonics).

Applying power balance:

$$p_C + p_L + p_g = V_{DC} I_{DC} = constant$$

where p_C, p_L and p_g are, respectively, the instantaneous power of capacitor, inductor and the grid branches (refer the Appendix for p_C, p_L and p_g expression derivation).

In the following discussion, the instantaneous power expressions for grid, inductor and capacitor are derived for an arbitrary PF angle α. Power balance equation is used to obtain the control condition of the APD scheme.

In order to simplify the analysis, the effect of filter inductor L_g and L_C is neglected. The assumption is justified as, their values are generally less than 0.05 per unit (p.u.).

As shown in the phasor diagram (figure 2) V_C and V_L lead V_g by angle θ and ϕ, respectively:

$$v_g = V_{gm} \sin \omega t, \tag{1}$$

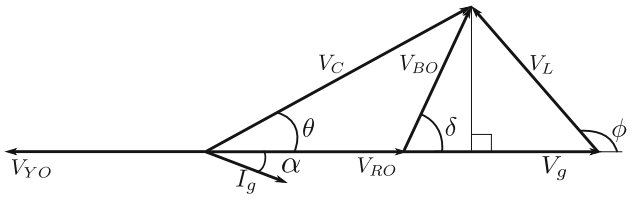


Figure 2. Phasor diagram for an arbitrary power factor (neglecting the drop across L_C and L_g).

$$i_g = I_{gm}\sin(\omega t - \alpha), \tag{2}$$

$$v_C = V_{Cm}\sin(\omega t + \theta), \tag{3}$$

$$i_C = I_{Cm}\sin\left(\omega t + \theta + \frac{\pi}{2}\right), \tag{4}$$

$$v_L = V_{Lm}\sin(\omega t + \phi), \tag{5}$$

$$i_L = I_{Lm}\sin\left(\omega t + \phi - \frac{\pi}{2}\right). \tag{6}$$

Instantaneous power pumped into the AC sink is

$$p_g = v_g i_g.$$

Substituting the expressions of v_g and i_g from Eqs. (1) and (2), this equation reduces to

$$p_g = V_g I_g[\cos\alpha - \cos(2\omega t - \alpha)]. \tag{7}$$

Power stored in the capacitor C is

$$p_C = v_C i_C. \tag{8}$$

Using Eqs. (3) and (4) in Eq. (8) gives

$$p_C = \frac{V_C^2}{|X_C|}\left[\sin 2\omega t\left(1 - 2\sin^2\theta\right) + 2\cos 2\omega t(\sin\theta\cos\theta)\right]. \tag{9}$$

Similarly, power stored in the inductor is

$$p_L = v_L i_L. \tag{10}$$

Substituting (5) and (6) in (10) gives

$$p_L = -\frac{V_L^2}{|X_L|}\left[\sin 2\omega t\left(1 - 2\sin^2\phi\right) + 2\cos 2\omega t(\sin\phi\cos\phi)\right]. \tag{11}$$

From figure 2

$$V_{BO}\sin\delta = V_C\sin\theta = -V_L\sin\phi. \tag{12}$$

Therefore, using Eqs. (9), (11) and (12), the expression for total power stored together in inductor and capacitor is

$$\begin{aligned} p_C + p_L &= \frac{1}{|X_C|}[\sin 2\omega t(V_C^2 - 2V_{BO}^2\sin^2\delta) \\ &\quad + 2\cos 2\omega t(V_{BO}\sin\delta V_C\cos\theta)] \\ &\quad - \frac{1}{|X_L|}[\sin 2\omega t(V_L^2 - 2V_{BO}^2\sin^2\delta) \\ &\quad - 2\cos 2\omega t(V_{BO}\sin\delta V_L\cos\phi)]. \end{aligned}$$

If $|X_C| = |X_L|$, RHS of this equation reduces to

$$\begin{aligned} &= \frac{1}{|X_L|}[\sin 2\omega t(V_c^2 - V_L^2) \\ &\quad + 2\cos 2\omega t V_{BO}\sin\delta(V_c\cos\theta - V_L\cos\phi)] \\ &= \frac{1}{|X_L|}[\sin 2\omega t(V_c^2\cos^2\theta - V_L^2\cos^2\phi) \\ &\quad + 2\cos 2\omega t V_{BO}\sin\delta(V_C\cos\theta - V_L\cos\phi)] \\ &= \frac{1}{|X_L|}(V_C\cos\theta - V_L\cos\phi)[\sin 2\omega t \\ &\quad \times (V_C\cos\theta + V_L\cos\phi) + 2\cos 2\omega t V_{BO}\sin\delta]. \end{aligned} \tag{13}$$

From figure 2, $(V_C\cos\theta - V_L\cos\phi) = 2V_{RO}$;

$$V_L\cos\phi = -(V_{RO} - V_{BO}\cos\delta);$$
$$V_C\cos\theta = V_{BO}\cos\delta + V_{RO};$$

Therefore, $(V_C\cos\theta + V_L\cos\phi) = 2V_{BO}\cos\delta$.

Substituting these relations into the power equation (13) gives

$$\begin{aligned} p_C + p_L &= \frac{2V_{RO}}{|X_L|}[\sin 2\omega t(2V_{BO}\cos\delta) + \cos 2\omega t(2V_{BO}\sin\delta)] \\ &= \frac{4V_{RO}V_{BO}}{|X_L|}\sin(2\omega t + \delta) \\ &= \frac{4V_{RO}V_{BO}}{|X_L|}\cos\left(2\omega t + \delta - \frac{\pi}{2}\right) \\ &= \frac{V_g(2V_{BO})}{|X_L|}\cos\left(2\omega t - \left(\frac{\pi}{2} - \delta\right)\right). \end{aligned} \tag{14}$$

Thus, in order to arrive at APD control condition, comparing (7) and (14) one can conclude that

$$1.\ |V_{BO}| = 0.5I_g(\text{in p.u. sense}) \text{ when } |X_L| = 1 \text{ p.u.} \tag{15}$$

$$2.\ \delta = \frac{\pi}{2} - \alpha. \tag{16}$$

These relationships guide one to select the reference voltage vectors at different loadings as well as PF.

Using this solution of V_{BO}, leg currents are obtained from the phasors for different loading conditions. The phasors are drawn with the current being pumped to the AC sink, which is the positive active power flow direction from DC to AC side.

The loading conditions considered for full load are

- inverter UPF ($\alpha = 0$),
- inverter ZPF for inductive load ($\alpha = \pi/2$),
- rectifier UPF ($\alpha = \pi$),
- inverter ZPF for capacitive load ($\alpha = 3\pi/2$).

2.1 *Individual case analysis*

For the rest of the analysis $|X_L|$ is considered as 1 p.u., which is a design criteria.

2.1a *Inverter UPF operation at full load*: From Eqs. (15) and (16)

$$|V_{BO}| = 0.5 \text{ p.u.},$$
$$\delta = \pi/2 - \alpha = \pi/2.$$

Therefore, from figure 3a

$$V_C = (\sqrt{2} \times 0.5)\angle\frac{\pi}{4} \text{ p.u.}$$
$$= 0.707\angle\frac{\pi}{4} \text{ p.u.}$$
$$V_L = 0.707\angle\frac{3\pi}{4} \text{ p.u.}$$

Thus, with the assumption $|X_L| = |X_C| =$ 1 p.u.

$$I_C = 0.707\angle\frac{3\pi}{4} \text{ p.u.},$$
$$I_L = 0.707\angle\frac{\pi}{4} \text{ p.u.}$$

This gives the leg currents

$$I_R = I_g - I_L = 0.707\angle -\frac{\pi}{4} \text{ p.u.},$$
$$I_Y = -(I_g + I_C) = 0.707\angle -\frac{3\pi}{4} \text{ p.u.},$$
$$I_B = I_C + I_L = 1\angle\frac{\pi}{2} \text{ p.u.}$$

2.1b *Inverter ZPF for inductive load at full load*: From Eqs. (15) and (16)

$$|V_{BO}| = 0.5 \text{ p.u.},$$
$$\delta = \pi/2 - \alpha = 0.$$

Therefore, from figure 3b

$$V_C = 1\angle 0 \text{ p.u.},$$
$$V_L = 0 \text{ p.u.}$$

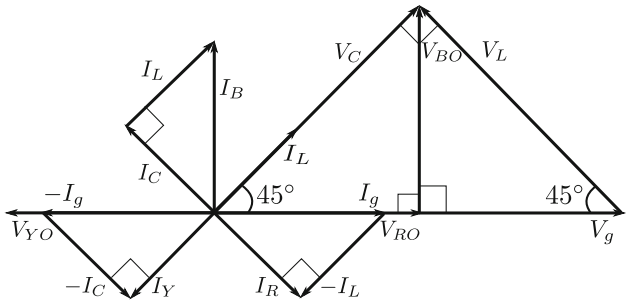
Thus, with the assumption $|X_L| = |X_C| =$ 1 p.u.

$$I_C = 1\angle\frac{\pi}{2} \text{ p.u.},$$
$$I_L = 0 \text{ p.u.},$$

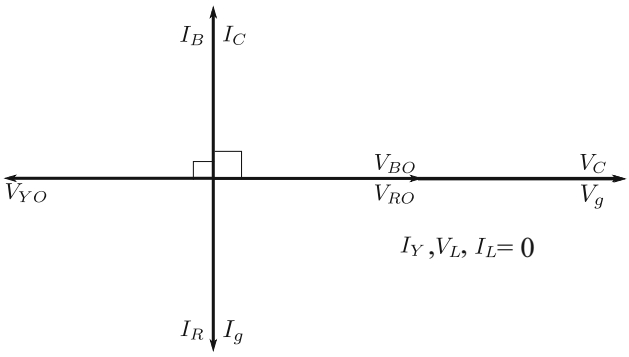
resulting in the leg currents

$$I_R = I_g - I_L = 1\angle -\frac{\pi}{2} \text{ p.u.},$$
$$I_Y = -(I_g + I_C) = 0 \text{ p.u.},$$
$$I_B = I_C + I_L = 1\angle\frac{\pi}{2} \text{ p.u.}$$

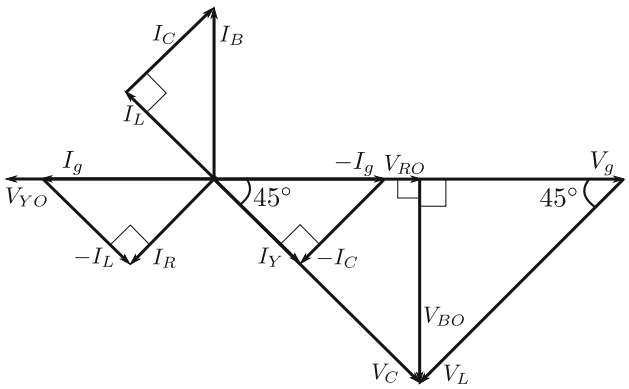
2.1c *Rectifier UPF operation at full load*: From Eqs. (15) and (16)



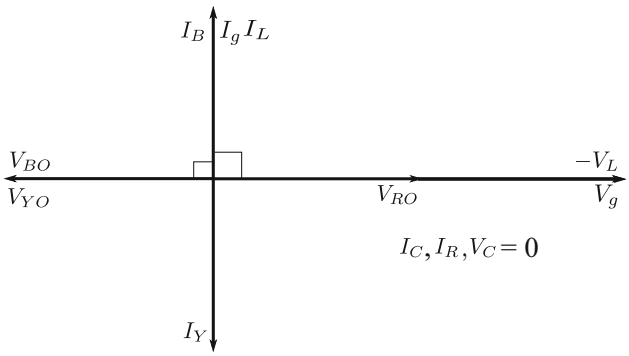
(a) Inverter operation at UPF



(b) Inverter operation at ZPF for Inductive load



(c) Rectifier operation at UPF



(d) Inverter operation at ZPF for Capacitive load

Figure 3. Phasor diagram at full load condition.

$$|V_{BO}| = 0.5 \text{ p.u.},$$
$$\delta = \pi/2 - \alpha = -\pi/2.$$

Therefore, with reference to figure 3c, following the same procedure as in *Case* 1, leg currents are

$$I_R = I_g - I_L = 0.707\angle -\frac{3\pi}{4} \text{ p.u.},$$
$$I_Y = -(I_g + I_C) = 0.707\angle -\frac{\pi}{4} \text{ p.u.},$$
$$I_B = I_C + I_L = 1\angle\frac{\pi}{2} \text{ p.u.}$$

2.1d *Inverter ZPF for capacitive load at full load*: From Eqs. (15) and (16)

$$|V_{BO}| = 0.5 \text{ p.u.},$$
$$\delta = \pi/2 - \alpha = \pi.$$

Therefore, from figure 3d

$$V_C = 0 \text{ p.u.},$$
$$V_L = 1\angle\pi \text{ p.u.}$$

Following the same process and with the same assumption as in *Case* 2, resulting leg currents are

$$I_R = I_g - I_L = 0 \text{ p.u.},$$
$$I_Y = -(I_g + I_C) = 1\angle -\frac{\pi}{2} \text{ p.u.},$$
$$I_B = I_C + I_L = 1\angle\frac{\pi}{2} \text{ p.u.}$$

These results are condensed in table 1 for the ease of comparison with the existing topology [12].

3. Comparison with existing topology

With reference to the phasor diagram figure 4 and the phasor diagrams presented in [12], the results of the existing topology are included in table 1.

From table 1, it can be seen that the proposed topology has identical 30% current reduction in both legs under UPF,

Table 1. Converter installed capacity comparison.

PF condition		With only C storage [12]				With L and C storage			
		Leg currents (in p.u.)				Leg currents (in p.u.)			
ϕ	α	$\lvert I_R\rvert$	$\lvert I_Y\rvert$	$\lvert I_B\rvert$	K_{SF}^a	$\lvert I_R\rvert$	$\lvert I_Y\rvert$	$\lvert I_B\rvert$	K_{SF}^a
0	π	1	0.77	1	**0.92**	0.71	0.71	1	**0.8**
$\pi/2$	$\pi/2$	1	0	1	0.67	1	0	1	0.67
π	0	1	0.77	1	**0.92**	0.71	0.71	1	**0.8**
$-\pi/2$	$-\pi/2$	1	1.44	1	**1.13**	0	1	1	**0.67**

[a] Stress Factor = 3 legged converter rating (APD compensated)/3 legged converter rating with 3rd leg rated identical as H bridge (uncompensated).

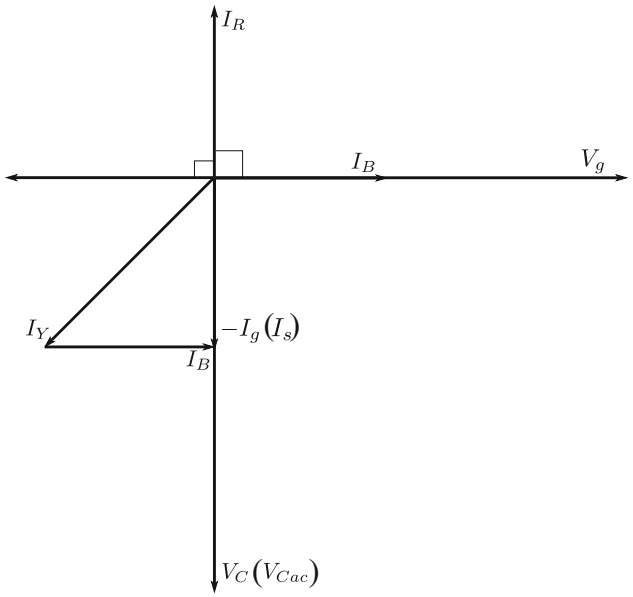


Figure 4. Phasor diagram of STATCOM operation, $I_s(-I_g)$ lagging V_g by $\pi/2$ for topology [12].

which means lesser loss and temperature rise of the semiconductor switches. This reduced stress results in higher reliability of the switches. The improvement is even more for $\phi = -\pi/2$, where leg Y is 44% overstressed for the existing topology in [12].

The parameter K_{SF}, stress factor, has been defined as the ratio of three-legged converter rating (APD compensated) to three-legged converter rating (the third leg is identical to uncompensated H bridge). From table 1, it can be seen that, K_{SF} reduces by 15% under UPF and 70% for capacitive load when compared with [12], which indicates reduced stress on the converter switches.

It should be noted that in the case of inductor being the only storage element instead of capacitor as in [11], the results will remain the same under UPF operation, whereas 70% reduction will be observed for inductive load instead of capacitive load.

4. Simulation results

For verification of the proposed topology and effectiveness of the decoupling method, a system rated for 230 V, 5 A has been modelled and simulated. The system parameters are listed in table 2.

The simulation results for inverter operating at UPF is presented in figures 5–7. From figure 5 it can be observed that the DC bus current ripple reduces to 0.2 A with APD compensation compared with 5.8 A under uncompensated scenario, thus validating the effectiveness of the scheme. Figure 6 shows that under UPF operation, both capacitor and inductor share the

Table 2. System parameters.

AC voltage, V_g	230 V (50 Hz)
AC current, I_g	5 A (50 Hz)
DC bus voltage, V_{DC}	400 V
Switching frequency, f_{sw}	20 kHz
Filter capacitor, C_{DC}	100 µF
Filter inductor, L_g	7.3 mH
Storage capacitor, C	68 µF
Storage inductor, L	146 mH
Filter inductor, L_C	2.2 mH

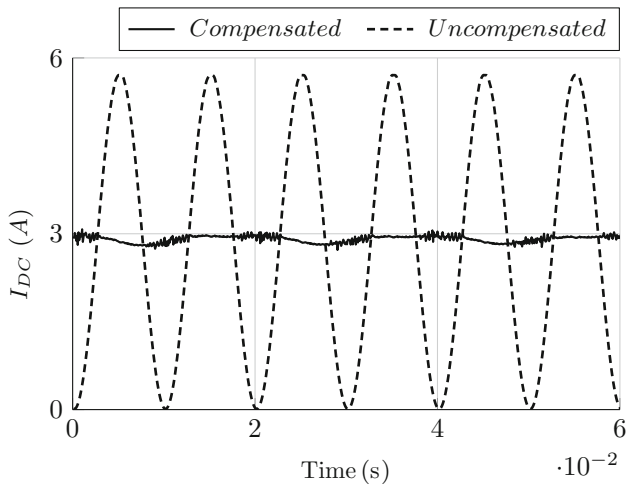


Figure 5. DC bus current with and without APD compensation at steady state.

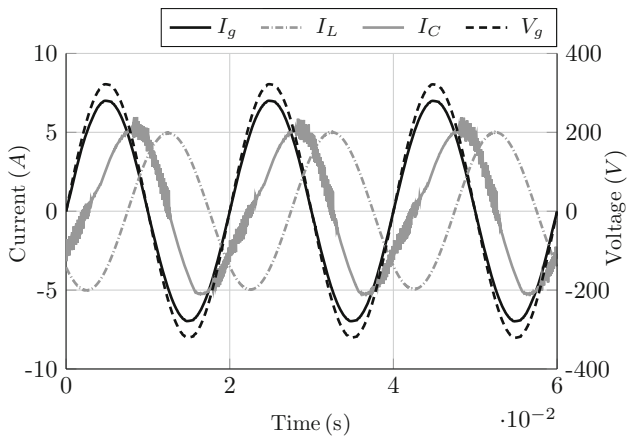


Figure 6. Branch currents and grid voltage at steady state.

energy equally and the currents through them are 70% of the grid current. In figure 7, leg currents of the converter are shown, from which the current reductions in two legs to 70% of the rated current (7 A peak) are clearly visible.

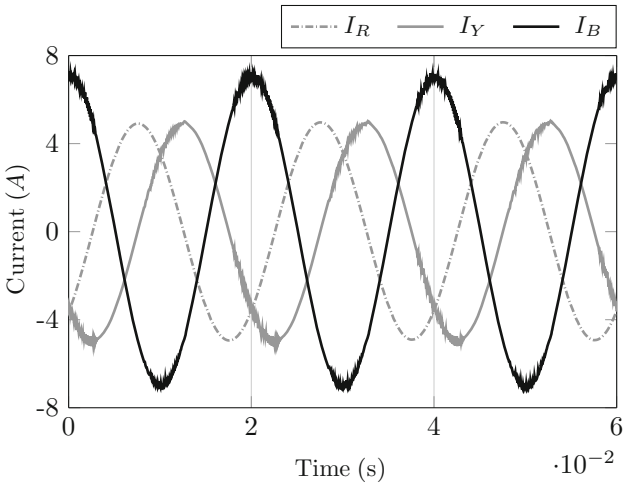


Figure 7. Leg currents with APD compensation at steady state.

5. Conclusion

In this paper, a novel topology is proposed to handle the single-phase power ripple. Analysis of the topology is performed using power balance equation and the phasor diagrams; 30% reduction in current rating of the H-bridge inverter is achieved for UPF. Also, the topology can handle all loading conditions with the maximum of 70% reduced stress compared with the existing topologies. Simulation results are presented for the validation of the same.

Appendix: Steady-state instantaneous power equations derivation

Grid power derivation

Instantaneous power pumped into AC sink

$$p_g = v_g i_g$$

Substituting expression of v_g and i_g from Eqs. (1) and (2), this equation reduces to

$$\begin{aligned} &= \frac{V_{gm} I_{gm}}{2} [\cos\alpha - \cos(2\omega t - \alpha)] \\ &= V_g I_g [\cos\alpha - \cos(2\omega t - \alpha)]. \end{aligned} \tag{17}$$

Capacitor power derivation

Power stored in capacitor C is

$$p_C = v_C i_C. \tag{18}$$

On simplifying Eq. (18), using Eqs. (3) and (4)

$$\begin{aligned} p_C &= V_{Cm}\sin(\omega t+\theta)I_{Cm}\sin\left(\omega t+\theta+\frac{\pi}{2}\right)\\ &= -V_C I_C\cos\left(2\omega t+2\theta+\frac{\pi}{2}\right)\\ &= V_C I_C\sin(2\omega t+2\theta)\\ &= \frac{V_C^2}{|X_C|}(\sin 2\omega t\cos 2\theta+\cos 2\omega t\sin 2\theta)\\ &= \frac{1}{|X_C|}[\sin 2\omega t(V_C^2-2V_C^2\sin^2\theta)\\ &\quad +2\cos 2\omega t(V_C\sin\theta V_C\cos\theta)]. \end{aligned} \tag{19}$$

Inductor power derivation

Similarly, for inductor L, power stored is

$$p_L = v_L i_L\,. \tag{20}$$

Solving Eq. (20) using Eqs. (5) and (6) results in

$$\begin{aligned} p_L &= V_{Lm}\sin(\omega t+\phi)I_{Lm}\sin\left(\omega t+\phi-\frac{\pi}{2}\right)\\ &= V_L I_L\left[-\cos\left(2\omega t+2\phi-\frac{\pi}{2}\right)\right]\\ &= -\frac{V_L^2}{|X_L|}\sin(2\omega t+2\phi)\\ &= -\frac{V_L^2}{|X_L|}(\sin 2\omega t\cos 2\phi+\cos 2\omega t\sin 2\phi)\\ &= -\frac{1}{|X_L|}[\sin 2\omega t(V_L^2-2V_L^2\sin^2\phi)\\ &\quad +2\cos 2\omega t(V_L\sin\phi V_L\cos\phi)]. \end{aligned} \tag{21}$$

References

[1] Harb S and Balog R 2013 Reliability of candidate photovoltaic module-integrated-inverter (pv-mii) topologies 2014: a usage model approach. *IEEE Trans. Power Electron.* 28(6): 3019–3027

[2] Kjaer S and Blaabjerg F 2003 Design optimization of a single phase inverter for photovoltaic applications. In: *Proceeding of the Power Electronics Specialist Conference. PESC '03, 34th Annual IEEE* , vol. 3, June 2003, pp. 1183–1190

[3] Shimizu T, Wada K and Nakamura N 2006 Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the dc input for an ac photovoltaic module system. *IEEE Trans. Power Electron.* 21(5): 1264–1272

[4] Kyritsis A, Papanikolaou N and Tatakis E 2007 A novel parallel active filter for current pulsation smoothing on single stage grid-connected ac-pv modules. In: *Proceedings of the Power Electronics and Applications, IEEE 2007 European Conference on*. pp 1–10

[5] Krein P and Balog R 2009 Cost-effective hundred-year life for single-phase inverters and rectifiers in solar and led lighting applications based on minimum capacitance requirements and a ripple power port. In: *proceeding of the Twenty-Fourth Annual IEEE. Applied Power Electronics Conference and Exposition, 2009, APEC 2009*, pp. 620–625

[6] Chen Y-M and Liao C-Y 2011 Three-port flyback-type single-phase micro-inverter with active power decoupling circuit. In: *Proceedings of the Energy Conversion Congress and Exposition (ECCE)*. IEEE, September 2011, pp. 501–506

[7] Hu H, Harb S, Fang X, Zhang D, Zhang Q, Shen Z and Batarseh I 2012 A three-port flyback for pv microinverter applications with power pulsation decoupling capability. *IEEE Trans. Power Electron.* 27(9): 3953–3964

[8] Harb S, Mirjafari M and Balog R 2013 Ripple-port module-integrated inverter for grid-connected pv applications. *IEEE Trans. Ind. Appl.* 49(6): 2692–2698

[9] Li H, Zhang K, Zhao H, Fan S and Xiong J 2013 Active power decoupling for high-power single-phase pwm rectifiers. *IEEE Trans. Power Electron.* 28(3): 1308–1319

[10] Bush C and Wang B 2009 A single-phase current source solar inverter with reduced-size dc link. In: *Proceedings of the IEEE Energy Conversion Congress and Exposition, ECCE 2009*, pp. 54–59

[11] Shimizu T, Jin Y and Kimura G 1999 DC ripple current reduction on a single-phase pwm voltage source rectifier. In: *IEEE Conf. Rec.* 2: 810–817

[12] Chen R, Liu Y and Peng F Z 2015 DC capacitor-less inverter for single-phase power conversion with minimum voltage and current stress. *IEEE Trans. Power Electron.* 30(10): 5499–5507