Design and comparative study of discrete and module-based IGBT power converters

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Abstract. This paper discusses concepts of a 20 kVA power converter design and key differences between discrete IGBT and module-based design approaches. Module-based power converters have been typically employed in academic and research institutes for power levels of 10 kVA and more. However, with advancement in IGBT technologies and the growing need to minimize system size and weight, designs based on discrete devices are now an attractive alternative for such power levels. A simple procedure is presented for power converter design that includes power loss evaluation, heat-sink thermal characterization, thermal model of overall system and sizing of DC link capacitor. Using the same, a state-of-the-art discrete device and module-based power converters are designed. A comparison is subsequently made, where it is shown that discrete approach yields a compact and economic design up to a power level of 20 kVA. A key objective of this work is to lay emphasis on laboratory design of power converters. This enables a graduate level student to build a converter from start and in the process gain insights into the underlying engineering design aspects.

Keywords. Discrete IGBT; inverter design; forced-air cooling; dc-link capacitor; multi-layer PCB; device junction temperature.

1. Introduction

Power electronic devices have evolved considerably over the past decade. Their fast switching speeds and low on-state saturation voltages result in lower power loss and reduced component size. A variety of semiconductor technologies are available today that differ in switching speeds and associated energy losses, saturation voltage, etc. Field-stop and Trench-gate IGBTs are designed for reduced saturation voltages [1, 2], whereas Warp IGBTs are designed for reduced switching energy losses [3]. Hybrid varieties such as high-speed Trench-stop IGBTs are also available now with optimized conduction and switching loss characteristics [4]. Power semiconductor packages have evolved as well from bulky modules to extremely compact surface mount designs.

For power levels on the order of 10 kVA, module-based two-level power converter designs have been prevalent in the form of off-the-shelf converter stacks, which are typically employed in various academic institutions. However, today, with existing technology in semiconductor and packaging, designs based on PCB-mounted discrete devices have become feasible for 10 kVA power level and more. A PCB-based design offers a variety of benefits such as

reduced parasitic inductances in power and gate-drive circuitry, compactness, reduced system cost and weight. Because parasitics are lowered in PCB, it is possible to increase switching frequency of operation and enhance power density.

In this work, a simple and practical design procedure with adequate design margins is introduced first in section 2, which targets graduate level engineering students, to enable them to build a power converter in the laboratory from the outset. The exercise of building a power converter from start allows the student to experience various underlying engineering challenges and develop a better understanding of the power electronic system. With this procedure, discrete and module-based designs are analysed and compared subsequently in section 3 in terms of cost, weight and power loss. This is followed by experimental verification of the design in terms of switching and thermal performance in section 4. Conclusions are subsequently drawn in section 5.

2. Discrete design procedure

Design of a power converter for a given power rating begins with selection of appropriate semiconductor devices of sufficient voltage and current ratings. A typical two-level three-phase four-leg converter

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Figure 1. Power circuit configuration of two-level three-phase four leg DC-AC converter.

configuration is shown in figure 1. A variety of semiconductor technologies are available today that differ in switching speeds, associated energy losses and saturation voltage [1–4]. One must choose a particular type that best suits the given application. This is followed by evaluating the amount of power loss incurred in the semiconductors during operation. Subsequently, a suitable heat-sink must be chosen that is capable of adequately dissipating the heat generated by the device losses, so as to maintain the heat-sink and device junction temperature around a desired value.

Heat extraction is done either through natural cooling or forced cooling using air or water. Forced-air convection cooling is preferred at higher power levels as it yields a more compact design. Although there are a variety of heat-sink profiles available in literature, the scope of this paper is restricted to design of one particular type shown in figure 2. A suitable thermal interface material is chosen, which is used between the device case and heat-sink surface, which has a decisive effect on the device junction temperature. Ultimately, the bottleneck in any power electronic design is the device junction temperature reached at steady state, which must be kept below the maximum device rating of 150 or 175°C with adequate margin, as explained in section 2.1. The target specifications of the converter shown in figure 1 are given in table 1 and the design procedures are explained below.

Figure 2. Geometry of forced-air cooled heat sink.

Table 1. Three-phase dc–ac power converter ratings.

Item	Value
Power	20 kVA
dc bus voltage V_{dc}	800 V
Output voltage (l–l)	400 V
Output current (RMS)	29 A
Nominal power factor	UPF
Nominal modulation index m_a	0.9
Switching frequency f_{sw}	10 kHz

2.1 Device selection

Device selection is largely based on three primal ratings of the device:

- **Voltage rating:** Typically, the device is rated such that the maximum peak collector–emitter voltage applied (inclusive of ringing excursion during turn-off transient) is about 20% below the device voltage rating. This ensures that adequate margin is available even during switching transients.
- **Current rating:** The ultimate current that a device can handle is constrained by bond wire current capacity and this is indicated in the safe operating area (SOA) curve. Keeping the device current level 20% below this value under all operating conditions is recommended.
- **Junction temperature:** Ensuring that the device junction temperature reached under nominal operating conditions is about 25°C below the maximum rating of 150 or 175°C is recommended. This constraint has implications on heat-sink geometry and cooling mechanism employed.

The chosen device that meets the converter specifications is IKW40N120H3 [5], which is a state-of-the-art IGBT.

2.2 Loss calculation

Once a device is chosen, total losses incurred during operation, which include that due to conduction and switching, must be evaluated. The conduction losses in IGBT are evaluated using an approximate model of series connected voltage source V_{ce0} and collector–emitter on-state resistance r_{ce} evaluated around the nominal operating point. A similar model is employed for anti-parallel diode as well [6]. The total conduction loss in a IGBT and diode is given by

$$P_{c,T} = V_{ce0}I_{T,avg} + r_{ce}I_{T,rms}^2 \quad (1)$$

$$P_{c,D} = V_{D0}I_{D,avg} + r_D I_{D,rms}^2 \quad (2)$$

where, for a three-phase power converter during operation that carries a peak current I_p , at a modulation index m_a and power factor $\cos \phi$, the IGBT and diode currents are given by [6]

$$I_{T,avg} = I_p \left(\frac{1}{2\pi} + \frac{m_a \cos \phi}{8} \right) \quad (3)$$

$$I_{D,avg} = I_p \left(\frac{1}{2\pi} - \frac{m_a \cos \phi}{8} \right) \quad (4)$$

$$I_{T,rms} = I_p \sqrt{\left(\frac{1}{8} + \frac{m_a \cos \phi}{3\pi} \right)} \quad (5)$$

$$I_{D,rms} = I_p \sqrt{\left(\frac{1}{8} - \frac{m_a \cos \phi}{3\pi} \right)}. \quad (6)$$

The total switching loss in IGBT and diode when the converter operates at frequency f_{sw} is given by

$$P_{sw,T} = \frac{1}{\pi} (E_{on,T} + E_{off,T}) \frac{V_{DC}}{V_{DC,test}} \frac{I_p}{I_{test}} f_{sw} \quad (7)$$

$$P_{sw,D} \approx E_{on,D} f_{sw} = \frac{1}{4} Q_{rr} V_{DC} f_{sw} \quad (8)$$

where $E_{on,T}$ and $E_{off,T}$ are turn-on and turn-off energy loss stated in the device datasheet at test conditions of certain $V_{DC,test}$, I_{test} , $R_{G,on}$, $R_{G,off}$, and Q_{rr} is the diode reverse recovery charge at circuit operating conditions. Using these power loss equations, the losses are evaluated at the desired operating conditions of dc-link voltage and current. Correction factor for energy loss, when different values of $R_{G,on}$ and $R_{G,off}$ are used, may be obtained from corresponding energy loss curves in datasheet [6, 7]. Table 2 shows the actual loss figures for the chosen device at rated operating conditions given in table 1.

For a three-phase three-leg converter operation, the total loss P_{loss} incurred in semiconductor would be 362 W. Hence, it is required to design a heat sink that is capable of dissipating 362 W of power loss. It may be noted that at rated operating conditions, efficiency of the power converter is over 98%. This is due to the fact that the chosen device is a state-of-the-art switching-loss-optimized IGBT.

2.3 Heat sink selection

At higher power levels, heat sink with forced-air-convection cooling using a fan is the most preferred arrangement

owing to its simplicity and effectiveness. A host of heat-sink geometries is available in literature, and the biggest challenge with them is to determine the thermal resistance theoretically for a given fan. It is possible to determine thermal resistance experimentally, but a method to estimate dissipation capacity of a given profile serves as a good starting point and would greatly aid first-pass design. The profile chosen in this paper, as shown in figure 2, is one that requires relatively simpler analysis for estimating power dissipation capacity.

It uses horizontal fins arranged symmetrically with the fan placed at one end. A shroud is employed to prevent the air from escaping through the sides, thus channelizing the flow through the fin gaps. With the shroud in place, the fin gap may be treated as an uninsulated rectangular duct. This means that the heat sink as a whole would consist of as many ducts as the number of fin gaps. The design procedure is explained here with the aid of an example.

1. Choose a fan of a certain dimension and volumetric-flow rate, which typically is rated in cubic foot per minute (CFM). For example, consider a 24V BLDC fan from Sanyo Denki [8], properties of which are listed in table 3.
2. Assume a heat-sink profile such that fin region spans the cross-sectional area of the fan. For example, for the profile shown in figure 2, total fin area spans the width and height of the fan considered in table 3. Choose a certain fin thickness and fin gap, say 2 and 5 mm, respectively. The length of the heat sink is determined by the number of devices to be mounted and the chosen gap between them. The corresponding dimensional parameters of a 200-mm-long heat sink are listed in table 4. It is now required to estimate the heat dissipation capacity of this heat-sink profile.
3. With the heat sink in place, the operating CFM of the fan would decrease depending on the static pressure offered by the heat-sink fin area. Assume that the CFM drops by 50%. Assume the inlet air temperature to be 25°C and exit air temperature to be 60°C. Hence, the bulk temperature would be the mean value, i.e., 42.5°C. Obtain the air properties at 40°C and 1 atm pressure from a standard table, as listed in table 5.

Table 2. IGBT and diode power loss at rated operating conditions.

Item	Value (W)
IGBT conduction loss	25.8
Diode conduction loss	4.1
IGBT switching loss	30.4
Total loss per device	60.3

Table 3. Properties of dc fan from Sanyo Denki.

Item	Value
Part no.	9G0824H101
Rated power	10.1 W
Rated voltage	24 V
Rated flow rate	80 cfm
Max. static pressure	171 Pa
Width	80 mm
Height	80 mm
Thickness	40 mm

Table 4. Heat-sink dimensions.

Item	Value
Fin thickness t_f	2 mm
Fin gap g_f	5 mm
Duct parameters	
Width w	34 mm
Thickness t	5 mm
Length L	200 mm
Perimeter p	78 mm
Cross-section area A_c	170 mm ²
Inner surface area A_s	15,600 mm ²
No. of ducts n	22

Table 5. Properties of air at 1 atm pressure and 40°C.

Item	Value
Density ρ	1.127 kg/m ³
Specific capacity C_p	1007 J/kg K
Thermal conductivity k	0.02662 W/m K
Kinematic viscosity ν	1.702×10^{-5} m ² /s
Prandtl no. Pr	0.7255

4. Next, the nature of air flow (laminar or turbulent) in the duct needs to be determined, with the help of the *Reynolds number* [9]

Flow rate in one duct $\dot{V}$ is given by

$$\dot{V} = \text{rated CFM} \times \left(\frac{0.5}{n}\right) = 1.82 \text{ cfm} \quad (9)$$

$$\Rightarrow \dot{V} = 0.85 \times 10^{-3} \text{ m}^3/\text{s}. \quad (10)$$

Equivalent hydraulic diameter of the duct is given by

$$D_h = \frac{4A_c}{p} = 8.71 \times 10^{-3} \text{ m}. \quad (11)$$

Average velocity of air in the duct is given by

$$v_{avg} = \frac{\dot{V}}{A_c} = 5.04 \text{ m/s}. \quad (12)$$

Reynolds number for the flow is given by

$$Re = \frac{v_{avg} D_h}{\nu} = 2584. \quad (13)$$

Flow is fully laminar when $Re < 2800$ and fully turbulent when $Re > 10,000$ [9]. It is recommended to keep the flow laminar for simplicity of calculations. Hence, if calculated $Re > 2800$, go to step 2 and modify duct dimensions appropriately.

5. Next, *Nusselt number* for the flow is calculated. Hydrodynamic entry length is calculated as

$$L_h = 10D_h = 8.71 \times 10^{-2} \text{ m}. \quad (14)$$

Nusselt number for the above laminar flow is given by

$$Nu = 7.54 + \frac{0.03(D_h/L)RePr}{1 + 0.016[(D_h/L)RePr]^{2/3}} \quad (15)$$

$$\Rightarrow Nu = 7.6. \quad (16)$$

6. From the Nusselt number, heat transfer coefficient h for the heat sink by forced air convection is evaluated:

$$h = k \frac{Nu}{D_h} \text{ W/m}^2 \text{ } ^\circ\text{C} \quad (17)$$

$$\Rightarrow h = 23 \text{ W/m}^2 \text{ } ^\circ\text{C}. \quad (18)$$

7. Finally, the amount of power drawn away by air through forced convection is calculated, which would give a fair idea about the capacity or effectiveness of the chosen heat sink. Mass-flow rate through the duct is

$$\dot{m} = \rho \dot{V} = 0.966 \times 10^{-3} \text{ kg/s}. \quad (19)$$

Assuming that inlet air temperature T_i is 25°C and duct surface temperature T_s is 80°C, exit air temperature T_e is determines as,

$$T_e = T_s - (T_s - T_i)e^{-hA_s/\dot{m}c_p} \quad (20)$$

$$\Rightarrow T_e = 42.1^\circ\text{C}. \quad (21)$$

Logarithmic mean temperature difference is given by

$$\Delta T_{ln} = \frac{T_i - T_e}{\ln \frac{T_s - T_e}{T_s - T_i}} = 45.9^\circ\text{C}. \quad (22)$$

Rate of heat loss from a single duct by forced convection is thus determined as

$$\dot{Q} = P_{duct} = hA_s \Delta T_{ln} = 23 \times 0.0156 \times 47.4 = 16.6 \text{ W}. \quad (23)$$

8. Total heat loss from whole heat sink by forced convection is given by

$$P_{tot} = nP_{duct} = 22 \times 16.6 = 366 \text{ W}. \quad (24)$$

9. If total device losses $P_{loss} > P_{tot}$, go to step 1 and modify fan CFM, or go to step 2 and change heat sink dimensions appropriately.

Therefore, the heat sink of the chosen geometry with 80 CFM fan is capable of extracting 366 W of power, with duct surface temperature at 80°C. An additional 20% margin can be kept and the system can be over-designed. This is an indicative value that serves as a starting point to estimate the capacity of heat sink. A rough theoretical estimate of force-cooled heat-sink thermal resistance can be obtained from P_{tot} and duct surface temperature, which yields a value of 0.15°C/W. For experimental measurement

Figure 3. Thermal model of forced-air cooled system showing (a) thermal equivalent circuit and (b) physical disposition.

of heat-sink thermal resistance, a suitable thermal model and experimentation is suggested.

2.4 Thermal model

For case-temperature rise estimation, a simple thermal model for the forced-convection cooled system is proposed. For simplicity, the fin region of the heat sink, where convection cooling is taking place, can be approximated as a single thermal resistance R_{conv} . Heat transfer through the stem of heat sink, taking place via conduction, can be approximated as another thermal resistance R_{stem} (figure 3). With the help of heat-sink dimensions, R_{stem} can be calculated analytically [9]. For measurement of R_{conv} , the following experiment is suggested:

- connect all devices in series and operate them as diodes;
- pass appropriate currents through the series arrangement for different levels of power dissipation;
- measure the mean mid-point temperature of fin region T_m for different values of power dissipation;
- calculate r_{conv} from total dissipated power P_{total} and temperature rise ΔT for each case and take the mean value.

From measurements, the mean convection thermal resistance $R_{conv} = 0.173^\circ\text{C/W}$ (table 6), which is close to the predicted value in section 2.3. Using the suggested thermal model, R_{conv} , along with thermal resistance of device R_{jc} and that of thermal interface material R_{Ti} , shall be used to estimate device case-temperature rise. This could serve as a useful starting point for the first-pass design.

2.5 dc-link capacitor selection

Dimensioning of dc-link capacitor depends on combination of factors such as allowable current stress that offers a certain working life as specified in the datasheet, allowable low frequency dc-link voltage ripple in case of single-phase applications and hold-up time required during front-end fault ride-through.

Table 6. Experimental data for heat sink with six devices carrying constant current.

P_d (W)	P_{total} (W)	$T_{c,avg}$ ($^\circ\text{C}$)	$T_{m,avg}$ ($^\circ\text{C}$)	T_{amb} ($^\circ\text{C}$)	ΔT ($^\circ\text{C}$)	r_{conv} ($^\circ\text{C/W}$)
20	120	67.4	47	26	21	0.18
25	150	78.3	51.5	26	25.5	0.17
30	180	86.7	56.3	26	30.3	0.17

In a three-phase PWM converter, only switching frequency ripple current flows through dc-link capacitor and hence it experiences only high-frequency current stress [10], the RMS value of which is given by

$$I_{C,rms} = I_p \sqrt{\frac{\sqrt{3}m_a}{4\pi} + \left(\frac{\sqrt{3}m_a}{\pi} - \frac{9m_a^2}{16}\right) \cos^2 \phi}. \quad (25)$$

In case of single-phase PWM converter, differential mode second harmonic current also flows through the dc-link capacitors in addition to switching frequency ripple, thus resulting in a second harmonic voltage ripple $\Delta v_{c,100\text{ Hz}}$ expressed as

$$\Delta v_{c,100\text{ Hz}} = \frac{V_{o,rms} I_{o,rms}}{2V_{DC} \pi f_1 C_{dc}} \quad (26)$$

where f_1 , $V_{o,rms}$ and $I_{o,rms}$ are fundamental frequency, output RMS voltage and RMS current, respectively. This value may be chosen to be 10% of nominal dc bus voltage.

All the above constraints must be considered appropriately for dc-link capacitor design.

3. Module versus discrete design

Designs of module-based and discrete component power converter differ in a few ways that are outlined below.

- *Dc bus structure:* External dc bus plates with bushes and appropriate geometry are employed in case of module-based design. With discrete IGBTs, dc bus would be in the form of internal layer planes of a multi-layer power PCB. Distance between dc-link capacitors and devices can be considerably reduced in a PCB and hence parasitic inductance can be reduced significantly.
- *Dc-link capacitor:* Module-based design requires screw-type dc bus capacitors that are attached to bus plates through bushes and screws appropriately. In discrete design, snap-in or plug-in capacitors are used that can get soldered to the power PCB, as shown in figure 4. For a given capacitance value and voltage rating, parameters such as equivalent series resistance ESR, equivalent series inductance ESL and current ratings would vary depending on the type of electrolytic capacitors used. Screw-type capacitors possess

Figure 4. Physical placement details of components on power PCB showing (1) DC bus capacitors, (2) high-frequency decoupling capacitors, (3) discrete IGBT devices, (4) bus bars, (5) gate-driver location, (6) current sensors, (7) output relays, (8) pre-charge circuit, (9) output connectors and (10) connector to digital controller.

higher ESL, lower ESR and higher current ratings as compared with snap-in capacitors. Also, screw-type capacitors are relatively expensive.

- *Gate-drive circuit:* In discrete design, gate drive circuitry may be placed closest to the device either by directly soldering them onto PCB or in the form of a daughter card [11] mounted on PCB near the device and thus reducing parasitics to minimal. In case of modules, owing to the mechanical layout, the parasitics are relatively higher due to wired interconnection, typically in the form of twisted pairs.
- *Power density:* PCB-based designs, especially when four or more layers are employed, offer much higher power density as compared with module-based design. At higher power levels, however, PCB trace widths must be sized sufficiently large so as to carry rated currents for a given temperature rise, which could reduce power density. This may be avoided and power density may be enhanced further by employing bus bars soldered on to PCB, as shown in figure 4.

Apart from device junction temperature limitation, parasitics also plays a key role in determining the maximum power level up to which a given design can be operated. This is due to the fact that at higher power levels, parasitics inductances in gate-drive circuitry and dc bus plates may cause excessive ringing during switching and the device voltage excursions may well be beyond admissible stress limits. It is desirable to keep parasitics to the minimum possible extent by having a clean physical layout [12], and in this viewpoint, PCB-based design stands better than module-based approach. Also, since housing of connectors is easier on a PCB, as illustrated by figure 4, interfacing

PCB-based power circuit with an external digital controller is rather simple.

As an example, a three-phase 20 kVA PCB-based two-level discrete power converter design using the aforementioned procedure is presented and compared to similar-rated module-based design in terms of system cost, for a three-leg topology, which is prevalent in commercial converters. State-of-the-art power devices and other components are employed in the two designs [5, 13–15]. At rated operating conditions, the ripple current catered by dc bus capacitor $I_{C,rms}$ calculated from Eq. (25) is 20.6 A and the dc bus capacitance value is chosen as 1000 μ F. The PCB, as shown in figure 4a, is designed such that the size of the dc-link capacitor bank can be increased by interfacing with external capacitors, in case of large hold-up time requirement.

The choices of system components with associated losses and cost details are compared, in table 7. The heat-sink design procedure described in section 2.3 would lead to similar-sized heat-sink structures for module and discrete design since their semiconductor losses are rather similar, as can be seen from table 7. Hence, the cost of heat sinks would be comparable in the two designs. Figure 4 shows physical component placement on a four-layer, 2.4-mm power PCB that uses 70- μ m copper, designed conforming to IPC-2221A design standard [16]. Two internal layers are used for DC-link in the power section, and for ground and power planes in the signal section. The PCB core is 1.4-mm thick, made of pre-preg 7628 with 300-V/mil breakdown strength. External layers are used for component interconnections and power traces [17].

The PCB includes dc-link capacitors with bleeder resistors, IGBT devices, diode-bridge-based pre-charge circuitry, heat-sink plus fan, gate-drive cards [11], on-board current sensors, output relays to power connectors, FRC connectors to external digital controller and power-supply connectors. To enhance the power density of the PCB, 1-mm thick copper bus bars have been used to interconnect inverter poles and current sensors. Altogether, the PCB foot-print measures 340 cm $\times$ 220 cm for a three-phase four-leg topology.

All protection and sensing mechanisms available in a commercial converter stack are present in this design as well. This includes IGBT de-saturation fault detection incorporated in gate-drive card [11], over-current protection, dc bus over and under-voltage protection, heat-sink over-temperature fault detection using thermostat, voltage sensing and current sensing circuitry, the details of which are discussed in [18] and [19]. It may be seen on the PCB that the distance between the device and gate driver is less than 5-cm, which leads to small gate parasitic inductance.

Changing switching frequency of operation would alter the losses in a device and hence operating power level of the converter needs to be changed appropriately to maintain a given device junction temperature for a given heat-sink arrangement. Using the loss equations discussed in

Item	Description	Component ratings	
		Module	Discrete
Capacitor	Package	Screw type	Snap in
	Part no.	CGS202T450 -X5C	382LX102M4 -500B062V
	Quantity used	2 (in series)	4 (2 × 2 in series)
	Rated capacitance	1000 μF	1000 μF
	Rated Voltage	450 V	450 V
	Rated current ripple	32 A	21.5 A
	Power loss	14.4 W	11.2 W
	Unit price (INR)	Rs 10,218	Rs 2,387
	Total cost(INR)	Rs 20,436	Rs 9,548
IGBT	Package	Module	TO-247
	Part no.	SKM50GB -12T4	IKW40N -120H3
	Voltage rating	1200 V	1200 V
	Current rating	81 A	80 A
	IGBT loss	59.3 W	62.6 W
	Diode loss	4.7 W	6 W
	Total loss	64 W	68.6 W
	IGBT $R_{\theta jc}$	0.53°C/W	0.31°C/W
	Diode $R_{\theta jc}$	0.84°C/W	1.1°C/W
	Quantity	3	6
	Unit price (INR)	Rs 7,610	Rs 690
	Total cost (INR)	Rs 22,830	Rs 4,140
Current sensor	Package	Panel mount	PCB mount
	Part no.	HAS-50S	HLSR-32P
	Quantity	3	3
	Unit price (INR)	Rs 2,500	Rs 1,200
	Total cost (INR)	Rs 7,500	Rs 3,600
Heat sink	Total cost (INR)	Rs 6,000	Rs 6,000
Miscellaneous	PCB	—	Rs 5,000
	Bus-plate assembly	Rs 4,000	—
	Relays	Rs 2,000	Rs 1,000
Overall system cost (INR)		Rs 62,766	Rs 29,288

Switching frequency (kHz)	60 W (kVA)	45 W (kVA)	30 W (kVA)
5	25	20	15
10	20	16	12
15	17	13	10
20	14	11	8
25	12	9	7
30	10	8	6

could increase the size and weight of the system, or reduction in switching frequency f_{sw} below 5 kHz, by which the capacity of the device is underutilized.

It can be seen from table 7 that a discrete-device-based PCB inverter would cost only half of that of a module-based design. Figure 6 compares relative sizes of the PCB-based inverter and a similar-rated commercially available module-based four-leg converter design [13], which employs screw-type DC bus capacitors, off-the-shelf IGBT heat sinks and radial blower fans. It can be noticed that the PCB based approach accommodates all the requisite components of the system and yet leads to a more compact design in terms of size and weight. Commercially available converter stacks are not only expensive but also available only for power levels of 50 kVA and above typically.

Figure 7. Experimental set-up showing power converter along with digital controller and protection card.

Figure 8. Clamped inductive switching during double-pulse test of IGBT at 800 V, 40 A, showing device voltage and current during second turn-on pulse.

Hence, for requirements up to 20 kVA, one invariably ends up procuring a fairly overrated stack.

4. Experimental results

The experimental set-up used for evaluating the power converter performance is shown in figure 7, where the tests are conducted with inductive loads.

Figure 8 shows test result of a standard double-pulse test [20] conducted on a single IGBT, switching at 800 V and 40 A. It can be seen that gate voltage V_{gs} transitions are clean and free from undesirable oscillations. About 30% overshoot in current is observed during turn-on due to diode reverse recovery, and about 15% overshoot is observed in turn-off voltage due to stray inductance. The corresponding turn-on T_{on} and turn-off T_{off} times are 350 and 150 ns, respectively. The measured stray inductance in the circuit, inclusive of that due to DC-bus plane, capacitors and device lead inductance, is about 50 nH.

Figure 9. Inverter voltage and load current waveforms at 5.5 kVA operation, 20 kHz switching frequency, 220 V, 25 A and zero p.f. inductive load.

Figure 10. Thermal test result at 5.5 kVA operation and 20 kHz switching frequency, showing (a) real image and (b) Thermal image.

Table 8. Comparison of thermal experimental results with theoretical estimation for inverter operation at 50.5 W loss per device.

Test condition	ΔT_c	ΔT_c	Err (%)
	(theoretical) (°C)	(measured) (°C)	
1 ϕ , 5.5 kVA, 400 Vdc, 20 kHz f_{sw} , 0 p.f.	82.9	74.6	10
3 ϕ , 10.5 kVA, 800 Vdc, 10 kHz f_{sw} , 0 p.f.	105.5	101	4.2

Figure 9 shows the converter pole voltage and load current waveforms when the converter is operated as a single-phase H-bridge inverter at a power level of 5.5 kVA, zero p.f. and 10 kHz carrier frequency. The calculated loss per device using the method discussed in section 2.2 is 50.5 W. Figure 10 shows the corresponding thermal image at steady state.

Table 8 shows the calculated and experimentally measured case-temperature rise for different operating conditions. It can be seen that there is a close match between predicted and measured temperature rise of the device case. With de-rating of switching frequency to 5 kHz, the operating power level can be pushed to 20 kVA. Experimental verification of the design has been done up to a power level of 15 kVA, at 10 kHz

switching frequency [21]. It can be seen that the suggested heat-sink design procedure acts as a good starting point for graduate level students to design a power converter.

For academic and research institutes, for power levels ranging up to 20 kVA, laboratory-built design not only serves as an economic alternative but also allows the students to experience the design process, which includes heat-sink selection, choice of devices, loss evaluation and its switching characteristics, dc-link current and selection of capacitors, PCB layout design and trace clearance issues.

5. Conclusion

A practical power converter design approach is presented and the same is employed to design a 20 kVA three-phase two-level power converter with state-of-the-art discrete devices and components. A comparison is made with a similar-rated converter with IGBT modules. The system cost of a module-based design was found to be more than twice that of the discrete design. This difference arises primarily due to the fact that semiconductor modules by themselves are far more expensive than individual devices of similar rating, and that modules necessitate usage of expensive screw-type dc-link capacitors and panel-mountable current sensors that further add to the system cost.

PCB-based discrete approach leads to a compact system with minimal parasitics and is appropriate for power levels up to 20 kVA. Experimental verification of the design has been done up to a power level of 15 kVA. There is a close match between the theoretically predicted and experimentally measured heat-sink thermal resistance. Also, measured voltage excursions and ringing due to stray inductances are minimal in the circuit.

Experimental results thus show the high performance that is achieved with the power converter designed in laboratory, in terms of switching transients, efficiency and thermal behaviour. The exercise of building a power converter in laboratory gives graduate engineering students a better insight into the system and the underlying technical challenges.

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