A nine-level hybrid symmetric cascaded multilevel converter for induction motor drive

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Abstract. A nine-level hybrid symmetric cascaded multilevel converter (MLC) fed induction motor drive is proposed in this paper. The proposed converter is capable of producing nine output voltage levels by using the same number of power cells as that of conventional five-level symmetric cascaded H-bridge converter. Each phase in this configuration consists of one five-level transistor-clamped H-Bridge (TCHB) power cell and one three-level H-bridge power cell with equal dc link voltages, and they are connected in cascade. Due to cascade connection and equal dc link voltage, the power shared by each power cell is nearly equal. Near-equal power sharing enables the feature of improving input current quality by using an appropriate phase-shifting multi-winding transformer at the converter input. In this paper, the operation of the converter is explained using staircase and hybrid multi-carrier sine PWM techniques. Further, a detailed analysis for the variations in the dc link capacitor voltages and the dc link mid-point voltage in TCHB power cell is carried out, and the analytical expressions thus obtained are presented. The performance of proposed system is analysed by simulating a 500 hp induction motor drive system in MATLAB/Simulink environment. A laboratory prototype is also developed to validate the claims experimentally.

Keywords. Multilevel converter; cascaded H-bridge (CHB); hybrid multilevel inverters; transistor-clamped H-bridge (TCHB) inverter; induction motor.

1. Introduction

The use of multilevel converters (MLCs) for high-power medium-voltage applications is now popular due to their capability for superior power quality at the input and output with low EMI and low switching losses [1–3]. There are several MLC topologies that are commercially available [2–6], out of which cascaded MLCs are popular as they feature modularity, simple control and ease of maintenance [5, 6]. Moreover, during fault conditions, the faulty cell or cells can be bypassed or replaced easily and quickly [5, 7].

However, the key limitation of cascaded MLC is the need for a large number of isolated dc power supplies. These power supplies are normally generated using a complex bulky multi-winding phase-shifting transformer at the converter utility interface [4–6]. Another drawback of cascaded MLC is the requirement for a large number of power electronic devices [4], gate drive circuits and auxiliary power supplies. In addition to this, the number of

power cells to be connected in cascade depends on output voltage levels. Therefore, in order to use the same low-power devices, the number of power cells connected in cascade increases with increase in output voltage levels. However, increase in number of power cells leads to a more complex system with a large number of passive components and most notably the increase in input transformer complexity. Increased component count and system complexity reduce the overall system reliability as well as efficiency.

To address these issues for higher level cascaded converters, several asymmetric and hybrid configurations with unequal dc link voltages or with different power cell configurations are reported in [8–18]. In asymmetric topologies, the number of output voltage levels is increased by selecting an appropriate ratio of dc link voltages [8–11]. For example, a 15-level asymmetric converter is proposed in [12] by cascading one five-level diode clamped power cell and one three-level H-Bridge (HB) power cell with dc link voltage ratio 1:6. In [13], an asymmetric CHB–MLC is reported using a five-level transistor-clamped H-Bridge (TCHB) power cell and keeping dc link voltage ratio 1:4. Hybrid asymmetric cascaded HB–MLC for Direct Torque Controlled (DTC) induction motor drive for electric or hybrid EVs is

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presented in [14]. The solution proposed in [15] can generate reasonably good quality output power using less number of power electronic devices. However, it requires a significant number of isolated dc supplies and a complex bulky isolation transformer. A hybrid cascaded converter realized by combining a three-phase inverter with half bridge legs is reported in [16]. In [19], multilevel outputs are generated using three-phase inverters and a complex multi-winding transformer at the converter output. Nevertheless, use of the asymmetric structure loses modularity [2, 20], and results in uneven power distribution among the power cells, which tends to deteriorate the input power quality [2]. One of the solutions to improve input current quality for asymmetrically loaded rectifier is suggested in [21]. However, this solution needs a complex design of input transformer and cannot handle all the loading conditions. Therefore, due to this limitation of asymmetric or hybrid cascaded converters on input power quality, the use of these converters is popular for electric vehicle applications, and have limited industrial use [20].

Several attempts have been made to increase the number of output voltage levels of symmetric CHB-MLCs as well. For example, in [22] a nine-level SCHB-MLC is proposed by cascading two five-level TCHB power cells per phase. However, in this topology, the dc link mid-point (MP) voltage balancing strategy needs to be employed for all the power cells, leading to more complex sensing and control arrangements. In [23], the number of output voltage levels in symmetric or asymmetric CHB-MLCs is increased to nearly double using a Level Doubling Network (LDN). LDN is an externally connected circuit to the CHB converter system and is similar to series active filters. The converters proposed in [22, 23] feature symmetry, uniform power distribution and significant number of redundant switching states.

To address these limitations, a nine-level hybrid symmetric cascaded converter using one five-level and one three-level HB power cell per phase is proposed in this work for induction motor drive applications. The features of proposed configuration are as follows: (a) increase in output voltage levels to nearly double of that of SCHB-MLC with the same number of power cells, (b) near-equal power distribution among the power cells (helps to improve input power quality [2, 6, 24, 25]), (c) symmetry and (d) minimized redundant switching states. Furthermore, the dc link MP voltage balancing strategy needs to be employed only for three TCHB power cells.

This paper is organised as follows. The proposed converter topology and its operating principle are discussed in section 2. Expressions for variations in dc link capacitor voltages in TCHB power cell are analysed in section 3. The simulation results obtained from the proposed converter-fed induction motor drive system and the experimental results obtained from the laboratory prototype are presented in section 4. Conclusions drawn from the proposed work are presented in section 5.

2. Proposed converter topology

The power circuit diagram of the proposed nine-level hybrid symmetric CHB-MLC fed induction motor (IM) drive system is shown in figure 1a. In this structure, each phase leg is realized using one five-level TCHB power cell (A1) and one three-level HB power cell (A2) having equal dc link voltages. The three-level power cell has a single-phase HB inverter at its output and is capable of generating three distinct output voltage levels, $+2V_{dc}$, 0 and $-2V_{dc}$ ($2V_{dc}$ is the cell dc link voltage). However, in the five-level power cell, the dc link MP is connected to one of the output terminals by means of a bi-directional switch S_{15} [13, 22]. This additional connection enables the output terminal to access the dc link MP voltage $+V_{dc}$, and hence the power cell becomes capable of generating five distinct voltage levels, $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, and $-2V_{dc}$.

Various configurations of bi-directional switches can be obtained by different combinations of diodes and IGBTs; however, the bi-directional switch that is used in TCHB power cell for proposed converter configuration is realized using four diodes and one IGBT switch as shown in figure 1b.

The expression of leg voltage waveform in m -cell cascaded MLC can be written as [5, 20] follows:

$$v_{jN} = \sum_{i=1}^m v_{ji}, \quad j \in (a, b, c) \quad (1)$$

where v_{ji} is the output of i th power cell in j phase, m is the number of power cells per phase and v_{jN} is the leg output voltage of phase j . Therefore, in conventional symmetric cascaded MLC with $m = 2$, i.e., two three-level HB power cells per phase, the number of distinct voltage levels obtained in v_{jN} is 5, and the number of levels generated in line voltage waveform (v_{line}) is 9 [5, 20].

In the proposed configuration, the five-level TCHB power cell with output voltage levels $\pm 2V_{dc}$, $\pm V_{dc}$ and 0 is in cascade with the three-level HB power cell with voltage levels $\pm 2V_{dc}$ and 0. Therefore, the distinct possible voltage levels generated in v_{jN} waveforms are $\pm 4V_{dc}$, $\pm 3V_{dc}$, $\pm 2V_{dc}$, $\pm V_{dc}$ and 0. Hence, the number of levels obtained in v_{jN} is 9 and in v_{line} is 17, which are nearly twice the number of levels obtained with conventional symmetric cascaded MLC.

Another advantage of proposed topology is equal dc link voltages in all the power cells, which makes this topology symmetric. With equal dc link voltages, the voltage rating of IGBTs in all the power cells is the same except for the switch S_{15} in TCHB power cell. The maximum voltage appearing across the IGBT in switch S_{15} is $+V_{dc}$, which is half of dc link voltage. Therefore, the voltage rating of IGBT in switch S_{15} is half of that of IGBTs used in HBs.

Furthermore, a symmetric cascaded converter has an added advantage apart from identical voltage-rated devices. Equal dc link voltage and cascade connection of power

Figure 1. (a) Power circuit of proposed nine-level hybrid symmetric cascaded MLC, (b) TCHB power cell and (c) HB power cell.

cells enable the feature of uniform power sharing among the power cells. Uniform power sharing and use of multi-winding phase-shifting transformer at the converter input eliminate the lower order harmonics from source current waveform and hence improve the input power quality. This feature makes the proposed hybrid topology suitable for industrial applications.

2.1 Operating principle

The switching states of nine switches S_{11} – S_{15} in TCHB power cell and S_{21} – S_{24} in HB power cell, of phase a along with the

outputs of individual power cells, and inverter leg are presented in table 1. It can be seen that the number of redundant switching states generated by this topology is much less compared with [22, 23]. In MLCs, redundant switching states are very common and normally used to balance the dc link voltages using space vector modulation or by using some special techniques [24]. However, the proposed converter is modulated using a multi-carrier based SPWM technique in which the switching redundancies are not beneficial for balancing dc link voltage, or balancing dc link MP voltage in TCHB power cells.

From the switching states presented in table 1, the expression for leg voltage waveform of phase a can be obtained as

$$v_{aN} = 2V_{dc}(S_{11} - S_{13}) + 2V_{dc}(S_{21} - S_{23}) + V_{dc}S_{15}. \quad (2)$$

The first two terms in (2) are similar to that of symmetric cascaded MLC, while the third term, associated with bi-directional switch S_{15} and V_{dc} (dc link MP voltage), is due to the addition of S_{15} in TCHB power cell. The term $+V_{dc}S_{15}$ in (2) offers V_{dc} voltage step at the converter output and hence the output voltage profile resolution improves from voltage step of $2V_{dc}$ to V_{dc} , i.e., increases number of output voltage levels from 5 to 9 (each level is divided in steps of V_{dc} except the 0 state).

2.2 Modes of operation

The five different operating modes of the proposed topology are shown in figure 2. In Mode I (figure 2a), the switch pairs S_{15} , S_{12} and S_{24} , S_{22} are ON in TCHB and HB power cells, respectively. This results $v_{TCHB} = +V_{dc}$, $v_{HB} = 0$ and hence $v_{aN} = +V_{dc}$. For $v_{aN} = +2V_{dc}$ in Mode II, switch pair S_{11} , S_{12} is conducting in TCHB power cell to generate $v_{TCHB} = +2V_{dc}$ and HB power cell is bypassed with the same pair of switches as in Mode I (figure 2b). For Mode III, $+3V_{dc}$ voltage level is obtained in v_{aN} by conducting switch pairs S_{15} , S_{12} and S_{21} , S_{22} in TCHB and HB power cells, respectively (figure 2c). Conduction of switch pairs S_{15} , S_{12} and S_{21} ,

Table 1. Switching states of phase a switches.

S_{11}	S_{12}	S_{13}	S_{14}	S_{15}	v_{TCHB}	S_{21}	S_{22}	S_{23}	S_{24}	v_{HB}	v_{aN}
1	1	0	0	0	$+2V_{dc}$	1	1	0	0	$+2V_{dc}$	$+4V_{dc}$
0	1	0	0	1	$+V_{dc}$	1	1	0	0	$+2V_{dc}$	$+3V_{dc}$
0	1	0	1	0	0	1	1	0	0	$+2V_{dc}$	$+2V_{dc}$
1	1	0	0	0	$+2V_{dc}$	0	1	0	1	0	$+2V_{dc}$
0	1	0	0	1	$+V_{dc}$	0	1	0	1	0	$+V_{dc}$
0	1	0	1	0	0	0	1	0	1	0	0
1	0	1	0	0	0	1	0	1	0	0	0
0	0	1	0	1	$-V_{dc}$	1	0	1	0	0	$-V_{dc}$
0	0	1	1	0	$-2V_{dc}$	1	0	1	0	0	$-2V_{dc}$
1	0	1	0	0	0	0	0	1	1	$-2V_{dc}$	$-2V_{dc}$
0	0	1	0	1	$-V_{dc}$	0	0	1	1	$-2V_{dc}$	$-3V_{dc}$
0	0	1	1	0	$-2V_{dc}$	0	0	1	1	$-2V_{dc}$	$-4V_{dc}$

Figure 2. Operating modes. (a) Mode I: $v_{aN} = +V_{dc}$, with S_{15} , S_{12} ON and HB cell bypassed, (b) Mode II: $v_{aN} = +2V_{dc}$, with S_{11} , S_{12} ON and HB cell bypassed, (c) Mode III: $v_{aN} = +3V_{dc}$, with S_{15} , S_{12} , S_{21} and S_{22} ON, (d) Mode IV: $v_{aN} = +4V_{dc}$, with S_{11} , S_{12} , S_{21} and S_{22} ON and (e) Mode 0: $v_{aN} = 0$, with S_{14} , S_{12} , S_{24} and S_{22} ON.

S_{22} results in outputs of $+V_{dc}$, $+2V_{dc}$ in TCHB and HB power cells, respectively. Similarly, output level of $+4V_{dc}$ is obtained in Mode IV (figure 2d) by operating switch pairs S_{11} , S_{12} and S_{21} , S_{22} with individual cell outputs as $+2V_{dc}$. In Mode 0, both the power cells are bypassed to get $v_{aN} = 0$ (figure 2e). The nine-level staircase leg voltage waveform and stepped output waveforms of TCHB, HB power cells are shown in figure 3.

2.3 PWM technique

In the proposed configuration, the switches in all the power cells do not have uniform and identical switching conditions. Therefore, a level-shifted In-Phase Disposition (IPD) multi-carrier [5, 20, 25, 26] based hybrid PWM technique is used to generate the PWM switching signals.

In the level shift PWM technique, total $n - 1$ number of vertically shifted triangular carriers are required for n -level SCHB-MLC [20, 25, 26]. Therefore, for the nine-level converter, total eight triangular carriers (four positive and four negative) of amplitude 0.25 pu each are used as shown in figure 4a. Four positive carriers between 0 and 1 are defined as C_1 – C_4 , whereas four negative carriers are defined as C'_1 – C'_4 from 0 to -1 . The lowermost carrier is termed as 4 and the uppermost as 1.

2.4 Hybrid PWM technique

In the hybrid PWM technique, all eight triangular carriers are used for TCHB power cells while only two carriers C_3 , C'_3 are used for HB power cells. In the TCHB power cell, five carriers C_1 , C_2 , C_3 , C_4 , C'_4 are used for switch S_{11} and five carriers C'_1 , C'_2 , C'_3 , C'_4 , C_4 for switch S_{14} . For bi-directional switch S_{15} all eight carriers are used, which results in continuous switching of S_{15} in one fundamental cycle. It is to be noted that only one switch from switch set (S_{11} , S_{14} , S_{15}) is ON at a time to avoid short circuit across the dc link. The switches S_{12} and S_{13} are complementary to each other and operate at the fundamental frequency. In HB power cells, the triangular carriers C_3 , C'_3 are used for switches S_{21} , S_{23} respectively. The switching signals to lower switches S_{22} and S_{24} are complementary to that of upper switches S_{21} and S_{23} , respectively.

The equations of three reference modulating signals for phases a , b and c can be defined by

$$v_{aN}^* = m_i \sin \omega_o t$$

$$v_{bN}^* = m_i \sin \left(\omega_o t - \frac{2\pi}{3} \right)$$

$$v_{cN}^* = m_i \sin \left(\omega_o t + \frac{2\pi}{3} \right)$$

Figure 3. Output voltage waveforms: (a) v_{TCHB} , (b) v_{HB} and (c) v_{aN} .

Figure 4. (a) Pulses to switches S_{11} , S_{15} , S_{14} and S_{12} in TCHB power cell and (b) pulses to switches S_{21} and S_{23} in HB power cell ($f_{cr} = 1950$ Hz, $m_f = 39$).

where $\omega_o = 2\pi f_o$, f_o is output frequency and m_i is the modulation index. As the proposed converter can generate total nine distinct voltage levels (four in the positive half, four in the negative half and zero state) at the output, the leg voltage waveforms v_{jN} can be divided into four sections in the positive as well as in the negative halves of a fundamental cycle. Therefore, the switching sequence based on the reference modulating signal v_{jN}^* is now defined as follows.

Table 2. Hybrid PWM technique.

v_{aN}^*	v_{TCHB}	v_{HB}	v_{aN}
$1.0 > v_{aN}^* > 0.75$	$+2V_{dc}$	$+2V_{dc}$	$+4V_{dc}$
$0.75 > v_{aN}^* > 0.5$	$+V_{dc}$	$+2V_{dc}$	$+3V_{dc}$
$0.5 > v_{aN}^* > 0.25$	$+2V_{dc}$	0	$+2V_{dc}$
$0.25 > v_{aN}^* \geq 0$	$+V_{dc}$	0	$+V_{dc}$
$0 > v_{aN}^* > -0.25$	$-V_{dc}$	0	$-V_{dc}$
$-0.25 > v_{aN}^* > -0.5$	$-2V_{dc}$	0	$-2V_{dc}$
$-0.5 > v_{aN}^* > -0.75$	$-V_{dc}$	$-2V_{dc}$	$-3V_{dc}$
$-0.75 > v_{aN}^* > -1.0$	$-2V_{dc}$	$-2V_{dc}$	$-4V_{dc}$

When the value of v_{jN}^* is from 0 to $+0.25$, the possible leg voltage output should be $+V_{dc}$ and hence switch pair S_{15} , S_{12} in TCHB power cell is turned ON and HB power cell is bypassed using S_{22} , S_{24} . When the reference is in the range of $+0.25$ to $+0.5$, possible leg voltage output should be $+2V_{dc}$; therefore the switch pair S_{11} , S_{12} of TCHB power cell is switched ON and HB power cell output is made zero. If value of v_{jN}^* ranges from 0.5 to 0.75, then the expected voltage output should be $+3V_{dc}$ and hence switches S_{15} , S_{12} of TCHB power cell and S_{21} , S_{22} of HB power cell are turned ON. For $+4V_{dc}$ leg voltage output, the reference v_{jN}^* should lie between 0.75 and 1.0 and the outputs of both the power cells should be $+2V_{dc}$. Therefore, S_{11} , S_{12} and S_{21} , S_{22} are turned ON in TCHB and HB power cells, respectively. For zero output voltage, both the cells are bypassed. The eight output voltage steps (zero state not shown) along with the reference signal v_{jN}^* are presented in table 2.

The generated PWM signals for the switches in TCHB and HB power cells are shown in figure 4. It can be noted that the switching signal to switch S_{15} is continuous, whereas switching signal to S_{12} is a square wave of fundamental frequency. The carrier frequency selected for this study is 1950 Hz, which is typical for high-power converters. The PWM output voltage waveforms generated using hybrid technique are shown in figure 5. The harmonic spectrum of leg voltage (v_{aN}) and line voltage (v_{ab}) waveforms is shown in figure 6a and b respectively. Note that the dominant harmonic component in v_{aN} waveform is at carrier frequency, 1950 Hz [20], while it is eliminated from v_{ab} waveform.

It can be seen from figure 4 that the average switching frequency of switches in HBs is much less than the carrier frequency, while switch S_{15} is switched at carrier frequency. Hence, in the proposed topology with hybrid PWM technique, the average inverter switching frequency becomes much less than the carrier frequency. Switch S_{15} is switched from 0 to $+V_{dc}$, which is half of the dc link voltage. Therefore, switching loss in S_{15} is much reduced though it switches at carrier switching frequency.

Figure 5. Voltage waveforms: (a) TCHB power cell v_{TCHB} , (b) HB power cell v_{HB} , (c) leg voltage v_{aN} and (d) line voltage v_{ab} .

Figure 6. Harmonic spectrum of (a) v_{aN} and (b) v_{ab} ($f_{cr} = 1950$ Hz, $m_f = 39$).

3. Capacitor voltage unbalance in TCHB power cell

As mentioned earlier, the switch S_{15} in TCHB power cell operates at carrier frequency and allows the bidirectional flow of chopped load current to the dc link MP. Moreover, the envelope of this current is same as that of load current. Therefore, due to the flow of this PWM current to the dc link MP, the instantaneous values of dc link capacitor voltages deviate from half of dc link voltage, i.e., $+V_{dc}$. In this section, an analytical expression for the variations in capacitor voltages are derived and analysed in detail.

In the TCHB power cell, the average value of PWM current through switch S_{15} during the positive and the negative half cycles respectively can be given as

$$i_{avr}^+ = \frac{\sum_{i=1}^{n_p} D_i i_i^+}{n_p} \quad \text{and} \quad i_{avr}^- = -\frac{\sum_{j=1}^{n_n} D_j i_j^-}{n_n}, \quad (3)$$

where i^+ , i^- are the instantaneous magnitudes of PWM current in positive and negative halves, respectively, D is the duty cycle and n_p , n_n are the total number of switchings in positive and negative halves of power cycles, respectively. The expression for voltage deviation of a capacitor can be given by

$$\Delta v = \frac{\Delta Q}{C} = \frac{\int idt}{C}. \quad (4)$$

Therefore, from (3), (4), the voltage variation during positive and negative halves (Δv^+ and Δv^-) can be obtained as

$$\Delta v^+ = \frac{\sum_{i=1}^{n_p} D_i i_i^+}{C} \quad \text{and} \quad \Delta v^- = -\frac{\sum_{j=1}^{n_n} D_j i_j^-}{C}.$$

For one complete fundamental cycle, the MP voltage variation can be expressed as

$$\Delta v = (\Delta v^+ + \Delta v^-) = \frac{1}{C} \left(\sum_{i=1}^{n_p} D_i i_i^+ - \sum_{j=1}^{n_n} D_j i_j^- \right). \quad (5)$$

At steady state and with synchronized triangular carriers, $i_{avr}^+ = -i_{avr}^-$ and $n_p = n_n$, and hence the average value of MP current is zero, which ensures natural balancing of capacitor voltages with average MP voltage close to $+V_{dc}$. However, during transients or due to parameter mismatch, i_{avr}^+ and i_{avr}^- may not be equal, which results in imbalance in capacitor voltages and shifting of MP voltage from $+V_{dc}$. Furthermore, the dc link MP current profile depends on load current magnitude, load power factor and device switching frequency. Therefore, for the proposed configuration, a balancing technique must be employed to ensure balancing of the capacitor voltages for the entire operating range [22, 26]. In addition, there is a 100 Hz ripple voltage present in the dc link voltages in all the power cells, which appears due to single-phase operation of a power cell. The nature of PWM current and variation in capacitor voltages v_{C1} , v_{C2} are shown in figure 7.

4. Proposed converter employed for induction motor speed control drive

To evaluate the performance of the proposed drive system, the nine-level converter fed 500 hp induction motor drive is simulated in MATLAB/Simulink environment with

Figure 7. PWM current through switch S_{15} and dc link capacitor voltages v_{C1} , v_{C2} .

Table 3. Simulation parameters.

Parameters and symbols	Values
Utility supply	2.3 kV, 50 Hz
Source impedance r_s, l_s	0.044 Ω (0.05 pu), 3.58 mH (0.1 pu)
Isolation transformer	85 kVA, 2300/660 V, Y/Y(3), Y/ Δ (3)
Cell dc link voltage, $2V_{dc}$	930 V
DC link capacitors C_1, C_2	3300 μ F
Switching frequency, f_{cr}	1950 Hz ($m_f = 39$)
Output frequency, f_o	50 Hz
Induction motor	500 hp, 2.3 kV, 50 Hz, 4P, 1485 rpm

Figure 8. Control block diagram of indirect rotor-field-oriented induction motor drive.

simulation parameters as listed in table 3. The indirect field-oriented control technique [20, 27, 28] is used to control the induction motor. The block diagram is shown in figure 8.

4.1 Simulation results

The HB and TCHB power cell voltages, the nine-level leg voltage of phase a and common-mode voltage v_{com} are shown in figure 9. The line voltage waveforms along with the line current waveforms are shown in figure 10. At rated load torque condition, the average dc link powers in TCHB and HB power cells are around 50 and 60 kW, respectively,

Figure 9. Phase a output voltage waveforms: v_{TCHB} , v_{HB} , v_{aN} and v_{com} .

Figure 10. Output line voltage (v_{line}) and load current (i_{load}) waveforms.

Figure 11. (a) Average dc link powers in TCHB and HB power cells, and source current (i_{source}) waveforms; (b) i_{source} harmonic spectrum.

Figure 12. Motor speed (ω_r) and electromagnetic torque T_{em} .

Figure 13. DC link current, capacitor voltages and MP current in TCHB power cell.

as shown in figure 11a. Moreover, the source current drawn by the drive system is also presented in figure 11a. Due to the use of star-delta, star-star multi-winding transformers and near-equal power distribution feature of proposed topology, it can be seen that the quality of source current waveform has significantly improved. The harmonic spectrum of source current waveform is shown in figure 11b. It can be seen that the magnitudes of 5th, 7th, 11th and 13th harmonic components are $\approx 2\%$, 1.5% , 3% and 2.1% , respectively, with $l_s = 0.1$ pu.

To analyse the dynamic behaviour of the system, rated load torque of 2.4 kN-m is suddenly applied to the motor shaft at time $t = 1.5$ s, and then it is decreased to 1.0 kN-m at time $t = 3.5$ s. A quick change in electromagnetic torque in response to the applied load torque can be observed in figure 12, keeping motor speed almost constant at 1300 rpm.

In TCHB power cell, the dc link current, dc link capacitor voltages v_{C1} , v_{C2} and MP current are shown in figure 13. The capacitor voltages are almost balanced with average voltage close to $+V_{dc}$.

4.2 Power loss and efficiency calculations

In this work, the power losses in SKM75GB120V IGBT module (two IGBTs connected in series, one leg of H-bridge) and SKKD 60F diode bridge module (two series-connected fast acting diodes) for the bidirectional switch S_{15} are estimated.

The conduction loss of a device depends on the ON state voltage drop across the device $v_{on,device}$, and the instantaneous current $i(t)$ flowing through it. Moreover, $v_{on,device}$ is a function of $i(t)$ and the corresponding characteristics curves can be obtained from the device data-sheets. In this loss calculations, MATLAB Curve Fitting toolbox is used to fit these curves into appropriate exponential or polynomial functions and equations for $v_{on,device}$ are obtained [22].

The expression for the conduction power loss of a device (IGBT/diode) can be obtained by

$$p_{cond,device} = v_{on,device}i(t). \quad (6)$$

The equations of $v_{on,device}$ of selected IGBT and diode modules are obtained as

$$v_{on,IGBT} = (1.39e^{0.0068i(t)} - 1.13e^{-0.072i(t)}). \quad (7)$$

$$v_{on,diode} = (1.49e^{0.0026i(t)} - 1.06e^{-0.033i(t)}). \quad (8)$$

Therefore, by substituting (7), (8) into (6), the expressions for $p_{cond,IGBT}$ and $p_{cond,diode}$ can be given by

$$p_{cond,IGBT} = (1.39e^{0.0068i(t)} - 1.13e^{-0.072i(t)})i(t), \quad (9)$$

$$p_{cond,diode} = (1.49e^{0.0026i(t)} - 1.06e^{-0.033i(t)})i(t). \quad (10)$$

In steady state, the average of $p_{cond,IGBT}$, $p_{cond,diode}$ over a fundamental cycle gives the average conduction power losses in IGBT and diode.

For switching loss calculations, the turn-on and turn-off energy associated with IGBT module SKM75GB120V can be obtained from its data-sheet as

$$e_{ON,IGBT} = [1.069 \times 10^{-5}i(t)^3 - 1.2 \times 10^{-3}i(t)^2 + 0.12i(t) + 0.0048]. \quad (11)$$

$$e_{OFF,IGBT} = [-7.22 \times 10^{-8}i(t)^3 - 8.9 \times 10^{-8}i(t)^2 + 0.13i(t) - 0.08]. \quad (12)$$

Therefore, the expressions for turn-on ($P_{ON,IGBT}$) and turn-off ($P_{OFF,IGBT}$) power losses can be given by

$$P_{ON,IGBT} = (1.069 \times 10^{-5}i(t)^3 - 1.2 \times 10^{-3}i(t)^2 + 0.12i(t) + 0.0048)/T. \quad (13)$$

$$P_{OFF,IGBT} = (-7.22 \times 10^{-8}i(t)^3 - 8.9 \times 10^{-8}i(t)^2 + 0.13i(t) - 0.08)/T. \quad (14)$$

Figure 14. Loss distribution of phase *a* switches.

Figure 15. Variations in losses with speed.

Since the module SKKD 60F has soft-recovery diodes, the power loss due to reverse recovery in this module is neglected.

The power loss distribution among the switches S_{11} , S_{13} , S_{14} , S_{15} , S_{21} and S_{24} in phase *a* is plotted in figure 14. It can be seen that, unlike conventional SCHB converter, the loss distribution is not symmetric among the devices for the proposed converter configuration. The non-symmetric loss distribution is because they occur mainly in the IGBTs, and all the IGBTs operating at different switching conditions, similar to the level-shift PWM technique. In switch S_{15} , as the diodes are continuously conducting for a complete fundamental cycle, power loss in it is significantly higher compared to anti-parallel diodes in rest of the switches. The loss profiles of switches S_{12} , S_{23} and S_{22} are not shown as they have similar loss profile as that of switches S_{13} , S_{21} and S_{24} , respectively. The variation in losses for motor speed range from 1300 to 400 rpm with constant load torque is shown in figure 15.

For efficiency calculation, the converter efficiency is defined by (15):

$$\eta_{conv} = \frac{P_o}{(P_o + P_{loss})} \quad (15)$$

The converter efficiency (η_{conv}) is calculated using (15) as 98.63%.

Figure 16. Laboratory prototype.

4.3 Experimental results

A scaled-down laboratory prototype of the proposed topology is built (figure 16) and tested in the laboratory using *RL* load. In this set-up, six power cells are realized using six rectifier-inverter stacks from SEMIKRON, and to realize TCHB power cell, the same stack is modified by connecting a bi-directional switch SK60GM123 from one of the output terminals to the dc-link MP. All power cells are fed by six phase-shifting isolation transformers and the transformer primaries are then connected to a three-phase variac. The PWM switching signals are generated using a TMS320F28377D Delfino experimenter kit. The components and their parameters used in this experimental work are listed in table 4.

Experimental results of cell voltage waveforms of phase *a* along with nine-level leg voltage waveform v_{aN} are shown in figure 17a. The leg voltage and line voltage waveforms are presented in figure 17b. The RMS values of line and leg voltage waveforms are 132 V and 75 V, respectively. Since the dc link voltage, $2V_{dc}$, is approximately 60 V, voltage step in leg voltage waveform is 30 V. Three-phase load current waveforms with RMS value 3.5 A are shown in figure 18. The source current drawn from the utility supply and its harmonic spectrum are presented in figure 19a and b respectively. It can be observed that due to

Table 4. Hardware setup parameters.

Parameters	Values
Utility supply	3- Ph, 400 V, 50 Hz
Isolation transformer	3 kVA, 200/200V, Y/Y (3), Y/ Δ (3)
Power cells (SEMIKRON)	3-ph Diode Rectifier+IGBT Inverter stack
HB IGBT modules	SKM75GB12T4
HB Gate drivers	SKYPER32R
HB dc link capacitors	3300 μ F
TCHB IGBT modules	SKM75GB12T4
TCHB bi-directional switch	SK60GM123
TCHB Gate drivers	SKHI22A
TCHB dc link capacitors	3300 μ F
Switching frequency, f_{cr}	1950 Hz ($m_f = 39$)
RL load	0.999 pu, 0.043 pu
3-ph variac	400 V, 16 A

Figure 17. Experimental results: (a) cell voltages v_{TCHB} , v_{HB} and leg voltage v_{aN} and (b) leg voltage v_{aN} , line voltage v_{ab} .

near-equal power distribution feature and with phase-shifting transformer action, the lower order harmonics are much suppressed in source current waveform. The harmonic spectrum of source current waveform is obtained

Figure 18. Experimental result of three-phase load currents i_a , i_b and i_c . **Figure 19.** Experimental results: (a) i_{source} waveform and (b) harmonic spectrum.

using a TEKTRONIX TPS2014B oscilloscope and plotting the data in MATLAB.

Figure 20a shows the voltages across capacitors C_1 , C_2 and current through switch S_{15} in TCHB power cell. It is to be noted that the nature of PWM current flowing through switch S_{15} is similar to the current obtained in simulation study (figure 7). Moreover, the average values of capacitor voltages v_{C1} and v_{C2} are almost equal. Figure 20b shows the PWM voltage appearing across switch

Figure 20. Experimental results of TCHB power cell: (a) dc link capacitor voltages v_{C1} , v_{C2} , (b) current through switch S_{15} (i_{S15}) and (c) voltage across switch S_{15} (v_{S15}).

S_{15} , confirming the transitions of V_{dc} , i.e., 30 V only with dc link voltage of 60 V.

5. Conclusion

A three-phase six-cell nine-level symmetric hybrid cascaded MLC fed high-performance induction motor drive is presented in this paper. Since, with the proposed topology, the output voltage levels are increased from 5 to 9, which is nearly double of that of SCHB–MLC with the same number of power cells, sinusoidal load currents are obtained without using an output filter. Moreover, in the proposed configuration it is observed that the power shared by all the power cells is almost equal. Uniform power sharing helped in improving the input power quality by using six phase-shifting isolation transformers. The simulation results obtained for the proposed drive system are presented and discussed. Experimental results obtained from a laboratory prototype are presented to confirm the effectiveness of the proposed converter system.

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