Discontinuous conduction mode analysis of phase-modulated series resonant converter

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Abstract. This paper proposes an analytical approach to derive voltage gain for phase-modulated dc–dc series resonant converter (SRC) operating in discontinuous conduction mode (DCM). The conventional fundamental harmonic approximation technique is extended for a non-ideal series resonant tank to clarify the limitations of SRC operating in continuous conduction mode (CCM). The DCM analysis is described in a normalized form defining appropriate base quantities. The converter is analysed both in time and frequency domain to derive a non-linear algebraic function of diode rectifier extinction angle. The root of this function is numerically determined using MATLAB and used to predict the dc bus voltage. Analytical derivation of critical load resistance is discussed, which indicates the CCM–DCM boundary condition. Experimental results are presented to validate the analysis.

Keywords. Discontinuous conduction mode (DCM); phase modulation; series resonant converter (SRC); time domain analysis; frequency domain analysis; critical load resistance.

1. Introduction

High efficiency and power density are reportedly achieved in dc–dc converters by adopting soft-switching techniques [1–4], viz., zero voltage switching (ZVS) and zero current switching (ZCS). Phase-modulated (PM) series resonant converters (SRCs) [5, 6] are widely used for dc–dc power conversion as they offer ZVS of full-bridge (FB) MOSFETs and ZCS of rectifier diodes. These converters are traditionally operated in continuous conduction mode (CCM) [7, 8], typically above resonant frequency, to guarantee ZVS of FB switches. Since CCM operation of SRC (CCMSRC) stipulates nearly sinusoidal state variables, conventional fundamental harmonic approximation (FHA) technique [10] is used to derive the voltage conversion ratio (A_v). Thus, selection of tank parameters for given input–output voltage levels and power rating of the converter is straightforward. However, as discussed later in this paper, CCMSRC compromises A_v significantly while ensuring ZVS in entire modulation range.

In contrast, discontinuous conduction mode (DCM) operation of SRC (DCMSRC) retains the ZCS property of rectifier diodes while ensuring ZCS of H-bridge MOSFETs [9]. Load- and modulation-independent soft-switching, while operating at tank resonant frequency, makes DCMSRC superior compared with its CCM counterpart. But FHA approach [10] and extended describing-function-

based techniques [11, 12] are not applicable for DCMSRC due to the discontinuous nature of inductor current. Absence of an analytical formulation of A_v complicates the DCMSRC design process, requiring repeated circuit simulations for design convergence.

Time domain analysis of DCMSRC is reported in [13] to derive A_v as a function of PM angle (α) and diode bridge rectifier (DBR) extinction angle (β). But this approach overlooks the fact that β itself is a function of α and load resistance (R_L). Thus it fails to analyse load-dependent property of A_v , which is inevitable in DCMSRC [9]. The technique presented in [9] expresses A_v as a function of not only α and β but loading condition also. But it does not report any analytical formulation for β and thus fails to determine A_v for any arbitrary α and R_L .

Generally, SRCs exhibit two different modes of continuous conduction under fixed-frequency PM operation, viz., CCM with energy recovery to supply (CCM1) and CCM with no energy recovery to supply (CCM2) [14]. During CCM1, the inductor current (i_s) lags the positive rising edge of tank input voltage (v_t). It results in a switching sub-interval when v_t is positive but i_s is negative. It means the energy stored in resonant tank is fed back to the input dc supply. On the other hand, CCM2 forces the current i_s to lead the positive rising edge of v_t . It indicates that v_t remains zero when i_s is negative. Thus the tank energy is dissipated in MOSFET on resistances and effective series resistance (ESR) of tank network. Boundary conditions for both CCM1–DCM and CCM2–

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DCM are reported in [13–15] considering above-resonance PM operation. But CCMSRC operated at resonant frequency ensures the fundamental of i_s to be in phase with the fundamental of v_t and thus CCM2 does not appear during the entire PM and load range [14]. Consequently, this paper considers only the CCM2–DCM boundary condition as the converter is switched at resonant frequency.

This paper presents DCM analysis of PM SRC, switched at resonant frequency, using time and frequency domain representations. Structured derivation of A_v is presented, which requires numerical solution of a single well-defined non-linear algebraic equation. Also, critical load resistance indicating CCM–DCM boundary condition is derived by solving two simultaneous non-linear algebraic equations. The remaining part of the paper is organized as follows. Section 2 analyses transfer characteristics of non-ideal SRC using FHA approach to clarify the drawbacks of CCM operation. Time domain analysis of DCMSRC is discussed in section 3.1 to explain soft-switching operation of FB MOSFETs and rectifier diodes. Section 3.2 analyses DCMSRC in frequency domain using multi-order decomposition technique [16]. Critical load resistance is determined in section 3.3 to define the CCM–DCM boundary of SRC. This mode boundary and analytical formulation of converter voltage gain are experimentally validated in section 4.

2. FHA analysis of non-ideal SRC

The complete circuit diagram of series resonant boost dc–dc converter is shown in figure 1a. The H-bridge is switched using PM approach [17–19]. It produces a high-frequency square/quasi-square wave to excite the resonant tank. The tank comprises two resonating elements: inductance L and capacitance C . They are connected in series and terminated at the primary of a step-up high-frequency transformer (HFT). Secondary of the HFT is connected to DBR, followed by a filter capacitor, C_f , to attenuate the

switching harmonics. The following assumptions are considered for the subsequent analysis.

1. Primary side MOSFETs and rectifier diodes are ideal.
2. Dead-time between the gating signals of FB MOSFETs are neglected.
3. The HFT does not contain any air-gap and thus offers very high magnetizing inductance. Hence, the parallel magnetizing branch is excluded from analysis of the tank network, shown in figure 1b.
4. The only non-ideality, r , comprises winding resistances of both inductor and transformer and ESR of capacitor.
5. The leakage inductance of HFT is included in the tank inductance L .

Assuming CCM operation, input admittance characteristic ($I_s(s)/V_t(s)$) and voltage transfer characteristic ($V_p(s)/V_t(s)$) of the tank network are derived using FHA approach [10]. For a given HFT turns ratio 1: N and load resistance, R_L , these transfer functions are normalized with respect to its natural frequency ω_0 and expressed as follows:

$$\begin{aligned} \frac{I_s(s)}{V_t(s)} &= \frac{s_0 \sqrt{C/L}}{s_0^2 + s_0(Q_0 + Q_r) + 1}, \quad s_0 = s/\omega_0, \\ \frac{V_p(s)}{V_t(s)} &= \frac{s_0 Q_0}{s_0^2 + s_0(Q_0 + Q_r) + 1}, \quad \omega_0 = 1/\sqrt{LC}, \\ Q_0 &= R \sqrt{C/L}, \quad Q_r = r \sqrt{C/L}, \quad R = (8R_L)/(\pi^2 N^2). \end{aligned} \quad (1)$$

ZVS of all four FB MOSFETs under PM demands tank input current i_s to lag positive rising edge of v_t . This is achieved by switching the converter at a frequency $\omega_1 > \omega_0$. Depending on required maximum PM for voltage regulation, ω_1 shifts far to the right half of ω_0 axis as shown in figure 2a. However, figure 2b clarifies that switching at ω_1 significantly compromises the converter voltage gain at rated load. This analysis clarifies the limitations of SRC when operated at CCM under PM. Thus to extract the maximum gain during CCM operation, the switching frequency f_s is chosen to be

Figure 1. (a) Series resonant dc–dc converter and (b) non-ideal tank network.

Figure 2. (a) Input admittance characteristic and (b) voltage transfer characteristic.

$$f_s = \omega_0/2\pi = 1/(2\pi\sqrt{LC}). \quad (2)$$

Careful inspection of figure 2b reveals minute variation in voltage gain at ω_0 during rated and 20% load conditions. It is caused by the voltage drop across r . This effect is considered while deriving the CCM voltage gain expression (A_{vC}) for the entire power train using FHA analysis [10]:

$$\begin{aligned} A_{vC} &= \frac{\langle V_{dc} \rangle}{\langle V_g \rangle} = \frac{\langle V_t \rangle}{\langle V_g \rangle} \frac{\langle V_p \rangle}{\langle V_t \rangle} \frac{\langle V_s \rangle}{\langle V_p \rangle} \frac{\langle V_{dc} \rangle}{\langle V_s \rangle}, \\ &= \frac{2\sqrt{2}}{\pi} \sin\left(\frac{\alpha}{2}\right) \frac{R}{R+r} N \frac{\pi}{2\sqrt{2}}, \\ &= N \sin\left(\frac{\alpha}{2}\right) \frac{R}{R+r}, \end{aligned} \quad (3)$$

where ' $\langle \rangle$ ' denotes respective rms quantities and α is the modulation angle as shown in figure 3a.

3. DCM analysis of SRC

All the parameters and state variables are referred to the primary side of HFT and normalized using the base quantities defined as follows:

$$V_B = V_{gmin}, \quad Z_B = \sqrt{L/C}, \quad I_B = V_B/Z_B, \quad (4)$$

where V_{gmin} denotes minimum input voltage. Per unit (p.u.) definitions of different parameters, state variables, input and output voltages are listed as follows:

$$\begin{aligned} r_{pu} &= \frac{r}{Z_B}, \quad R_{Lpu} = \frac{R_L}{N^2 Z_B}, \quad i_{spu} = \frac{i_s}{I_B}, \quad v_{cpu} = \frac{v_C}{V_B}, \\ V_{gpu} &= \frac{V_g}{V_B}, \quad V_{dcpu} = \frac{V_{dc}}{NV_B}, \quad v_{ppu} = \frac{v_p}{V_B}, \quad i_{Rpu} = \frac{Ni_R}{I_B}. \end{aligned} \quad (5)$$

3.1 Time domain analysis

Figure 3a illustrates ideal waveforms of state variables for steady-state DCM operation of SRC, where $\theta = \omega_0 t$ and β denotes extinction angle of DBR. Considering the half-wave symmetry of tank variables, the analysis is presented for a half cycle of DCM switching period. This half-cycle is further divided into three sub-intervals. Equivalent circuits of each sub-interval are shown in figure 3b–3d.

3.1a Interval-I ($0 \leq \theta \leq \alpha$): This mode begins when the diagonal pair M_1 – M_4 of FB network is turned on. Due to discontinuous nature of the inductor current, i_s , secondary side DBR also turns on at the beginning of this mode. Switching function, S , of DBR is shown in figure 3a. During this interval, tank capacitor voltage, v_C , rises from its initial value V_{C0} and i_s builds up from zero. This ensures ZCS turn-on of FB MOSFETs M_1 and M_4 and secondary diodes D_1 and D_4 . This mode ends when i_s reaches its peak, I_{s1} , and v_C rises to V_{C1} . The normalized state equations for this interval are derived as

$$\frac{d}{d\theta} \begin{bmatrix} i_{spu} \\ v_{cpu} \end{bmatrix} = \begin{bmatrix} -r_{pu} & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_{spu} \\ v_{cpu} \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} V_{gpu} + \begin{bmatrix} -1 \\ 0 \end{bmatrix} V_{dcpu}. \quad (6)$$

The boundary conditions of Interval-I are normalized using respective base quantities and given by

$$i_{spu}(0) = 0, \quad v_{cpu}(0) = V_{C0pu}, \quad (7)$$

$$i_{spu}(\alpha) = I_{s1pu}, \quad v_{cpu}(\alpha) = V_{C1pu}. \quad (8)$$

These mode boundaries are used to solve (6) as follows:

$$I_{s1pu} = -A_1 e^x (p + E) \sin \gamma, \quad (9)$$

Figure 3. (a) Ideal waveforms of SRC operating in DCM. (b) Equivalent circuits during three intervals of DCM: interval-I, (c) interval-II and (d) interval-III.

$$V_{C1pu} = A_1 e^x (\cos \gamma + 2E \sin \gamma) + K. \quad (10)$$

All parameters of (9) and (10) are listed in Appendix I.

3.1b Interval-II ($\alpha \leq \theta \leq \beta$): ZVS turn-on of M_3 and hard turn-off of M_4 define the beginning of this mode. The source V_g remains disconnected, thus forcing i_s to fall. But v_c further rises and reaches V_{C2} at the end of this interval. This mode ends when the DBR ceases to conduct, ensuring ZCS turn-off of diodes D_1 and D_4 . The normalized state equations for this interval are expressed as follows:

$$\frac{d}{d\theta_1} \begin{bmatrix} i_{spu} \\ v_{cpu} \end{bmatrix} = \begin{bmatrix} -r_{pu} & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} i_{spu} \\ v_{cpu} \end{bmatrix} - \begin{bmatrix} 1 \\ 0 \end{bmatrix} V_{dcpu}, \quad \theta_1 = (\theta - \alpha). \quad (11)$$

Noting that i_s becomes zero at the end of this interval, the normalized mode boundaries are presented as

$$i_{spu}(\beta) = 0, \quad v_{cpu}(\beta) = V_{C2pu}. \quad (12)$$

The state equations are solved using (8) and (12) as

$$0 = e^y [I_{s1pu} \cos \delta - F \sin \delta], \quad (13)$$

$$V_{C2pu} = e^y [A_2 \cos \delta + B_2 \sin \delta] - V_{dcpu}. \quad (14)$$

All parameters of (13) and (14) are listed in Appendix I.

3.1c Interval-III ($\beta \leq \theta \leq \pi$): During this mode, the DBR is in off state and thus i_s remains zero. The capacitor holds the charge and v_c remains constant at V_{C2} . ZCS turn-off of M_1 and ZCS turn-on of M_2 define the end of this interval.

Considering the steady state of capacitor voltage, v_c , the following expression is derived:

$$V_{C2pu} = -V_{C0pu}. \quad (15)$$

These simultaneous algebraic mode equations are simplified to derive an expression for V_{dcpu} by eliminating intermediate variables as follows. Noting that $e^y \neq 0$, the expression for I_{s1pu} is derived from (13) as

$$I_{s1pu} = A_2 J, \quad J = \frac{2p^2 + (r_{pu}^2/2)}{2p \cot \delta - r_{pu}}. \quad (16)$$

Equating (9) and (16), V_{C1pu} is simplified as

$$V_{C1pu} = M(K - V_{C0pu}) - V_{dcpu}, \quad M = [e^x (p + E) \sin \gamma] / J. \quad (17)$$

Rearranging (10) and (17),

$$V_{C0pu} = [1 - (1/(M + U))] V_{gpu} - V_{dcpu}, \quad U = e^x [\cos \gamma + 2E \sin \gamma]. \quad (18)$$

Another expression for V_{C0pu} is derived using (14) and (15):

$$V_{C0pu} = [GV_{gpu} - (G + 1)V_{dcpu}] / (G - 1), \quad G = MDe^y, \quad D = \cos \delta + [(J/p) + (r_{pu}/2p)] \sin \delta. \quad (19)$$

Equating (18) and (19), the converter voltage gain, A_{vt} , is expressed as a function of α and β as follows:

$$A_{vf} = \frac{V_{dcpu}}{V_{gpu}} = \frac{1}{2} \left[1 + \frac{G-1}{M+U} \right]. \quad (20)$$

3.2 Frequency domain analysis

Frequency domain analysis of SRC is performed using the multi-order decomposition technique [16]. The large-signal model of the converter is considered as a superposition of n -subsystems. Each of these operates at different steady-state frequencies, as shown in figure 4a. Due to the non-linear nature of DBR, n th order harmonic of i_s generates the following components of rectified current, i_R :

$$i_{spu}^{(n)} S^{(m)} = i_{Rpu}^{(n-m)} + i_{Rpu}^{(n+m)}, \quad (21)$$

where m is the harmonic order of switching function S . It is obvious that $n = m$ constructs the dc component of i_R , $I_R^{(0)}$ and $n \neq m$ results in higher order switching harmonics. Since the converter operates at resonant frequency, the higher order harmonics are adequately attenuated. With this simplified, yet realistic, assumption a reduced order model is realized using $n = m = 1$ and depicted in figure 4b. The fundamental components of tank input voltage v_t and transformer primary voltage v_p are normalized using base voltage V_B and expressed as follows.

$$v_{ipu}^{(1)} = (2V_{gpu}/\pi)[\sin \phi \cos \theta + (1 - \cos \phi) \sin \theta], \quad (22)$$

$$v_{ppu}^{(1)} = (2/\pi)[A_p \cos \theta + B_p \sin \theta], \quad (23)$$

$$A_p = (V_{dcpu} + V_{C0pu}) \sin \beta, \quad (24)$$

$$B_p = V_{dcpu}(1 - \cos \beta) - V_{C0pu}(1 + \cos \beta). \quad (25)$$

Since SRC is switched at resonant frequency, the p.u. fundamental component of i_s is derived as

$$i_{spu}^{(1)} = (v_{ipu}^{(1)} - v_{ppu}^{(1)})/r_{pu}. \quad (26)$$

The fundamental component of S is given by

$$S^{(1)} = (2/\pi)[\sin \beta \cos \theta + (1 - \cos \beta) \sin \theta]. \quad (27)$$

Using (21), (26) and (27), $I_{Rpu}^{(0)}$ is derived as

$$I_{Rpu}^{(0)} = (2/(r_{pu}\pi^2))[V_{gpu}\lambda - 2V_{dcpu}(1 - \cos \beta)], \quad (28)$$

$$\lambda = \cos(\alpha - \beta) - \cos \alpha - \cos \beta + 1.$$

Assuming the double-frequency switching harmonic, $i_{Rpu}^{(2)}$ is completely bypassed through C_f ; the normalized dc bus voltage V_{dcpu} is expressed as

$$V_{dcpu} = I_{Rpu}^{(0)} R_{Lpu}. \quad (29)$$

Rearranging (29), the voltage gain expression (A_{vf}) from frequency domain analysis is derived:

$$A_{vf} = \frac{V_{dcpu}}{V_{gpu}} = \frac{2\lambda R_{Lpu}}{\pi^2 r_{pu} + 4R_{Lpu}(1 - \cos \beta)}. \quad (30)$$

Using (20) and (30), a non-linear algebraic function of β is defined as follows.

$$f(\beta) = A_{vt} - A_{vf}. \quad (31)$$

For a given set of (R_{Lpu}, α) , the root of $f(\beta)$ is numerically determined and A_v is calculated from either (20) or (30).

3.3 CCM–DCM boundary condition

If the capacitor voltage at the end of interval-II ($\theta = \beta$), V_{C2pu} , is greater than V_{dcpu} , DBR remains in on state. Thus, using (15), the CCM–DCM boundary condition is defined as

$$V_{dcpu} = -V_{C0pu}. \quad (32)$$

Rearranging (18) and (32), the boundary condition for continuous and discontinuous modes of operation is expressed as

Figure 4. (a) Large-signal and (b) reduced order model of SRC.

Figure 5. Experimental prototype: (a) top view and (b) bottom view.

$$M + U - 1 = 0. \quad (33)$$

It should be noted that the quantities M and U are functions of α and β . But frequency domain analysis clarifies that β depends on both α and R_{Lpu} . Henceforth, for a given α , derivation of p.u. critical resistance R_{Lcpu} demands one additional design constraint. Equating A_{vt} and A_{vf} at CCM–DCM boundary, the second design constraint is derived as

$$A_{vt} - A_{vf} = 0. \quad (34)$$

Subsequently, two simultaneous non-linear algebraic equations, (33) and (34), are numerically solved using the MATLAB function *fsolve* to determine R_{Lcpu} . This normalized quantity is appropriately scaled by the base impedance to calculate critical load resistance, R_L . Obviously, $R_L < R_{Lc}$ for a given α indicates CCM operation.

4. Results and discussion

An experimental prototype of series resonant dc–dc boost converter is fabricated and shown in figure 5. It comprises FB switches along with the gate drivers, series resonant tank network, HFT, the DBR and output filter capacitor. Analog phase shift controller [17–19] is used to switch the FB MOSFETs. All the parameters of experimental hardware and operating conditions are listed in table 1. Considering these data, β is numerically determined using (31) in MATLAB. The dc bus voltage V_{dc} is calculated from (3) and (30) for CCM and DCM operations, respectively, and detailed in table 2.

CCM SRC is depicted in figure 6a and b, where continuous nature of secondary side current, i_{sec} , is evident. Peak value of tank capacitor voltage, v_C , is greater than the transformer primary voltage, v_p . This ensures that the rectifier diodes remain in on-state for the entire switching cycle, which confirms CCM operation. The spikes in v_t indicate that the leading leg of FB network (M_1 – M_2) does not experience soft turn-on and thus increases voltage stress on switches.

Table 1. System specifications.

L	C	r	L_m
3.84 μ H	165 nF	100 m Ω	700 μ H
f_s	N	C_f	V_{gmin}
200 kHz	20	1 μ F	10 V
V_g	α	R_L (CCM)	R_L (DCM)
20 V	32°	1.4 k Ω	6.4 k Ω

Table 2. Analytical and experimental results.

Results	β (°)	V_{dc} (DCM) (V)	V_{dc} (CCM) (V)	R_{Lc} (k Ω)
Analysis	97	122.5	106.5	4.23
Experiment	92	124	106	4.1

However, DCM operation (figure 6c and d) ensures ZCS turn-on of leading leg MOSFETs, which reduces voltage stress. When the DBR turns off, i_{sec} does not become zero in practice due to the presence of body capacitance across rectifier diodes. The series LC branch resonates with diode capacitances and oscillations are experimentally observed not only in i_s and i_{sec} but also in v_C . Moreover, finite magnetizing inductance (L_m) of HFT acts as a resonating element during DCM operation. This causes slow transition at the edges of v_p during off-state of DBR. Obviously, reflection of capacitor voltage in transformer primary does not appear, as shown in figure 3a. However, the rectifier extinction angle, β , is measured as shown in figure 6c and presented in table 2. Close agreement of experimentally obtained V_{dc} with analytical prediction indicates that the effects of finite L_m and diode body capacitances are negligible.

Figure 7a and b shows tank variables and dc bus voltage when the converter operates at CCM–DCM boundary. It is clear from figure 7a that the peak of v_C just touches the reflected dc bus voltage in transformer primary, which ensures boundary operation. In this condition, the value of R_L is noted and listed in table 2. Close agreement between analytical and experimental R_{Lc} is evident.

Figure 6. Output dc bus voltage and electrical variables of tank network: (a) and (b) CCM operation, (c) and (d) DCM operation. Scale v_t (20 V/div), V_{dc} (50 V/div), i_{sec} —CCM (200 mA/div), DCM (100 mA/div), i_s (2 A/div), v_c (5 V/div), v_p (5 V/div). X-axis (time—1 μ s/div).

Figure 7. CCM–DCM boundary condition—Output dc bus voltage and electrical variables of tank network. Scale v_t (20 V/div), i_s (2 A/div), v_c (5 V/div), v_p (5 V/div), V_{dc} (50 V/div), i_{sec} (100 mA/div). X-axis (time—1 μ s/div).

Figure 8. Analytical and experimental plots of (a) V_{dc} and (b) β at different loads. (c) Plots of e_{vdc} and e_{β} at different loads.

Analytical and experimental values of V_{dc} and β are plotted at different load conditions in figure 8a and b, respectively. The following percentage errors

$$e_{vdc} = \frac{|V_{dc}(\text{analysis}) - V_{dc}(\text{exp})|}{V_{dc}(\text{analysis})} \times 100, \quad (35)$$

$$e_{\beta} = \frac{|e_{\beta}(\text{analysis}) - e_{\beta}(\text{exp})|}{e_{\beta}(\text{analysis})} \times 100, \quad (36)$$

are calculated at different loads and shown in figure 8c. Maximum errors in analytical prediction of V_{dc} and β are observed to be less than 1% and 3.5%, respectively.

5. Conclusion

Time and frequency domain analyses for PM series resonant dc–dc converter operating in DCM are presented. Advantages of operating SRC in DCM are discussed in appropriate detail. Limitations of conventional approaches are noted for DCM analysis. The analysis is described in a normalized form considering ESR in resonant tank. Voltage gain expressions are derived both in time and frequency domain. The rectifier extinction angle is determined by numerically solving a non-linear algebraic equation, which is analytically derived. Derivation of critical load resistance defining the CCM–DCM boundary condition is presented. Analytical predictions for output dc bus voltage and critical load resistance are experimentally validated. This normalized analytical approach provides a definite design guideline for PM SRC operating in DCM.

Appendix I. Parameters of mode equations

$$p = 1 - (r_{pu}^2/4), \quad A_1 = V_{C0pu} - K, \quad K = V_{gpu} - V_{dcpu}$$

$$E = r_{pu}/4p, \quad x = -(r_{pu}\alpha)/2, \quad \gamma = p\alpha$$

$$F = (pA_2 + (B_2r_{pu}/2)), \quad A_2 = V_{C1pu} + V_{dcpu},$$

$$B_2 = (1/p)[I_{s1pu} + (r_{pu}A_2/2)],$$

$$y = r_{pu}(\alpha - \beta)/2, \quad \delta = p(\beta - \alpha).$$

Nomenclature

A_v	voltage conversion ratio of SRC
A_{vC}	A_v during CCM operation of SRC
A_{vt}, A_{vf}	A_v during DCM in time and frequency domain
α, β	phase modulation and DBR extinction angle
θ	phase angle of state variables
S	switching function of DBR
ω_0	tank resonant frequency in rad/s
f_s	converter switching frequency in Hz
L, C	resonant inductor and capacitor
r	effective series resistance (ESR) of tank network
R_L, C_f	load resistance and filter capacitor
R	R_L reflected in transformer primary during CCM
R_{Lc}	critical load resistance for CCM–DCM boundary
v_t, i_s	tank input voltage and current
v_p, v_s	HFT primary and secondary voltages
v_C	voltage across capacitor C
i_{sec}, i_R	HFT secondary and rectified currents
N, L_m	HFT turns ratio and magnetizing inductance
Q_0, Q_r	quality factor due to R_L and r
V_g, V_{dc}	input and output dc voltages
Z_B, V_B	base impedance and voltage for normalization
I_B, V_{gmin}	base current and minimum input voltage
n, m	harmonic order of i_s and S
e_{vdc}, e_{β}	p.u. errors in V_{dc} and β

References

- [1] Bhardwaj S, Borage M and Tiwari S 2008 Simplified loss analysis and comparison of full-bridge, full-range-ZVS DC–DC converters. *Acad. Proc. Eng. Sci. Sadhana* 33(5): 481–504
- [2] Yang J and Do H 2013 Analysis and design of a high-efficiency zero-voltage-switching step-up DC–DC converter. *Acad. Proc. Eng. Sci. Sadhana* 38(4): 653–665
- [3] Lakshminarasamma N, Ramanarayanan V and Sidharthan P 2008 A new family of soft transition converters: design and dynamic model. *Acad. Proc. Eng. Sci. Sadhana* 33(5): 459–479

- [4] Kundu U, Yenduri K and Sensarma P 2016 Accurate ZVS analysis for magnetic design and efficiency improvement of full bridge LLC resonant converter. *IEEE Trans. Power Electron.* 32(3): 1703–1706
- [5] Gayathri N and Chandorkar M C 2008 Design and implementation of FPGA-based phase modulation control for series resonant inverters. *Acad. Proc. Eng. Sci. Sadhana* 33(5): 505–522
- [6] Prieto-Araujo E, Fekri-Fekriasi S and Gomis-Bellmunt O 2015 Control and experimental validation of a dual active bridge series resonant converter. In: *Proceedings of the IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, pp. 1–8
- [7] Chansri P, Noicharoen N and Phetphoi K 2011 A high power LED driver with Class D ZVS series resonant converter. In: *Proceedings of the IEEE International Conference on Electrical, Control and Computer Engineering (INECCE)*, pp. 457–460
- [8] Kline M, Izyumin I, Boser B and Sanders S 2011 Capacitive power transfer for contactless charging. In: *Proceedings of the IEEE Applied Power Electronics Conference (APEC)*, pp. 1398–1404
- [9] Vandelac J P and Ziogas P D 1988 A DC to DC PWM series resonant converter operated at resonant frequency. *IEEE Trans. Ind. Electron.* 35(3): 451–460
- [10] Erickson R W and Maksimovic D 2000 Resonant conversion. In: *Fundamentals of Power Electronics*, 2nd edn. India: Springer International Edition (Chapter 19)
- [11] Ayachit A, Murthy-Bellur D and Kazimierczuk M K 2012 Steady-state analysis of series resonant converter using extended describing function method. In: *Proceedings of the IEEE International Midwest Symposium on Circuits and Systems (MWSCAS)*, pp. 1160–1163
- [12] Shuilin T, Lee F C and Qiang L 2016 A simplified equivalent circuit model of series resonant converter. *IEEE Trans. Power Electron.* 31(5): 3922–3931
- [13] Safaee A, Jain P and Bakhshai A 2014 Time-domain steady-state analysis of fixed-frequency series resonant converters with phase-shift modulation. In: *Proceedings of the IEEE Transportation Electrification Conference and Exposition (ITEC)*, pp. 1–7
- [14] Aboushady A A, Ahmed K H, Finney S J and Williams B W 2010 Steady-state analysis of full-bridge series resonant converter with phase-shift and frequency control. In: *Proceedings of the IET International Conference on Power Electronics, Machines and Drives (PEMD)*, pp. 1–6
- [15] Singh Y V, Viswanathan K, Naik R, Sabate J A and Lai R 2013 Analysis and control of phase-shifted series resonant converter operating in discontinuous mode. In: *Proceedings of the IEEE Applied Power Electronics Conference*, pp. 2092–2097
- [16] Chaudhary P and Sensarma P 2013 Front-end buck rectifier with reduced filter size and single-loop control. *IEEE Trans. Ind. Electron.* 60(10): 4359–4368
- [17] Kundu U, Chakraborty S and Sensarma P 2015 Automatic resonant frequency tracking in parallel LLC boost DC–DC converter. *IEEE Trans. Power Electron.* 30(7): 3925–3933
- [18] Kundu U and Sensarma P 2016 Gain-relationship-based automatic resonant frequency tracking in parallel LLC converter. *IEEE Trans. Ind. Electron.* 63(2): 874–883
- [19] Kundu U, Chakraborty S and Sensarma P 2013 Analog controller for MPPT and self-tuning of resonant frequency in parallel LLC boost DC–DC converter for PV microinverter. In: *Proceedings of the National Power Electronics Conference (NPEC)*, Kanpur, India