PI controller scheme for charge balance in implantable electrical stimulators

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MS received 2 March 2015; revised 24 September 2015; accepted 23 October 2015

Abstract. Electrical stimulation has been used in a wide variety of medical implant applications. In all of these applications, due to safety concerns, maintaining charge balance becomes a critically important issue that needs to be addressed at the design stage. It is important that charge balancing schemes be robust to circuit (process) and load impedance variations, and at the same time must also lend themselves to miniaturization. In this communication, simulation studies on the effectiveness of using Proportional Integral (P-I) control schemes for managing charge balance in electrical stimulation are presented. The adaptation of the P-I control scheme to implant circuits leads to two possible circuit realizations in the analog domain. The governing equations for these realizations are approximated to simple linear equations. Considering typical circuit and tissue parameter values and their expected uncertainties, Matlab as well as circuit simulations have been carried out. Simulation results presented indicate that the tissue voltages settle to well below 20% of the safe levels and within about 20 stimulations cycles, thus confirming the validity and robustness of the proposed schemes.

Keywords. Neural stimulation; biomedical implant; charge balance.

1. Introduction

In the recent past, implantable circuit stimulators have started proliferating due to advances in miniaturization. Some of the applications which use stimulators include Cochlear, Retinal, Vestibular and Bladder control implants [1–4]. The key design issues that are traditionally addressed include low power consumption, high voltage compliance, immunity to time varying tissue impedance/process variations and reliability. Apart from addressing the primary design goals, stimulation circuits must address all issues related to electrical safety. Though the importance of this issue is well known, it has not been the focus of study in many papers that deal with the design of implant electronics. The present paper addresses the safety issue associated with charge balance in stimulator. The commonly used biphasic stimulation is typically realized by connecting a current sink and source alternately to the tissue for stipulated time. The current pulse parameters like anodic and cathodic pulse widths, their separation, amplitudes and repetition period are dependent on the specific application. In the case of cochlear implants for example, the charge delivered/retrieved in the cathodic/anodic phase is of the order of a few nanocoulombs. In practice, due to process and load variations, a mismatch of the order of 2–5% is encountered between the current amplitudes of the cathodic and anodic phases, leading to charge imbalance in the tissue. However, from biological

safety considerations, it is necessary that the ‘Charge Balance’ condition be maintained which implies that the charge accumulation over a period of time is not permitted.

The issue of charge balance has been conventionally addressed by using a blocking capacitor [5]. With typical values in the order of a few hundred nano Farads, its on-chip realization poses difficulties. Another effective method is to discharge the electrodes [6] by periodically shorting them for a sufficient time (a few milliseconds). This, however, restricts the stimulation rate in applications like cochlear implants. Hence, alternative circuit techniques for charge balancing have been gaining importance. The existing schemes for charge balancing can be classified as either open loop or closed-loop charge balancing schemes. The open loop schemes rely on matching the currents delivered to the load in the cathodic and anodic phases. The current calibration technique [7], the dynamic copier scheme [1], and the charge metering scheme [8] are some examples of open loop charge balancing technique. However, load variations and leakage contribute to a residual charge imbalance in these schemes.

In closed-loop charge balancing schemes, the residual voltage is sensed at the end of each stimulation phase, and used to correct the charge delivered in the subsequent stimulation cycle. Instead of ensuring charge balance within every cycle, it can now be achieved progressively across a few cycles, in different ways. For example, in [9], charge balancing is achieved by inserting a multitude of compensating small amplitude spikes after each biphasic pulse. However,

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the stimulation profile now gets altered, and as noted in [10], it remains to be further investigated to rule out the possibility of invoking unwanted neural responses. As the amplitudes of the correcting spikes ought to be small, there will be limitations on the achievable correction and the stimulation rate. Another approach, the offset regulation scheme [2], monitors the residual voltage and uses a discrete set of current sources to incrementally change the anodic phase of the subsequent stimulation. A digital control unit is used to compute the offset. The accuracy of correction is limited by the number of current sources available and as noted in [10], this offset scheme may not be very effective since correction is a continuous background process.

A more general closed-loop feedback approach of employing P-I controllers [10, 11] has been proposed in recent literature. In [10], the amplitude of the compensating anodic phase current is determined from a P-I model of the feedback system. The feedback path included a 3-level comparator and an FIR filter, and the scheme was validated in simulation by studying the step responses of the system. In a similar scheme in [11], a P-I controller was used for charge cancellation by controlling the time duration of the compensation pulse. The underlying system equations are nonlinear, but this aspect is not elaborated upon by the authors. While both these works [10] and [11] establish that P-I control scheme can be effective in restoring charge balance, circuit realization is not carried out. Also the functional blocks are in the digital domain, assuming the availability of onchip Digital Signal Processing capabilities. Alternate to having complex digital processing capability, it would be appropriate to implement them in the analog domain. An analog implementation of the P-I controller based charge balance scheme in nerve cuff stimulators is reported in [12]. However the design reported is carried out using discrete 'commercial off the shelf' components. Moreover, the stimulation parameters (current amplitude and stimulation period) as well as the capacitor values considered are much more relaxed than those considered in [10] and [11].

The present work discusses robust closed loop analog realisations based on P-I controllers that are completely integrable onto a chip. Starting from the work reported in [10] and [11], the present work further explores the use of P-I control schemes to address charge balance issues, and proposes alternate analog domain realizations. Two possible methods have been considered for charge correction that can be applied during the subsequent anodic phase. These include the modification of either the amplitude, or the duration of the anodic current. These proposed schemes are carried out in the analog domain in such a way that digital processing is not required and hence can be easily incorporated into chip realization of the standalone stimulation driver circuitry. The governing system equations of the proposed realizations are linearized wherever required by considering valid approximations. Matlab and circuit level simulation results are presented to demonstrate the effectiveness of the proposed P-I schemes.

The rest of this communication is organized as follows: Section 2 explains the proposed charge balance method along with the analysis carried out for the closed-loop P-I system. The possible circuit realization of the proposed methods is discussed in Section 3. The results obtained through block level and circuit level simulations are presented, followed by the conclusions of the present work in Section 4.

2. Closed-loop charge balance scheme

The internal unit of a typical implant comprises subsystems like the power and data / clock recovery unit, stimulus data generation unit, stimulation and the back telemetry unit [13]. The subsystems are predominantly analog with the exception of the stimulus generator unit, which operates on the data stream retrieved by the data recovery unit to provide the details required for stimulation [14]. This information typically comprises the pulse profile data and 5–9 bit of current amplitude data [15]. In every cycle, the current amplitude required for stimulation is supplied from the current mode DAC, based on this amplitude data. It should be noted that the DAC inputs are externally obtained quantized value of stimulus signals and the PI controller mechanism continues to have analog values unlike [11] and [10]. The current from the DAC is mirrored for the cathodic and anodic phases by switching the current sink and source in succession in the typical CMOS stimulation driver, shown in figure 1. The recovered clock, which is in the range of 1–20MHz, and the pulse profile data are used to derive the various timing signals.

The equivalent circuit parameters that model the tissue are shown in figure 1 and they include the solution resistance R , Faradic resistance R_f and the double layer capacitance C . In monopolar stimulation, one of the electrodes, namely the reference electrode, is maintained at the reference voltage, V_{ref} which is typically at the mid rail. As shown in the typical stimulation timing sequence in figure 2, the biphasic pulse repeats periodically with a period t_{st} . Cathodic and anodic pulses are of durations t_c and t_a respectively with an inter pulse interval t_i . The corresponding voltage developed across the tissue due to this biphasic current is also shown.

2.1 Analysis

The residual output voltage of the tissue is measured and compared against a reference voltage to determine the error signal. The control signal is then arrived at after passing the error signal through appropriate proportional and integral paths. The resulting control voltage can change any of the anodic pulse parameters, i.e., amplitude or duration in the subsequent cycle.

The appropriate discrete time closed loop model of the implant with the sampling done at the end of the stimulation cycle has been worked out for the present scheme and is presented in figure 3. The driver block delivers the cathodic

Figure 1. Typical stimulation driver circuit.

current $I_c[n]$ every cycle, and is considered as the external input to the system. Although the anodic current ideally is expected to be the same as the cathodic current, in practice it differs and is considered to be $I_c[n] \cdot (1 - M)$, where M represents the mismatch between them. The residual output

voltage at the tissue $V_o[n]$ measured at the end of the n^{th} stimulation cycle is determined by three components, namely the cathodic current, anodic current and the charge leakage. The blocks labeled Cathodic/Anodic Stimulation represent the contributions of the cathodic and anodic currents

Figure 2. Typical biphasic current pulse and the voltage developed across the tissue.

Figure 3. Block diagram of a discrete time closed-loop system with anodic current control.

respectively to the tissue voltage measured at the end of the n^{th} stimulation period. The corresponding gains of these blocks are denoted by G_c and G_a respectively. $V_o[n]$ also has a component that is related to the natural decay through the tissue of the voltages measured in the previous cycle. The Charge Leakage block in figure 3, represents this contribution $V_d[n]$ and has a gain G_d .

Following a procedure similar to the one used in [11], the tissue voltage $V_o[n]$, in the absence of feedback, is given as a superposition of these three components.

$$V_o[n] = V_c[n] + V_a[n] + V_d[n]. \quad (1)$$

with

$$\begin{aligned} V_c[n] &= -I_c[n] \cdot R_f \cdot (1 - e^{-t_c/(R_f \cdot C)}) \\ &\quad \cdot e^{-(t_{st}-t_c)/(R_f \cdot C)} \\ &= G_c \cdot I_c[n]. \\ V_a[n] &= I_c[n] \cdot (1 - M) \cdot R_f \cdot (1 - e^{-t_a/(R_f \cdot C)}) \\ &\quad \cdot e^{-(t_{st}-t_c-t_a-t_i)/(R_f \cdot C)} \\ &= G_a \cdot (1 - M) \cdot I_c[n]. \\ V_d[n] &= V_o[n-1] \cdot e^{-t_{st}/(R_f \cdot C)} \\ &= G_d \cdot V_o[n-1]. \end{aligned}$$

where $V_c[n]$ and $V_a[n]$ are respectively the voltage contributions at the output due to the cathodic and anodic stimulation blocks. It should be noted that during the sampling instant, there is no current stimuli and hence there will be no drop across R . The sampled output voltage $V_o[n]$ and its various components are hence independent of R . The above equation is adequate to account for the open loop operation of the typical biphasic system.

The operation of the closed loop system is considered next. The proportional and integral paths are represented by

the P-I block, and has a gain denoted by G_{PI} . The feedback correction signal can be subsequently generated either as a current or a time duration signal and the schemes are hereafter referred to as amplitude control scheme, and duration control scheme respectively. Either of these cases are modeled by a single block in figure 3 with a conversion gain G_X . The motivation for using both the schemes is only to establish charge balance with either of them and realize the circuits in analog domain. Depending on the application, there can be restriction in the maximum value of either current or duration and the appropriate scheme can be chosen. Both the schemes are analysed to decide on the optimum method. However, the governing system equations of the anodic phase are different for the two cases, and hence have to be analyzed separately. When the smallest resolution in correction is considered, Amplitude control scheme has continuum of current levels for correction (ΔI) an inherent advantage compared to some previous works [16] which have limited current correction levels. Duration control scheme is bound to have adequate accuracy as the time resolution is decided by the system clock, which is typically a few MHz for a typical implant.

When the schemes are observed from the view of the largest correction value attainable, the schemes will not be limited by large correction value as the integrator provides adequate damping.

2.1a Amplitude control scheme: In this method, the G_X block (of figure 3) would correspond to a voltage to current converter, denoted by G_i and provides the correction current that needs to be added along with the anodic current.

The block diagram of the charge balance system with current amplitude being used to correct the net charge level is presented in figure 4. As the amplitude correction has to be done in a time period t_a and it should be of magnitude such

Figure 4. Block diagram of an amplitude control scheme.

that it removes the net error voltage given by V_{PI} , due to the charge accumulated across C , it can be shown that

$$G_x = G_i = \frac{C}{t_a}.$$

The P-I controller is characterized by the proportional and integral path gains K_p and K_i respectively and its transfer function G_{PI} is given by

$$G_{PI} = K_p + K_i \frac{z}{z-1}.$$

With reference to figure 4, the output voltage can now be expressed in the z transform domain as

$$V_o(z) = I_c(z) \cdot [G_c + H_a] + V_o(z) \cdot z^{-1} G_d - V_o(z) \cdot z^{-1} \cdot G_{PI} \cdot G_i \cdot G_a.$$

where $H_a = (1-M) \cdot G_a$.

The transfer function of the closed loop system can then be expressed as

$$H(z) = \frac{V_o(z)}{I_c(z)} = \frac{G_c + H_a}{1 - z^{-1} \cdot G_d + z^{-1} \cdot G_i \cdot G_{PI} \cdot G_a}. \quad (2)$$

2.1b Duration control scheme: In this method, the G_x block (of figure 3) would correspond to a voltage to time converter of gain G_t and provides the correction time (Δt) for which the anodic phase current should be supplied. The block diagram for the charge balance system with anodic duration being used to correct the charge is presented in figure 5.

It may be noted that the anodic current is maintained at $I_c \cdot (1-M)$. From the output of the P-I controller

$V_{PI}[n]$, the G_t block computes Δt and the gain is given by

$$G_x = G_t = \frac{C}{I_c \cdot (1-M)}.$$

The voltage at the end of the stimulation period due to the anodic current is given by

$$V_a[n] = I_c[n] \cdot (1-M) \cdot R_f \cdot \left(1 - e^{-(t_c + \Delta t)/(R_f \cdot C)} \right) \cdot e^{-(t_{st} - t_i - 2t_c - \Delta t)/R_f \cdot C}.$$

The anodic stimulation block can now be thought of as having two inputs $I_c[n]$ and Δt , the latter again is a function of $I_c[n]$ and $V_o[n-1]$. The above equation can then be simplified by considering the first two terms of Taylor's series approximation for the exponential $e^{(t_c + \Delta t)/(R_f \cdot C)}$ and is written as

$$V_a[n] = I_c[n] \cdot (1-M) \cdot R_f \left(\frac{t_c}{R_f \cdot C} + \frac{\Delta t}{R_f \cdot C} \right) D'.$$

where $D' = D \cdot e^{\Delta t/(R_f \cdot C)}$ with D being a constant equal to $e^{-(t_{st} - t_i - 2t_c)/(R_f \cdot C)}$. The term D' is relatively insignificant as it represents the marginal reduction in charge leakage due to Δt . Assuming Δt to be small when compared to the nominal stimulation period, the exponential term $e^{\Delta t/(R_f \cdot C)}$ always turns out to be close to unity and can be treated as a constant.

$$V_a[n] = \left(\frac{I_c[n] (1-M) t_c}{C} + V_{PI}[n] \right) D'.$$

The anodic phase component of the residual output voltage is given by

$$V_a[n] = I_c[n] (1-M) \cdot \left(\frac{t_c}{C} + \frac{\Delta t}{C} \right) D'. \quad (3)$$

Figure 5. Block diagram of a duration control scheme.

$$= \left(\frac{I_c[n](1-M)t_c}{C} + V_{PI}[n] \right) D'. \quad (4)$$

$V_{PI}[n]$ is derived from $V_o[n-1]$ when $V_{ref} = 0$, as

$$V_{PI}[n] = -K_p \cdot V_o[n-1] - K_i \cdot V_o[n-1] + V_{PI}[n-1].$$

The above equation can be written in z domain as

$$V_{PI}[z] = -z^{-1} \cdot G_{PI} \cdot V_o[z] \text{ with } G_{PI} = K_p + \frac{K_i \cdot z}{z-1}.$$

The residual output voltage $V_o[z]$ is given by

$$V_o[z] = I_c(z) \cdot G_c + \frac{I_c(z) \cdot (1-M) \cdot t_c}{C} \cdot D' - z^{-1} \cdot G_{PI} \cdot V_o[z] \cdot D' + z^{-1} \cdot V_o[z] \cdot G_d.$$

The transfer function of the closed loop system can then be expressed as

$$H(z) = \frac{V_o(z)}{I_c(z)} = \frac{G_c + (1-M) \cdot D' \cdot t_c / C}{1 - z^{-1} \cdot G_d + z^{-1} \cdot G_{PI} \cdot D'}. \quad (5)$$

Figure 6. Amplitude control based P-I scheme.

From the mathematical analysis carried out it can be concluded that the duration control approximation holds good for application with longer stimulation period t_{st} . Both the solutions are explored further with circuit realisation, as the circuit topology could pose additional limitation on the charge balance accuracy.

3. Circuit realization

The circuit details of the two charge balancing schemes are discussed along with the corresponding timing waveforms.

3.1 Amplitude control scheme

The circuit details of the amplitude control scheme are given in figure 6. The currents for the cathodic and anodic phases are mirrored from a single Digital to Analog Converter (DAC) using M1 and M4 respectively. The feedback path comprising the P-I controller and G_i block will provide the additional current ΔI (obtained as I_{out} in figure 7) in the anodic phase. The incremental current is added to the original anodic current from transistor M4. The tissue

is maintained at midrail V_{ref} . The voltages V_{b2} and V_{b3} are used to provide the biasing for the cascode transistors M6 and M7.

P-I controller and G_i blocks of figure 6 are implemented as shown in figure 7. V_{b1} provides the bias for the transistor M24 which produces the tail current for the differential pair M21-M22. The sampling of the output voltage is carried out during ϕ_1 at the end of the stimulation period. There are two parallel paths namely the proportional path and the integral path. The values of the circuit elements are chosen as follows from the block parameters of the described models.

$$R1 = R2 = \frac{1}{G_i}$$

$$g_{m21} = g_{m22} = K_p \cdot G_i.$$

With the value of $C1$ chosen to aid ease of integration,

$$C2 = \frac{C1}{K_i}. \quad (6)$$

For the proportional path, the residual voltage V_o is sampled by the capacitor C_3 during ϕ_1 . The folded cascode amplifier is designed to have a transconductance that is equal to

Figure 7. P-I controller block realization.

Figure 8. Timing waveforms for the amplitude control scheme.

the product of K_p and G_i . The current output from this amplifier forms the proportional part of I_{out} and adds at the source of the transistor M34. The integral path comprises a switched capacitor integrator (OPAMP OA1, C_1 , C_2) followed by voltage to current conversion (OPAMP OA2, M35, R_1). For the integral path, the output voltage is sampled to C_1 whose other end is maintained at V_{ref} during the phase ϕ_1 . The switched capacitor integrator implements the integral path gain K_i as $\frac{C_1}{C_2}$. The capacitor is discharged during the reset phase ϕ_r . OPAMP OA2 and R_1 implement the G_i block of figure 4. During the post sampling phase ϕ_2 , the integrator output voltage is converted to current by a factor $\frac{1}{R_1}$. The current from this integral path is added to the proportional path current to provide the output current I_{out} of this P-I block.

The anodic and cathodic phases are enabled by signals ϕ_p and ϕ_n respectively. The timing details of the amplitude control scheme is given in figure 8. The correction with additional current ΔI is carried out from the second cycle onwards and this timing is represented by the signal ϕ_2 . The system reset is carried out during ϕ_r .

3.2 Duration control scheme

The circuit details of the duration control scheme are given in figure 9. The currents for the cathodic and anodic phases are obtained from a Digital to Analog Converter (DAC) using the current sink M1 and source M4 respectively. The feedback path comprising the P-I controller and G_t block (of figure 5) will decide the extended time for the anodic phase Δt .

To compute this additional time, the timing decision block uses the voltages across the capacitor C_r and V_{PI} , the P-I controller output voltage. The voltage V_{PI} is the voltage

developed across the resistor R_2 by the current I_{out} of P-I block. The circuit of the P-I controller in figure 7 is used to implement the P-I block but the proportional path gain now equals product of K_p and R_2/R_1 . The integral path gain now equals product of K_i and R_2/R_1 .

The circuit realization of the voltage to time conversion G_t block (figure 5) is detailed in figure 10. The voltage to time conversion is initiated by the signal ϕ_{pe} at the end of nominal anodic pulse duration (represented by ϕ_{pi}). A scaled version of the anodic current is mirrored and fed to a timing capacitor, C_r . The voltage across this capacitor is compared against the control voltage derived from the P-I controller V_{PI} . The simple logic ensures that the anodic phase duration is the sum of the ϕ_{pi} and the comparator output during the phase ϕ_{pe} . When the voltage across the capacitor C_r increases beyond V_{PI} , the comparator output switches state and the output of the logic gates ϕ_p goes low. Hence the unit dynamically decides the actual duration of the current anodic phase ϕ_p .

The timing details of the duration control scheme is given in figure 11. The sampling of the residual output voltage is done at the end of the stimulation cycle and this is represented as ϕ_1 . The feedback loop is closed from the second cycle onwards represented by ϕ_2 . This phase duration is equal to the maximum possible anodic duration and throughout this period V_{PI} is available. The anodic phase ϕ_p comprises two parts, namely the fixed initial part ϕ_{pi} and a varying time component Δt decided in the phase ϕ_{pe} , the ending part of the anodic phase. The cathodic phase is enabled by ϕ_n and the system is reset during ϕ_r .

But in the present circuit realization, the comparator offset voltage limits the accuracy. Additionally the sensitivity of the timing capacitor to the tissue variations lowers the net accuracy. It is concluded that though both the schemes

Figure 9. Duration control based P-I scheme.

are equally efficient in the analysis phase and the amplitude control scheme has better performance in the present circuit realization.

3.3 Results

This section first presents the closed form expressions obtained after plugging in nominal values applicable to

Cochlear implants. Matlab simulations of the proposed system are carried out, and from the results, the optimum value for the block parameters is arrived. Circuit simulation results are then presented for the two alternative realizations proposed. Finally the work is compared with similar schemes reported in the literature.

The actual values for the tissue parameters could vary between users and also over a period of time. The solution

Figure 10. Duration control based P-I scheme- timing decision block.

Figure 11. Timing waveforms of duration control based P-I scheme.

resistance R can be from a few hundred ohms to 20 kilo ohms. The test cases considered the mismatch parameter M to be in the range 0.05 and 0.15, the range being larger than the expected process mismatch between the anodic and cathodic phase current amplitudes. The specifications and values of the pulse profile used in the simulation are given in table 1. The values of the various components used are summarized in table 2.

Using the information available from the earlier literature [10, 11] reporting on charge balancing circuits across stimulation cycles as a guideline, the target specifications are arrived at. From the perspective of well controlled safe stimulation, the settling time is defined as the time required for the step response to change from its initial state and remain within 20% of its safe zone limit i.e. 20mV and this is targeted as 25 cycles. It is concluded that the system is to restrict the overshoot to no higher than 20% of the safe zone. The settling time and overshoot could vary depending on the application and acceptable ranges are based on insitu measurements. However, the design methodology will remain by and large the same irrespective of the values chosen.

Table 1. Typical values used for specification and pulse profile.

Specifications		Miscellaneous values		Pulse profile	
Settling time	25 cycles	V_{ref}	2.5 V	t_c	30 us
Over shoot	20%	V_{dd}	5 V	t_a	30 us
I_c	20 uA to 1 mA	V_{b1}	3.84 V	t_i	20 us
Mismatch	$\pm 15\%$	V_{b2}	3.44 V	t_{st}	550 us
V_o variation	< 100 mV	V_{b3}	1.5 V		

Table 2. Values for the various components used.

R	500 Ω
R_f	1 M Ω
C	10–100 nF
R_1	300 Ω
C_1	350 fF
C_2	10 pF
C_3	1 pF
C_r	10 nF

Optimization of the block parameters: The system was modeled using Matlab with the actual values plugged into Eq. (2) and Eq. (5). The system is analyzed for different proportional and integral path gains. Initially a closed loop system is considered, with the gain block alone and the results are shown in figure 12. As the gain is increased the steady state error is decreased as shown in the figure. But after a point ($K_p = 1.046$), the increase in gain results in unstable behavior. Hence it is concluded that without the integral block, there will be some pronounced error.

Next the system is observed with an optimum value of K_p as 0.24 and for various integral gains. The results are summarized in figure 13. Very low values of the integral constant is not preferred as it takes time to converge at the desired value. Very large values of K_i are again not preferred. Tuning of the system parameters is done using Matlab.

It can be seen from the graph of figure 14, that a trade-off exists amongst the overshoot, settling time, steady state output error and values of K_p and K_i . The plot corresponding to K_p of 0.27 and K_i of 0.037 keeps the parameters overshoot, settling time and steady state output error within the

Figure 12. Variation of the tissue voltage with time for various K_p with $K_i = 0$.

requirements of the application and hence are chosen in circuit realization. With these K_p and K_i values plugged in, the transfer function from Eq. (2) reduces to

$$\frac{V_o(z)}{Ic(z)} = \frac{-16.1 \cdot z \cdot (z - 1)}{(z^2 - 1.69z + 0.72)} \text{ in ohms.} \quad (7)$$

The corresponding step response of such a system is given as

$$V_o[n] = -124.76 \cdot (0.85)^n \cos(-1.44 + 0.13 \cdot n) \text{ in volts.} \quad (8)$$

In Eq. (2), after setting $K_i = 0$, the transfer function is solved for maximum K_p for which the poles are inside the unit circle. It is found to have a pronounced steady state output value, $V_o(\infty)$ as seen in figure 12 and hence inclusion of integral path is essential.

Analysis of system flexibility: Even with variation in tissue impedance, the value of the faradic resistance R_f is always above $1\text{M}\Omega$ [1]. Any variation does not impact

Figure 13. Variation of the tissue voltage for various K_i , with K_p held constant at 0.24.

Figure 14. Output voltage for various K_p and K_i values.

the performance as shown in figure 15 and can be safely neglected. The present system is independent of the tissue resistance R , as this does not feature in the system equations. The double layer capacitance C is varied and the system performance is summarized in figure 16 for the chosen values of PI controller gains K_p and K_i . It should be noted that the values of the PI controller gains have to be adjusted with the initial estimate in the double layer capacitance.

Initially the performance of the system was analyzed for various extent of mismatch. Considering the variation of M alone, it can be seen from figure 17 that the system is quite robust for values of M below 0.15. Beyond this, the overshoot exceeds the safety range of 100 mV and would be barely acceptable. Accommodating this much mismatch may be too conservative and may not be called for in practice. However even for accommodating this, some degree of freedom exists in terms of varying the quantities K_p and K_i . The modeled system can control the bidirectional deviation of V_o from its reference value, as shown in figure 17 for

Figure 15. Output voltage of amplitude control scheme for different values of Faradic resistance values.

Figure 16. Output voltage of amplitude control scheme for different values of double layer capacitance values.

a duration control scheme. Both the amplitude control and the duration control schemes can respond and correct bipolar excursions in tissue voltage. To enable this in either case, the corresponding nominal anodic currents are a priori set lower than the corresponding cathodic currents by predetermined amounts by appropriately sizing the transistor M4 in figure 6 and figure 9. This in turn permits one to use unidirectional correction signals (either ΔI or Δt) to restore loop balance.

The duration control scheme is further investigated by simulating the system using Matlab for different values of ratio C_r/C . As can be seen from figure 18, the system converges to V_{ref} for different values of C_r/C . Hence there is a flexibility in the choice of the value of the timing capacitance for an acceptable performance. The above results were for a step input of 1 mA current amplitude. In reality the amplitude will be varying with every stimulation cycle and hence

Figure 17. Output voltage of the tissue for various values of mismatch factor M .

Figure 18. Sensitivity of the timing capacitor.

Figure 19. Response to different excitation current distributions.

Figure 20. Sampled values of the tissue voltage with 1 mA step current input.

the system is simulated for different distributions of current and their time response is shown in figure 19.

Apart from unit step input for current, simulations were also performed for input current amplitude values drawn

Figure 21. Sampled tissue voltage of amplitude control scheme with variation in double layer capacitance.

from a normal distribution of 1 mA rms. This latter excitation would correspond more closely to the realistic situation where the successive input current samples may not be correlated. For this case also, it was confirmed from figure 19 that the output variations were well within 100 mV safety

window. The blue trace corresponds to an unit step current of 1 mA, while the red and the black traces represent the currents of uniform and Gaussian distributions respectively.

Circuit simulation and transient results: The W/L values of the transistors in figures 6–9 are arrived at using the 1 μ m CMOS GPDK libraries and the simulation was performed using Cadence Spectre. In figure 7, the folded cascode transconductor has a transconductance of 0.9 mS. This provides the functionality of both proportional path of gain 0.27 and the G_x block gain of 3.33 mS (of figure 3). The ratio of the capacitances C_1 and C_2 was chosen to implement an integral path gain of 0.037. The V to I converter following the switched capacitor integrator has a linear range of 890 mV and has a transconductance of 3.33 mS.

Figure 20 gives the plot of the sampled version of the transient response of the realized circuit for a step input of 1 mA amplitude. The output voltage transient waveform samples for the circuits in figure 6 and figure 9 are plotted on the same figure. It may be seen that the circuit simulation results for both cases closely agree with those predicted using Matlab simulations and settle to well below 20% of the acceptable safety voltage range of 100 mV at nearly 20th sample (11 ms) which complies with the target specifications.

Figure 22. Amplitude control scheme (a) transient output of the current waveforms; (b) variation of the incremental current with stimulation cycles.

The double layer capacitance of the tissue is varied for an amplitude control scheme and simulations were carried out. The sampled values of the tissue output voltage are plotted in figure 21.

The gain parameters of the PI controller block were maintained at the same value. The transconductance of transistor $M_{21,22}$ and resistance R1 were changed correspondingly. The current values were reduced to 0.5 mA to accommodate the rail as there will be more voltage variation with the smaller values of the double layer capacitance for the same values of mismatch (15%). It should be noted that the transient specifications will be modified from that stated in table 1, for smaller values of double layer capacitances.

The transient waveform of the biphasic pulse current flowing through the tissue in an amplitude control scheme is given in figure 22a. It is noted that there is an incremental current in each stimulation cycle over the nominal current. The maximum current in a phase cannot exceed the stimulation current range for the considered application. From figure 22b, it can be observed that the incremental current variation did not pose a problem for the extent of mismatches considered and anodic current was contained to 1.04 mA.

The transient waveform of the timing signals in a duration control scheme is given in figure 23a. The voltages V_{PI} and the voltage across the timing capacitor C_r are given in figure 23b.

It should be noted that when the two voltages cross each other there is a corresponding shift in the level of the signal ϕ_p in figure 23a. The incremental time more than the nominal anodic pulse duration for which anodic current flows is plotted against the stimulation cycles in figure 23c and the maximum value was found to be less than 10 μ s for the stimulation levels used.

Comparison: The various charge balancing schemes reported in literature have addressed different specifications of charge levels, stimulation rate and tissue parameters, and hence a fair comparison is difficult. As charge balancing by dynamic current copier [1] is an open loop scheme, the system critically depends on the matching of the cathodic and anodic currents and the residual voltage was reduced to 12 mV. But as it is an open loop scheme, in the presence of any non-ideality the residual voltage can grow out of the safe voltage range. In an earlier work [2] employing feedback using an integrator, the time constant of the integrator had to be chosen iteratively to reduce the overshoot. Another approach namely offset regulation scheme [16] depends on the availability of a digital processor for the computation of the control signal and the compensating current assumes only a few discrete values. The schemes reported in [2] and [16] both aim at bringing the voltage to within the acceptable range ± 100 mV. Two recent papers [10, 11] propose

Figure 23. The transient waveforms showing the comparator switching (a) the timing waveforms; (b) the input waveforms to the comparator; (c) the variation of the incremental time with the stimulation cycles.

the use of P-I controller for charge balancing, but have suggested digital realization of control blocks, and hence need to consider the impact of quantization. In the present work, two possible alternate analog realizations of P-I controller are presented with both exhibiting very small steady state error of 10 mV. The analog realizations are found to settle to well below 20% of the acceptable voltage range within a few stimulation cycles (20th cycle or 11 ms) which satisfies the desired requirements.

4. Conclusion

Analog realization of two alternate P-I based charge balancing schemes was presented. Although device fabrication and experimental validation have not been carried out, the objective of the present work is only to establish the feasibility of analog domain P-I based charge balance schemes. In this work, it is demonstrated that the two investigated versions are very efficient in converging the tissue to the nominal reference potential irrespective of the source of the charge accumulation. It is also shown that the proposed scheme is quite tolerant to current mismatch and P-I controller values. As the implementation is carried out in CMOS circuits in analog domain, this permits seamless integration of the circuits into the stimulator electronics which is predominantly analog. As the monitoring is continuous, blocking capacitors can be safely downsized or even eliminated, leading to ease of integration. The two reported schemes possess many degrees of freedom to optimize charge balance, settling time and circuit parameters.

Acknowledgements

The author would like to thank Dr. P.V. Ramakrishna, Department of ECE, College of Engineering, Guindy for his guidance at various stages and insightful comments that greatly helped to improve on the results.

References

- [1] Sit J J and Sarpeshkar R 2007 A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6 nA DC error for 1-mA full-scale stimulation. *IEEE Trans. Biomed. Circuits Syst.* 1(3): 172–183, doi: 10.1109/TBCAS.2007.911631
- [2] Sooksood K, Stieglitz T and Ortmanns M 2010 An active approach for charge balancing in functional electrical stimulation. *IEEE Trans. Biomed. Circuits Syst.* 4(3): 162–170, doi: 10.1109/TBCAS.2010.2040277
- [3] Jiang D, Demosthenous A, Perkins T, Liu X and Donaldson N 2011 A stimulator ASIC featuring versatile management for vestibular prostheses. *Biomed. Circuits Syst. IEEE Trans.* 5(2): 147–159 doi: 10.1109/TBCAS.2011.2138139
- [4] Li Y T, Chen J J, Chen L T, Lin W S, Chu C H 2012 Wireless implantable biomicrosystem for bladder pressure monitoring and nerve stimulation. In: *Biomedical circuits and systems conference (BioCAS), 2012 IEEE*, pp 296–299, doi: 10.1109/BioCAS.2012.6418438
- [5] Cogan S F 2008 Neural stimulation and recording electrodes. *Ann. Rev. Biomed. Eng.* 10(1): 275–309, doi: 10.1146/annurev.bioeng.10.061807.160518, PMID: 18429704
- [6] Sooksood K, Stieglitz T and Ortmanns M 2009 An experimental study on passive charge balancing. *Adv. Radio Sci.* 7(15): 197–200
- [7] Lee E K F, Lam A 2007 A matching technique for biphasic stimulation pulse. *IEEE international symposium on circuits and systems*, pp 817–820, doi: 10.1109/ISCAS.2007.378031
- [8] Fang X, Wills J, Granacki J, LaCoss J, Choma J 2008 CMOS charge-metering microstimulator for implantable prosthetic device. *MWSCAS 2008 51st Midwest symposium on circuits and systems*, pp 826–829, doi: 10.1109/MWSCAS.2008.4616927
- [9] Ortmanns M, Rocke A, Gehrke M and Tiedtke H 2007 A 232-channel epiretinal stimulator ASIC. *IEEE J. Solid-State Circuits* 42(12): 2946–2959, doi: 10.1109/JSSC.2007.908693
- [10] Zheng L, Shin S, Kang S 2012 Design of a neural stimulator system with closed-loop charge cancellation. In: *VLSI and System-on-Chip (VLSI-SoC), 2012 IEEE/IFIP 20th international conference on*, IEEE, pp 1–6
- [11] Lo Y K, Hill R, Chen K, Liu W 2013 Precision control of pulse widths for charge balancing in functional electrical stimulation. In: *(NER) 6th international IEEE/EMBS conference on neural engineering*, pp 1481–1484, doi: 10.1109/NER.2013.6696225
- [12] Chu J U, Song K I, Shon A, Han S, Lee S H, Kang J Y, Hwang D, Suh J K F, Choi K and Youn I 2013 Feedback control of electrode offset voltage during functional electrical stimulation. *J. Neurosci. Methods* 218(1): 55–71, doi: 10.1016/j.jneumeth.2013.05.003, <http://www.sciencedirect.com/science/article/pii/S0165027013001775>
- [13] Zeng F G, Rebscher S, Harrison W, Sun X and Feng H 2008 Cochlear implants: System design, integration, and evaluation. *IEEE Rev. Biomed. Eng.* 1: 115–142 doi: 10.1109/RBME.2008.2008250
- [14] Jiang D, Demosthenous A, Cirmirakis D, Perkins T, Donaldson N 2010 Design of a stimulator asic for an implantable vestibular neural prosthesis. In: *Biomedical circuits and systems conference (BioCAS), 2010 IEEE*, pp 206–209, doi: 10.1109/BIOCAS.2010.5709607
- [15] Guo S, Lee H, Loizou P 2008 A 9-bit configurable current source with enhanced output resistance for cochlear stimulators. In: *Custom integrated circuits conference, 2008. CICC 2008. IEEE*, pp 511–514, doi: 10.1109/CICC.2008.4672134
- [16] Noorsal E, Sooksood K, Xu H, Hornig R, Becker J and Ortmanns M 2012 A neural stimulator frontend with high-voltage compliance and programmable pulse shape for epiretinal implants. *IEEE J. Solid-State Circuits* 47(1): 244–256, doi: 10.1109/JSSC.2011.2164667