Analog domain adaptive equalizer for low power 40 Gbps DP-QPSK receivers

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Abstract. Electrical domain equalization of chromatic and polarization mode dispersion is attractive in coherent optical communication links. Digital coherent receivers used for this purpose are based on high speed ADCs followed by DSP, which dissipate excessive amount of power and are very costly to implement. We propose analog coherent receiver to drastically reduce the power consumption, size and cost. An adaptive feed forward equalizer for 40 Gbps dual polarization quadrature phase shift keying (DP-QPSK) systems, which processes signals in analog domain itself, is demonstrated using circuit and system simulations. The equalizer, designed in 90 nm CMOS technology, consumes 450 mW of power and occupies $1.8 \text{ mm} \times 1.1 \text{ mm}$ chip area. System simulations are used to show that blind equalization is also possible when this approach is used in decision directed mode.

Keywords. Optical fibre communications; analog signal processing; adaptive equalizers; CMOS integrated circuits.

1. Introduction

Rapidly increasing data rates in the Internet backbones are posing serious challenges in development of optical networking equipment. In particular, the growing power dissipation in the communication equipment is making matters more complicated due to increasing thermal management requirements, which also increases size and cost of the equipment. In data centers, costs of energy and heat management is increasingly exceeding the cost of IT equipment (Belady 2007).

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High data rate optical links rely on coherent modulation and polarization multiplexing to increase spectral efficiency. These links use electronics, to remove channel impairments and recover transmitted data, which has become the bottleneck in practical receivers. Currently, electronic receivers rely on ultra-high-speed analog-to-digital converters (ADCs) followed by a digital signal processor (DSP). While ADCs generate data at a very high speed (typically at $\sim 4 \times 56$ GBytes/s or more for a 100 Gbps coherent DP-QPSK link (Dedic 2010; Zhang *et al* 2012)), the DSP speed is limited to ~ 500 MHz clock rates. Therefore, digital data from each ADC has to be massively parallelized, resulting in thousands of parallel interconnects and concurrent logic operations. As a result, there is an excessive amount of power consumption in high-speed ADCs, parallel interconnects, logic gates, parallel-to-serial/serial-to-parallel conversion blocks. In addition to power and chip area, a significant power/heat management effort is required that can finally make the solution very bulky.

As an example, a 40 Gbps DP-QPSK receiver employing this approach implemented in 90 nm CMOS technology dissipates 21 Watts of power (Sun *et al* 2008). A coherent receiver in a more advanced technology (65 nm CMOS) is expected to consume 50 Watts or more for a 100 Gbps DP-QPSK link (Dedic 2010), whereas a 100GBASE-ER4 compliant transceiver from Fujitsu is reported to consume 28 Watts (Fujitsu 100 GE CFP Transceiver).

To drastically reduce the power and chip area requirement, the high speed signals can be processed in analog domain itself, as suggested in figure 1. Primary signal processing operations in coherent receivers are equalization, carrier phase recovery and compensation (CPRC) and clock and data recovery (CDR). Analog circuits are, in general, preferred over digital for carrying out CDR and CPRC operations in high speed transceivers (Liao & Iuan Liu 2008; Huang *et al* 2011). A 100 Gbps analog coherent receiver for short distance DP-QPSK links employing Costas loop based CPRC has been discussed in Nambath *et al* (2013).

Equalization of high speed signals can be done in both analog and digital domains. However, equalization of complex signals has mostly been implemented in digital domain only, as it needs a two-dimensional (spatio-temporal) equalizer to jointly process two real signals. To make things more complicated, optical front-end of a DP-QPSK receiver provides two complex electrical signals (i.e., four real signals). Joint equalization of such signals in analog domain becomes hard to imagine. However, it is realized that since chromatic dispersion (CD) and polarization mode dispersion (PMD) are linear in nature, they can easily be compensated using tapped delay line equalizers (that act as linear transversal filters). Hence, joint equalization can be done using cross connected transversal filters. It can also be stated that even non-linear equalizers, such as decision feedback equalizer, can be implemented for joint processing in analog domain.

Figure 1. Analog coherent receiver architecture. The electrical signals from the photo-detectors are processed in the analog domain itself, obviating the need for power hungry ADCs and DSP.

In our work, we propose the design of an analog domain adaptive equalizer for 40 Gbps DP-QPSK link (initial results were published in Moyade *et al* (2012)). At high speeds, analog signal processing appears to be a much better choice for improving power efficiency of the system. Moreover, silicon implementation has got better prospects of integration with monolithic silicon coherent receivers such as the one in Doerr *et al* (2011). Here, we also show that the equalizer can be used in decision directed mode to adapt weight coefficients without using a training sequence.

2. Analog signal processing equalizer

Linear equalizer primarily has three unit operations—delay, multiplication and addition. In analog domain, high-speed multiplication can easily be performed using a variable gain amplifier or a Gilbert cell with less than 10 transistors. Similarly, summation of signals can be performed by simply adding currents onto a resistor. In addition, filter coefficients can be represented by charge stored on capacitors. In our design, adaptation is performed using Least Mean Square (LMS) algorithm in analog domain. However, part of LMS training block can be implemented in digital domain also (for example, see ref. Momtaz *et al* 2007), since the update of filter coefficients has to be performed at a much lower speed (and has negligible effect on the total power consumption of the system).

For DP-QPSK signals, the multidimensional transversal filter used to equalize the linear dispersive effects can be described by the equations (Savory *et al* 2007):

$$\tilde{x} = \mathbf{h}_{xx}^T \mathbf{x} + \mathbf{h}_{yx}^T \mathbf{y}, \quad (1)$$

$$\tilde{y} = \mathbf{h}_{xy}^T \mathbf{x} + \mathbf{h}_{yy}^T \mathbf{y}, \quad (2)$$

where, $\mathbf{x}$ and $\mathbf{y}$ are the column vectors of the delayed complex input electrical signals corresponding to the two polarization channels and $\tilde{x}$ and $\tilde{y}$ are the complex equalized outputs. Here $\mathbf{h}_{xx}$, $\mathbf{h}_{xy}$, $\mathbf{h}_{yx}$, $\mathbf{h}_{yy}$ are the column vectors of the complex LMS coefficients and can be computed as given in Savory *et al* (2007).

For analog domain implementation generic LMS update equation of a real coefficient is given by Karni & Zeng (1989):

$$h(t) = \beta \int_0^t x(\tau) \cdot e(\tau) \cdot d\tau, \quad (3)$$

where $h(t)$ is the weight coefficient, β is the gain parameter, $x(t)$ is the input signal, and $e(t)$ is the error signal (difference between desired signal and equalizer output). Here convergence of $h(t)$ is guaranteed for all positive values of β (Karni & Zeng 1989).

For complex signals and complex coefficients Eq. (3) can be modified as:

$$h(t) = \beta \int_0^t x(\tau) \cdot e^*(\tau) \cdot d\tau \quad (4)$$

The update equations for complex coefficients of the multidimensional equalizer, are modified versions of Eq. (4), which can be represented as

$$h_{xxk}(t) = \beta \int_0^t x(\tau - k\tau_d) \cdot e_x^*(\tau) \cdot d\tau, \quad (5)$$

$$h_{yxx}(t) = \beta \int_0^t y(\tau - k\tau_d) \cdot e_x^*(\tau) \cdot d\tau, \quad (6)$$

$$h_{xyk}(t) = \beta \int^t x(\tau - k\tau_d) \cdot e_y^*(\tau) \cdot d\tau, \quad (7)$$

$$h_{yyk}(t) = \beta \int^t y(\tau - k\tau_d) \cdot e_y^*(\tau) \cdot d\tau, \quad (8)$$

where, $x(t) = x_I(t) + jx_Q(t)$ and $y(t) = y_I(t) + jy_Q(t)$ are input signals to the equalizer in X and Y polarizations, $e_x(t) = e_x^I(t) + je_x^Q(t)$ and $e_y(t) = e_y^I(t) + je_y^Q(t)$ are error signals in X and Y polarizations, τ_d is the delay provided by a delay stage, and k is an integer between 0 and L , where L is the number of delay stages per dimension of the equalizer. The real and imaginary parts of $h_{xxk}(t)$ in Eq. (5) are given by

$$Re \{h_{xxk}(t)\} = \beta \int^t [x_I(\tau - k\tau_d) \cdot e_x^I(\tau) + x_Q(\tau - k\tau_d) \cdot e_x^Q(\tau)] d\tau, \quad (9)$$

$$Im \{h_{xxk}(t)\} = \beta \int^t [x_Q(\tau - k\tau_d) \cdot e_x^I(\tau) - x_I(\tau - k\tau_d) \cdot e_x^Q(\tau)] d\tau. \quad (10)$$

Similar expressions can be found for other coefficients also.

Depending on whether the equalizer uses a training sequence or decisions made on equalized outputs for generating error signals, operation of the equalizer can be classified into two modes - training mode and decision directed mode.

2.1 Training mode of equalizer

During the training mode of a feed forward equalizer (FFE), the error signals used in Eqs. (5–8) are calculated as:

$$e_x(t) = d_x(t) - \tilde{x}(t), \quad (11)$$

$$e_y(t) = d_y(t) - \tilde{y}(t), \quad (12)$$

where $d_x(t)$ and $d_y(t)$ are the transmitted training sequences and $\tilde{x}(t)$ & $\tilde{y}(t)$ are the equalized signals in X and Y polarizations respectively. Block diagram of an FFE in training mode is shown in figure 2. It consists of delay cells, butterfly multipliers, and LMS block.

2.2 Decision directed mode of equalizer

FFE is dependent on a known training sequence for its initial convergence (training mode). Storage of training sequence and synchronizing it with the incoming signal which is corrupted by channel imperfections add to the design overheads. Traditionally, blind equalizers are used to avoid training sequence. FFE works as a blind equalizer in decision directed mode and can easily be implemented using analog processing blocks.

In decision directed mode of operation, the error signals used for weight update in Eqs. (5–8) are generated as

$$e_x(t) = \hat{x}(t) - \tilde{x}(t), \quad (13)$$

$$e_y(t) = \hat{y}(t) - \tilde{y}(t), \quad (14)$$

where, $\hat{x}(t)$ and $\hat{y}(t)$ are decisions made on the equalized signals $\tilde{x}(t)$ and $\tilde{y}(t)$, respectively. During the initial phase of equalizer operation the probability of getting correct decision in the decision block is 0.5. Therefore equalizer weights are assured to be updated in the correct direction for half the time. Whereas, owing to the randomness of data, error signal due to incorrect decisions averages to zero over time because the chances of getting +ve error and -ve are

Figure 2. Block diagram of a 3 tap feed forward equalizer. $x_I + jx_Q$ and $y_I + jy_Q$ are the received signals corresponding to X and Y polarizations respectively, $d_{x,I} + jd_{x,Q}$ and $d_{y,I} + jd_{y,Q}$ are the training signals and $\tilde{x}_I + j\tilde{x}_Q$ and $\tilde{y}_I + j\tilde{y}_Q$ are the output signals. Inset shows the structure of a butterfly multiplier. All signals shown in the butterfly multiplier are complex signals.

equal. Hence, in the long run equalizer weights are updated so as to minimize error signals and convergence is achieved.

Figure 3 shows block diagram of an FFE in decision directed mode of operation. Signals from the delay lines are fed to butterfly multiplier blocks, where those are getting multiplied with the filter coefficients which are being generated in the LMS block. Outputs from the butterfly multipliers are added together to generate equalized signals $\tilde{x}(t)$ and $\tilde{y}(t)$ from which the decision blocks make decisions $\hat{x}(t)$ and $\hat{y}(t)$ respectively. These decisions are then fed-back to generate error signals $e_x(t)$ and $e_y(t)$ as given in Eq. (13) & Eq. (14). These error signals are used for filter coefficient update governed by Eqs. (5–8). Digital logic and proper initialization of equalizer

Figure 3. A 3 tap feed forward equalizer in decision directed mode of operation. $x_I + jx_Q$ and $y_I + jy_Q$, respectively are the received signals in X and Y polarizations and $\tilde{x}_I + j\tilde{x}_Q$ and $\tilde{y}_I + j\tilde{y}_Q$ are the corresponding output signals. Here decisions made on the equalizer outputs serve as training signals.

coefficients can be used to make sure that all output channels do not lock to the same transmitted signal.

3. Simulation results

The optical system was modelled in VPI transmission Maker. At the transmitter side, optical carrier from a DFB laser source with $\lambda = 1550$ nm and 1 MHz line-width was split into X and Y polarizations and were modulated using nested Mach-Zehnder modulators (MZMs). Combined optical signal from MZMs was transmitted through a standard single mode fibre having 16 ps/nm.km CD and mean differential group delay (DGD) of $0.1 \text{ ps/km}^{-1/2}$ due to PMD. The receiver had a polarization beam splitter (PBS) and polarization controllers (PCs) followed by 90° hybrids and photo-detectors (PDs) as shown in figure 1. In the absence of a carrier recovery and phase compensation circuit, the local oscillator (LO) optical signal was derived from the transmitter laser in the simulations.

3.1 Circuit simulations of training mode

Circuit simulations were carried out to verify the equalizer in training mode of operation. Electrical signals from PDs were fed to the equalizer circuit which was implemented using 90 nm CMOS technology. Figure 4a gives the schematic of a differential delay circuit using active load (Lin & Chiu 2007). Use of active delay circuit reduced area considerably as opposed to passive LC delay line. Each delay circuit gave a delay of 13 ps with 5.7% variation and had a bandwidth of 12.6 GHz after considering all loading effects including parasitic capacitances due to interconnects.

Butterfly multiplier used 16 real multipliers based on the folded version of Gilbert cell topology. The filter coefficients were taken from the output of integrators with a bandwidth of $\sim 1\text{--}5$ MHz, and hence were connected to the low speed inputs of multipliers. LMS block was implemented using high frequency Gilbert cell multipliers (again using a total of 16 multipliers) and two integrators for each weight coefficient. Circuit generating the real part of a single filter coefficient is shown in figure 4b. A common mode feedback circuit for maintaining dc levels and a digital control block for correcting offsets were also used in the LMS block. Total power

Figure 4. Schematics of (a) delay cell, in which M3(M4) and M5(M6) act as an active inductor and (b) LMS circuit for the real part of a single filter coefficient h .

dissipation of the equalizer was found to be 450 mW and it occupied an area of $1.8 \text{ mm} \times 1.1 \text{ mm}$. The chip has been fabricated and testing is pending due to want of set-up.

Circuit simulation results for a transmission over 50 km fibre (effective CD of 800 ps/nm and PMD with a mean DGD of 0.71 ps) at received OSNR of 15 dB is shown in figure 5a. Convergence of the error signals are shown figure 5b, from which it can be observed that polarization tracking can be done within a microsecond. A comparison of the equalizer performance for transmissions over 30 km and 75 km fibre at received OSNR of 25 dB is given in figure 6. It can be observed that a 3 tap equalizer removes dispersion completely for 30 km fibre (~ 40 ps dispersion), whereas it removes dispersion partially for 75 km fibre (~ 90 ps dispersion). Figure 7 shows bit error rate (BER) curves for transmission over different fibre lengths. With proper power budgets extremely low BER values can be obtained, obviating the need for forward error correction (FEC). Digital equalizers for long-haul links usually require an FEC module which also contributes to the total power consumption significantly. Pre-FEC BER of the order of 10^{-3} is reported in Zhang *et al* (2012) for a transmission of 1920 km with 0 dBm launch power. Similar BER were reported in Sun *et al* (2008) at 12.5 dB OSNR in a link of 900 km length and in Savory *et al* (2007) at -7 dBm launch power in a 6400 km link. Ultimately, total dispersion that can be mitigated by analog domain equalizer is limited by the number of delay stages

Figure 5. Circuit simulation results of feed forward equalizer in training mode for a transmission over 50 km fibre and an OSNR of 15 dB: (a) Signal constellations and (b) error signal corresponding to X polarization.

Figure 6. Circuit simulation results of feed forward equalizer in training mode for a transmission over (a) 30 km and (b) 75 km fibre. X polarization signal constellations at a received OSNR of 25 dB are shown.

Figure 7. Simulated bit error rate plots for different fibre lengths.

Figure 8. X polarization signal constellations for decision directed mode of the equalizer with 50 km fibre and 15 dB input OSNR.

in the equalizer. However, for short distance links and CD compensated links, where effective dispersion is not very high, analog equalizer appears to be a much more efficient implementation.

3.2 System simulations of decision directed mode

For decision directed mode of operation, the equalizer was modelled in Simulink as a fractionally spaced one with a delay of 20 ps per delay cell. Figure 8 shows the input and output constellations obtained for the X polarization signals at a received OSNR of 15 dB for a transmission over 50 km fibre.

4. Conclusion

Analog domain adaptive equalizers will be a cost effective solution for low power, high performance coherent receivers, particularly for short distance links, dispersion managed links or for coherent links using 1300 nm wavelength where only polarization rotation, small amount of PMD and residual CD has to be removed. An analog signal processing equalizer, implemented using 90 nm CMOS technology for 40 Gbps DP-QPSK link, consumes 450 mW of power and occupies an area of 1.8 mm × 1.1 mm. System simulations show that blind equalization is also possible with analog domain processing. An analog coherent receiver for 40 Gbps DP-QPSK links can be implemented with less than 1 Watt power consumption.

100 Gbps DP-QPSK signals, with a baud rate of 25 Gbaud, would typically require an electrical bandwidth of less than 20 GHz. Such bandwidths have been achieved using 65 nm or 40 nm CMOS technologies, and more conveniently using processes supporting HBTs, such as SiGe BiCMOS technology (that can easily have unity gain frequency beyond 200 GHz). Therefore, analog implementation in these advanced processes is expected to work for 100 Gbps coherent links. For long haul links, analog processing combined with low resolution ADC+DSP approach appears to be a low power alternative to high resolution ADC+DSP chips.

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