Sādhanā Vol. 38, Part 4, August 2013, pp. 653–665. © Indian Academy of Sciences

Analysis and design of a high-efficiency zero-voltage-switching step-up DC–DC converter

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MS received 22 September 2011; revised 13 June 2013; accepted 26 June 2013

Abstract. A high-efficiency zero-voltage-switching (ZVS) step-up DC–DC converter is proposed. The proposed ZVS DC–DC step-up converter has fixed switching frequency, simple control, and high efficiency. All power switches can operate with ZVS. The output diodes are under zero-current-switching (ZCS) during turn-off. Due to soft-switching operation of the power switches and output diodes, the proposed ZVS DC–DC converter shows high efficiency. Steady-state analysis of the converter is presented to determine the circuit parameters. A laboratory prototype of the proposed converter is developed, and its experimental results are presented for validation.

Keywords. DC–DC converter; soft-switching; high voltage gain; zero-voltage-switching; zero-current-switching.

1. Introduction

Recently, high-efficiency power conversion techniques have been researched due to the increasing emphasis on the environment protection and energy saving. Also, high efficiency is one of the most important factors in step-up DC–DC converters used in applications such as electric vehicles, uninterruptible power supplies, fuel cells, and photovoltaic systems (Wai *et al* 2008; Wang & Nehrir 2008; Wai & Wang 2008; Prudente *et al* 2008; Ismail *et al* 2008).

The step-up DC–DC converters can be classified into two types; voltage-fed type and current-fed type. The current-fed converters are often used in step-up applications due to their inherent low input current ripple characteristic (Zhu *et al* 2003; Cha *et al* 2008; Adib & Farzanehfard 2009). However, in the current-fed converters, the voltage stresses of the switches are serious. In order to clamp the voltages across the switches and provide ZVS features, active snubbers are often employed. However, since the snubbers cause additional conduction losses, the system efficiency decreases. On the other hand, the voltage-fed converters shows low voltage stress of

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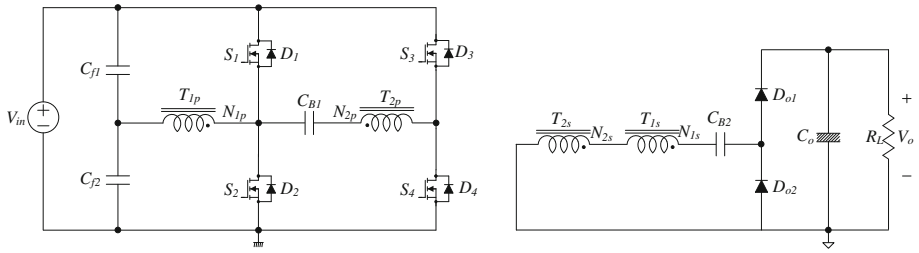

Figure 1. Circuit diagram of the proposed converter.

the switching devices, which is confined to the input voltage. Among them, phase-shift full-bridge converters are widely used. They feature fixed switching frequency and ZVS of power switches. However, they have some drawbacks such as large conduction loss due to circulating current, duty cycle loss, and the voltage spikes across output rectifiers. The large voltage spikes of the output rectifiers are serious problems especially in high voltage applications. To remedy these problems, many topologies have been proposed in (Jang & Jovanovic 2004; Borage *et al* 2008; Jang & Jovanovic 2007; Ordonez & Quaicoe 2011; Chen *et al* 2008; Redl *et al* 1991). In some of them, auxiliary snubbering circuits are employed to suppress the voltage spikes at the secondary side. However, the complexity and the overall cost are raised and the system efficiency decreases due to the additional circuits.

In order to overcome these problems, a high-efficiency ZVS step-up DC–DC converter shown in figure 1 is proposed. Asymmetrical pulse width modulation (APWM) control technique suggested in (Imbertson & Mohan 1993) is applied to the proposed converter to eliminate switching losses and maintain low conduction loss. The proposed converter features fixed switching frequency, soft-switching operations of all power switches and output diodes, and clamped voltage across power switches and output diodes without any auxiliary circuit. Moreover, the reverse-recovery problem of the output diodes is significantly alleviated due to the leakage inductance of the transformers. Therefore, the proposed converter shows high efficiency and it is suitable to high voltage applications.

2. Analysis of the proposed DC–DC converter

Figure 1 shows the circuit diagram of the proposed high-efficiency ZVS step-up DC–DC converter. The proposed converter has two split input filter capacitors C_{f1} and C_{f2} and two dc-blocking capacitors C_{B1} and C_{B2}. In order to obtain a high voltage gain, the output stage of the proposed converter has a voltage doubler structure which consists of two secondary windings N_{1s} and N_{2s} of two transformers, the capacitor C_{B2}, and the output diodes D_{o1} and D_{o2}. APWM control technique in (Imbertson & Mohan 1993) is applied to the proposed converter to eliminate switching losses and maintain low conduction loss. The equivalent circuit of the proposed high-efficiency ZVS step-up DC–DC converter is shown in figure 2. The diodes D_1 through D_4 are the intrinsic body diodes of all switches. The capacitors C_1 through C_4 represent their parasitic output capacitances. The transformer T_1 is modelled as the magnetizing inductance L_{m1} and the ideal transformer which has a turn ratio of $1{:}n_1$ ($n_1 = N_{1s}/N_{1p}$). Its leakage inductance is included in the total leakage inductance L_k. Similarly, the transformer T_2 is modelled as the magnetizing inductance L_{m2} and the ideal transformer which has a turn ratio of $1{:}n_2$ ($n_2 = N_{2s}/N_{2p}$). To simplify the analysis, the voltages across the capacitors are assumed to be

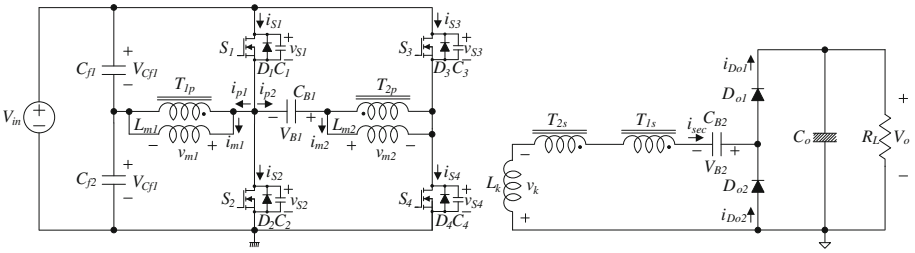

Figure 2. Equivalent circuit of the proposed converter.

constant under a steady state. The theoretical waveforms of the proposed ZVS DC–DC converter are shown in figure 3. The switch S_1 (S_4) and the switch S_2 (S_3) are operated asymmetrically and the duty ratio D is based on the switch S_1 (S_4). The operation of the proposed converter during a switching period T_s can be divided into four modes and they are shown in figure 4. Before t_0, the switches S_1 and S_4, and the output diode D_{o1} are conducting. At t_0, the magnetizing currents i_{m1} and i_{m2} and the output diode current i_{Do1} arrive at their maximum values I_{m1}, I_{m2}, and I_{Do1}, respectively.

Mode 1 [t_0, t_1]: At t_0, the switches S_1 and S_4 are turned off at the same time. Then, the energy stored in the magnetic components starts to charge/discharge the parasitic capacitances C_1 through C_4. Therefore, the voltages v_{S1} and v_{S4} start to rise from zero and the voltage v_{S2} and v_{S3} start to fall from the input voltage V_{in}. Since all the parasitic output capacitances C_1 through C_4 are very small, this transition time interval is very short and it can be ignored. When the voltages v_{S2} and v_{S3} arrive at zero, their body diodes D_2 and D_3 are turned on. Then, the gate signals are applied to the switches S_2 and S_3 at the same time. Since the currents have already flown through D_2 and D_3 and the voltages v_{S2} and v_{S3} are clamped as zero before the switches S_2 and S_3 are turned on, zero-voltage turn-on of S_2 and S_3 is achieved. With the turn-on of S_2, the voltage v_{m1} across L_{m1} is $-V_{Cf2}$. Then, the current i_{m1} decreases linearly from its maximum value I_{m1} as follows:

$$i_{m1}(t) = I_{m1} - \frac{V_{Cf2}}{L_{m1}}(t - t_0). \tag{1}$$

The voltage v_{m2} across L_{m2} is $-(V_{in} - V_{B1})$. Therefore, the current i_{m2} decreases linearly from its maximum value I_{m2} as follows:

$$i_{m2}(t) = I_{m2} - \frac{V_{in} - V_{B1}}{L_{m2}}(t - t_0) \tag{2}$$

Since the voltage v_k across L_k is $-(n_1 V_{Cf2} + n_2(V_{in} - V_{B1}) + V_o - V_{B2})$, the current i_{sec} decreases from its maximum value I_{Do1} as follows:

$$i_{\text{sec}}(t) = I_{Do1} - \frac{n_1 V_{Cf2} + n_2(V_{in} - V_{B1}) + V_o - V_{B2}}{L_k}(t - t_0). \tag{3}$$

In this mode, the switch currents i_{S2} and i_{S3} can be written by

$$i_{S2}(t) = -i_{m1}(t) - i_{m2}(t) - (n_1 + n_2)\, i_{\text{sec}}(t), \tag{4}$$

$$i_{S3}(t) = -i_{m2}(t) - n_2 i_{\text{sec}}(t). \tag{5}$$

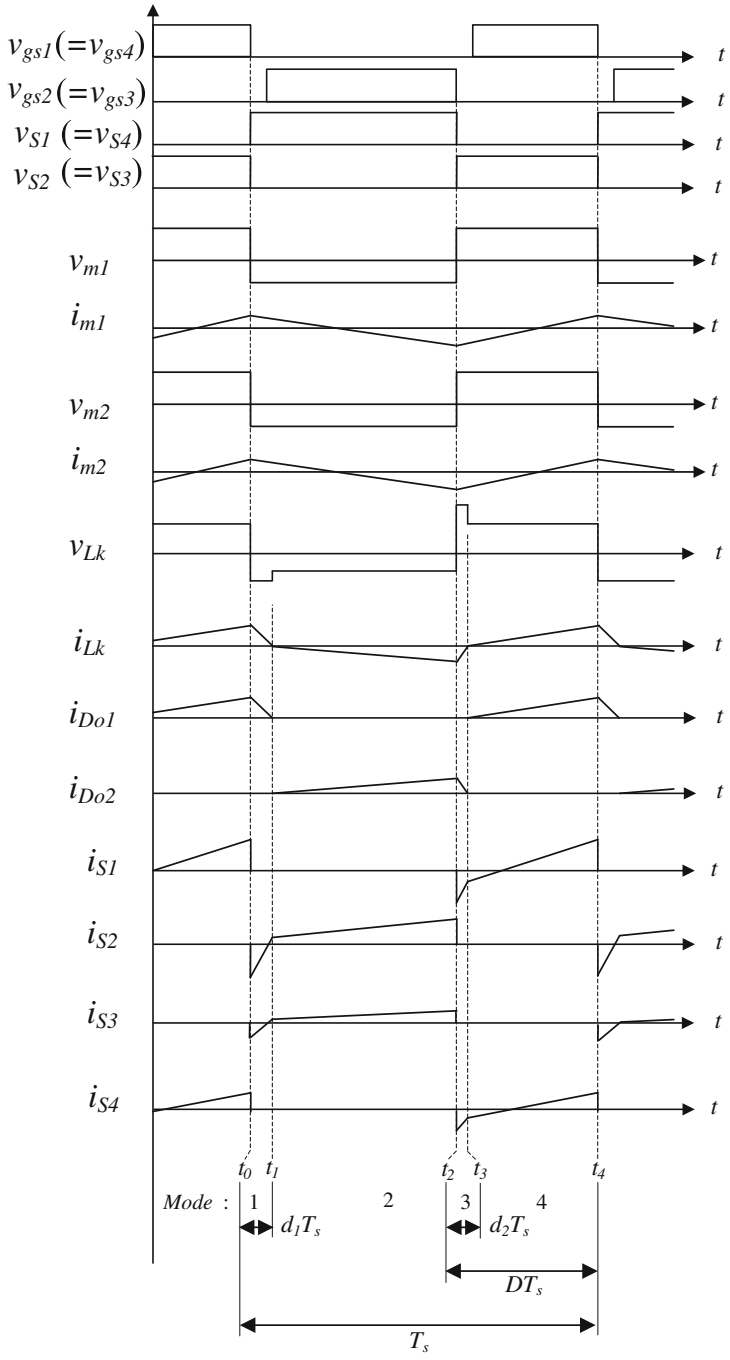

Figure 3. Theoretical waveforms.

Mode 2 [t_1, t_2]: At t_1, the current i_{Do1} decreases to zero and the diode D_{o1} is turned off. Then, the output diode D_{o2} is turned on and its current increases linearly. Since the current changing rate of D_{o1} is controlled by the leakage inductance L_k of the transformers T_1 and T_2, its

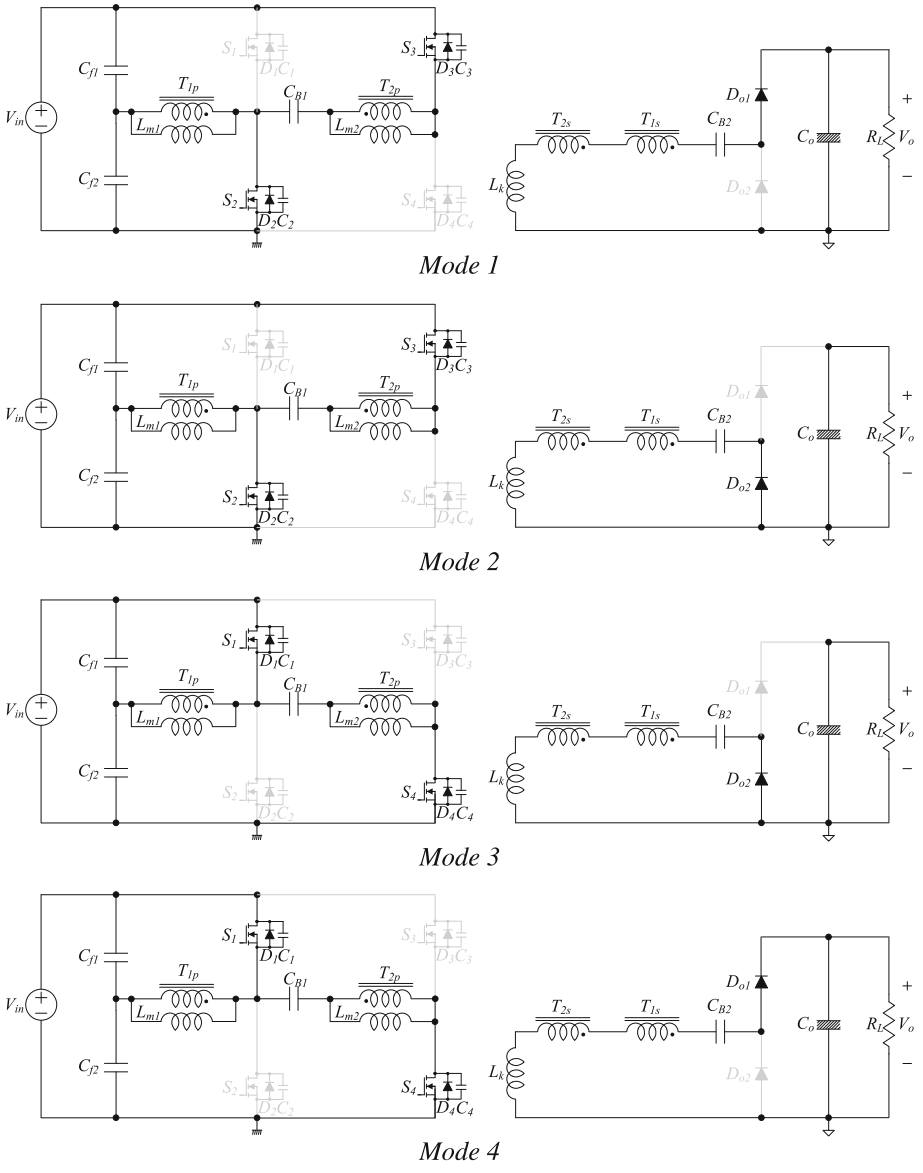

Figure 4. Operating modes.

reverse-recovery problem is alleviated. Since the voltage v_k is $-(n_1 V_{Cf2} + n_2(V_{in}-V_{B1})-V_{B2})$ in this mode, the current i_{sec} are given by

$$i_{\text{sec}}(t) = -\frac{n_1 V_{Cf2} + n_2 (V_{in} - V_{B1}) - V_{B2}}{L_k} (t - t_1) . \tag{6}$$

Since the voltages v_{m1} and v_{m2} are not changed in this mode, the equations of (1), (2), (4), and (5) are still effective. At the end of this mode, the currents i_{m1}, i_{m2}, and i_{sec} arrive at their minimum value $-I_{m1}$, $-I_{m2}$, and $-I_{Do2}$, respectively.

Mode 3 [t_2, t_3]: At t_2, the switches S_2 and S_3 are turned off at the same time. Similar to mode 1, the parasitic capacitors C_2 and C_3 start to be charged from zero, whereas the parasitic capacitors C_1 and C_4 start to be discharged from V_{in} due to the energy stored in the magnetic components. Since all the parasitic capacitors C_1 through C_4 have very small values, this transition time interval is very short and it can be ignored. After the parasitic capacitors are fully charged and discharged, the voltages v_{S1} and v_{S4} become zero and the body diodes D_1 and D_4 are turned on. Then, the gate signals are applied to the switches S_1 and S_4. Since the currents have already flown through D_1 and D_4 and the voltages v_{S1} and v_{S4} are clamped as zero before the switches S_1 and S_4 are turned on, zero-voltage turn-on of S_1 and S_4 is achieved. With the turn-on of S_1, the voltage v_{m1} across L_{m1} is V_{Cf1}. Then, the current i_{m1} increases linearly from its minimum value $-I_{m1}$ as follows:

$$i_{m1}(t) = -I_{m1} + \frac{V_{Cf1}}{L_{m1}}(t - t_2). \tag{7}$$

The voltage v_{m2} across L_{m2} is $V_{in} + V_{B1}$. Therefore, the current i_{m2} increases linearly from its minimum value $-I_{m2}$ as follows:

$$i_{m2}(t) = -I_{m2} + \frac{V_{in} + V_{B1}}{L_{m2}}(t - t_2). \tag{8}$$

Since the voltage v_k across L_k is $n_1 V_{Cf1} + n_2(V_{in} + V_{B1}) + V_{B2}$, the current i_{sec} increases from its minimum value $-I_{Do2}$ as follows:

$$i_{\text{sec}}(t) = -I_{Do2} + \frac{n_1 V_{Cf1} + n_2(V_{in} + V_{B1}) + V_{B2}}{L_k}(t - t_2). \tag{9}$$

In this mode, the switch currents i_{S1} and i_{S4} can be written by

$$i_{S1}(t) = i_{m1}(t) + i_{m2}(t) + (n_1 + n_2)\, i_{\text{sec}}(t), \tag{10}$$

$$i_{S4}(t) = i_{m2}(t) + n_2 i_{\text{sec}}(t). \tag{11}$$

Mode 4 [t_3, t_4]: At t_3, the current i_{Do2} decreases to zero and the diode D_{o2} is turned off. Then, the output diode D_{o1} is turned on and its current increases linearly. Since the current changing rate of D_{o2} is controlled by L_k, its reverse-recovery problem is significantly alleviated. Since the voltage v_k is $n_1 V_{Cf1} + n_2(V_{in} + V_{B1}) - V_o + V_{B2}$, the current i_{sec} is given by

$$i_{\text{sec}}(t) = \frac{n_1 V_{Cf1} + n_2(V_{in} + V_{B1}) - V_o + V_{B2}}{L_k}(t - t_3). \tag{12}$$

Since the voltages v_{m1} and v_{m2} are not changed in this mode, the equations of (7), (8), (10), and (11) are still effective. At the end of this mode, the currents i_{m1}, i_{m2}, and i_{Lk} arrive at I_{m1}, I_{m2}, and I_{Do1}, respectively.

3. Design parameters

3.1 *Voltages across the split input filter capacitors C_{Cf1} and C_{Cf2}*

Since the average inductor voltage must be zero under a steady-state condition, the capacitor voltages V_{Cf1} and V_{Cf2} are equal to the average values of the switch voltages v_{S1} and v_{S2},

respectively. Therefore, they are given by

$$V_{Cf1} = (1 - D)\, V_{in}, \tag{13}$$

$$V_{Cf2} = DV_{in}. \tag{14}$$

3.2 *Voltage across the dc-blocking capacitor C_{B1}*

Similarly, the voltage V_{B1} across C_{B1} is equal to the difference between the average values of the switch voltages v_{S4} and v_{S2} as follows:

$$V_{B1} = (1 - 2D)\, V_{in}. \tag{15}$$

3.3 *Maximum values of the magnetizing currents i_{m1} and i_{m2}*

From (1) and (14), the maximum magnetizing current I_{m1} is derived by

$$I_{m1} = \frac{D\,(1 - D)\, V_{in} T_s}{2L_{m1}}. \tag{16}$$

From (2) and (15), the maximum magnetizing current I_{m2} is derived by

$$I_{m2} = \frac{D\,(1 - D)\, V_{in} T_s}{L_{m2}}. \tag{17}$$

3.4 *Voltage gain*

From (3) and (12), the maximum diode current I_{Do1} is derived by

$$\begin{aligned} I_{Do1} &= \frac{n_1 V_{Cf2} + n_2\,(V_{in} - V_{B1}) + V_o - V_{B2}}{L_k} d_1 T_s \\ &= \frac{n_1 V_{Cf1} + n_2\,(V_{in} + V_{B1}) - V_o + V_{B2}}{L_k}\,(D - d_2)\, T_s. \end{aligned} \tag{18}$$

From (13), (14), (15), and (18), the following relation can be obtained by

$$V_o - V_{B2} = \frac{D\,(1 - D) - Dd_1 - (1 - D)\, d_2}{D + d_1 - d_2} \cdot (n_1 + 2n_2)\, V_{in}. \tag{19}$$

Similarly, from (6) and (9), the maximum diode current I_{Do2} can be written as follows:

$$\begin{aligned} I_{Do2} &= \frac{n_1 V_{Cf2} + n_2\,(V_{in} - V_{B1}) - V_{B2}}{L_k}\,(1 - D - d_1)\, T_s \\ &= \frac{n_1 V_{Cf1} + n_2\,(V_{in} + V_{B1}) + V_{B2}}{L_k} d_2 T_s. \end{aligned} \tag{20}$$

From (13), (14), (15), and (20), V_{B2} can be obtained by

$$V_{B2} = \frac{D\,(1 - D) - Dd_1 - (1 - D)\, d_2}{1 - D - d_1 + d_2} \cdot (n_1 + 2n_2)\, V_{in}. \tag{21}$$

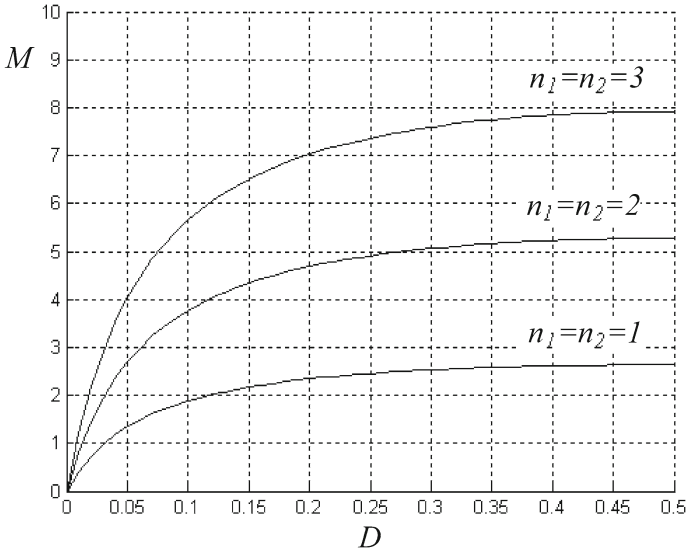

Figure 5. Voltage gain M with $k = 0.06$.

From figure 3, the output current I_o can be represented by

$$I_o = \frac{(D + d_1 - d_2)\, I_{Do1}}{2} = \frac{(1 - D - d_1 + d_2)\, I_{Do2}}{2}. \tag{22}$$

From (18) through (22), d_1 and d_2 is obtained by

$$d_1 = k\,(1 - D)\,, \tag{23}$$

$$d_2 = kD, \tag{24}$$

$$k = \frac{1}{2}\left(1 - \sqrt{1 - \frac{8L_k I_o}{(n_1 + 2n_2)\, D\,(1 - D)\, V_{in} T_s}}\right). \tag{25}$$

From (19) and (21), the voltage gain M of the proposed converter is obtained by

$$M = \frac{V_o}{V_{in}} = \frac{(n_1 + 2n_2)\,(1 - 2k)\, D\,(1 - D)}{(D - (2D - 1)\,k)\,(1 - D + (2D - 1)\,k)}. \tag{26}$$

Figure 5 shows the voltage gain M according to D.

3.5 *ZVS conditions for the switches S_1 through S_4*

Since the currents i_{m1}, i_{m2}, and i_{sec} arrive at I_{m1}, I_{m2}, and I_{Do1} at the end of mode 4, the ZVS conditions for S_2 and S_3 are given by

$$I_{m1} + I_{m2} + (n_1 + n_2)\, I_{Do1} > 0, \tag{27}$$

$$I_{m2} + n_2 I_{Do1} > 0. \tag{28}$$

Similarly, since the currents i_{m1}, i_{m2}, and i_{sec} arrive at $-I_{m1}$, $-I_{m2}$, and $-I_{Do2}$, at the end of mode 2, the ZVS conditions for S_1 and S_4 are given by

$$I_{m1} + I_{m2} + (n_1 + n_2)\, I_{Do2} > 0, \tag{29}$$

$$I_{m2} + n_2 I_{Do2} > 0. \tag{30}$$

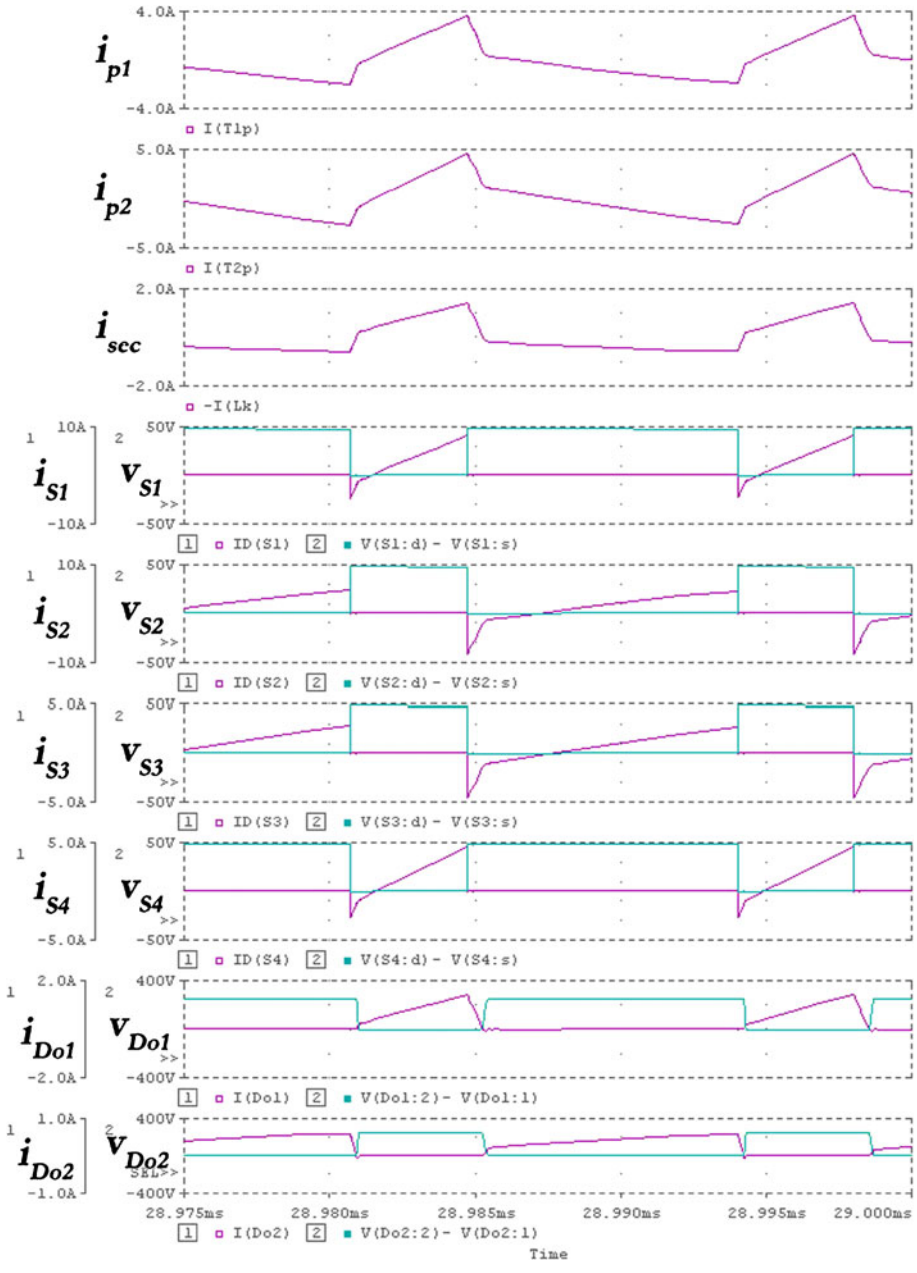

Figure 6. Simulation results.

Since n_1, n_2, I_{m1}, I_{m2}, I_{Do1}, and I_{Do2} always have positive values, it can be easily seen that the ZVS of all switches is achieved. For a proper ZVS operation, deadtimes of S_1 and S_2 (S_3 and S_4) also need to be considered. It is because the gate signal should be applied to the switch before the current flowing through the anti-parallel diode changes its direction. This condition can determine the leakage inductance. From (25), the leakage inductance L_k can be determined as follows:

$$L_k = \frac{(n_1 + 2n_2)\, V_{in} D\,(1 - D)\, T_s}{8 I_o} \left[1 - \left(1 - 2k^*\right)^2\right], \tag{31}$$

where $k^* =$ a predetermined value of k.

4. Experimental results

The performance of the proposed converter was verified on a 60 W prototype. The prototype was designed to operate from a 48 V input voltage and provide 240 V output voltage. Its operating frequency was 75 kHz. The required voltage gain was 5. The value of k was selected as 0.06. According to (26), the turn ratios n_1 and n_2 were selected as 2 with an assumption that the duty ratio D was 0.3. The magnetizing inductances L_{m1} and L_{m2} were selected as 82 μH. The total leakage inductance L_k was 90 μH. The filter capacitors C_{f1} and C_{f2} and the dc-blocking capacitors C_{B1} and C_{B2} were chosen as 6.6 μF. Figure 6 shows p-spice simulation results based on the specifications and the circuit parameters of the prototype. The key waveforms and the soft-switching waveforms of the power switches S_1 through S_4 and the output diodes D_{o1} and D_{o2} are shown in figure 6. The ZVS turn-on of the power switches and the ZCS turn-off of the output diodes are achieved. Figure 7 shows the measured waveforms of the proposed high-efficiency ZVS DC-DC converter with a high voltage gain at fixed switching frequency 75 kHz. Figure 7 shows the currents i_{p1}, i_{p2}, i_{sec}, the output voltage V_o, and the switch voltage v_{S2}. Since the magnetizing current of T_2 is two times larger than that of T_1, the peak value of the current i_{p2} is larger than that of i_{p1}. It can be seen from figure 7 that the experimental waveforms agree with the theoretical analysis and the simulation results. The measured soft-switching waveforms of all switches and diodes are shown in figure 8. The ZVS operations of the full-bridge switches are shown in figure 8a. The voltages across the switches go to zero before the gate pulses are applied to the switches. Since the switch voltages are clamped as zero before the gate pulses are applied, the ZVS turn-on of the switches is achieved. Figure 8b shows the ZCS of the output

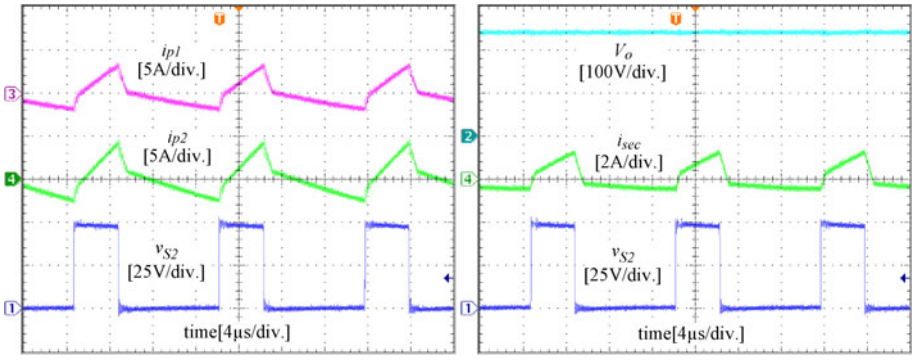

Figure 7. Measured key waveforms.

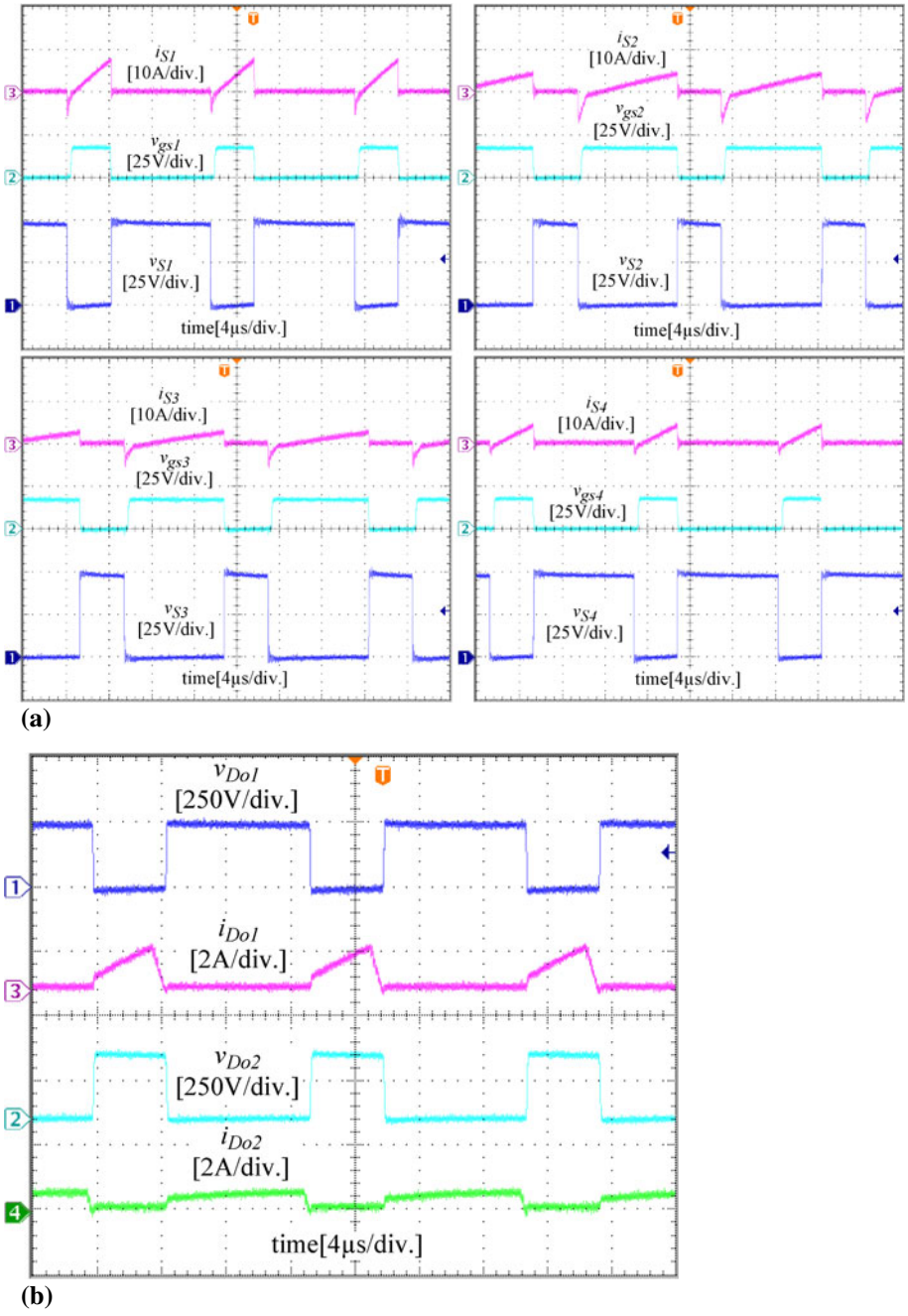

Figure 8. Measured soft-switching waveforms of all switches and diodes: (**a**) S_1 through S_4, (**b**) D_{o1} and D_{o2}.

diodes. After the diode currents fall to zero, the voltages across the diode rise to the output voltage V_o. Therefore, the ZCS turn-off of the output diodes is achieved. It can be seen that the voltages v_{Do1} and v_{Do2} are confined to V_o without a clamping circuit and a snubbering circuit.

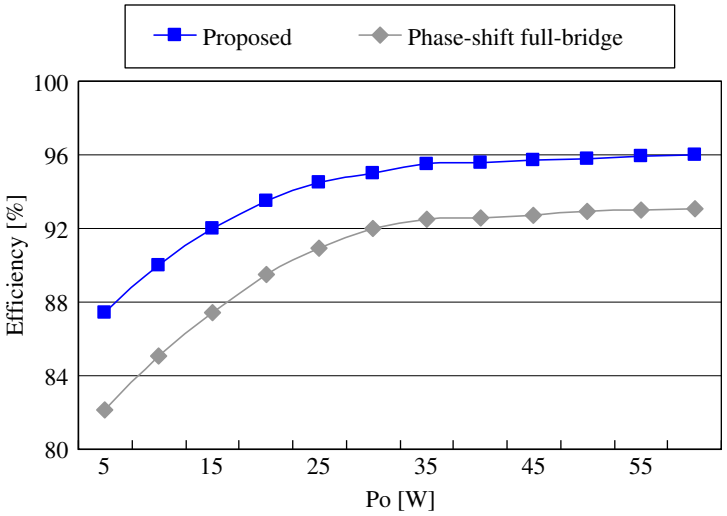

Figure 9. Measured efficiency.

Figure 9 shows the measured efficiency of the proposed ZVS step-up DC–DC converter. The efficiency was measured with WT230-Digital Power Meter from YOKOGAWA from 5 W to 60 W load. The proposed converter exhibits the efficiency of 96.1% at full load. Due to its soft-switching characteristic and alleviated reverse-recovery problem, it shows a higher efficiency than the previous phase-shift full-bridge converter.

5. Concluding remarks

The analysis, design, and experimental results of a high-efficiency ZVS step-up DC–DC converter have been presented. The ZVS of all power switches and ZCS of the output diodes are achieved. The proposed converter shows a higher efficiency than previous works. Also, without any auxiliary circuits, the voltages across the switches and the output diodes are confined to the input voltage and the output voltage, respectively. Therefore, the proposed step-up DC–DC converter is suitable for high voltage applications. Experimental results on a prototype are provided for validation.

Acknowledgement

This work was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2011-0021186).

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