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RF sputtering: A viable tool for MEMS fabrication

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Abstract. Fabrication of Micro-Electro-Mechanical-Systems (MEMS) requires deposition of films such as SiO_2, Si_3N_4, ZnO, polysilicon, phosphosilicate glass (PSG), Al, Cr-Au, Pt, etc. for use as structural, sacrificial, piezoelectric and conducting material. Deposition of these materials at low temperature is desirable for fabricating sensors/actuators on temperature-sensitive substrates and also for integrating MEMS structures on silicon in post-CMOS processing procedures. Plasma enhanced chemical vapour deposition (PECVD) and sputtering are amongst potential techniques for preparing films for MEMS fabrication at comparatively low temperatures. The sputtering technique has an added advantage that the process is carried out in an inert ambient (argon) and chemically sensitive substrate/sacrificial layers can be used in realization of MEMS. Furthermore, the same system can be used for depositing dielectric, piezoelectric and conducting materials as per requirement in the fabrication sequence. This enables rapid low-cost prototyping of MEMS with minimum fabrication facilities.

In the present work, we report preparation, characterization and application of RF sputtered SiO_2, Si_3N_4 and ZnO films for MEMS fabrication. The effect of RF power, sputtering pressure and target-to-substrate spacing was investigated on the structural and other properties of the films. The residual stress in the films was obtained using wafer curvature measurement technique. The deposition parameters are optimized to obtain low stress films of SiO_2 and Si_3N_4. The self-heating of the substrate during deposition was advantageously exploited to obtain highly *c*-axis oriented films of ZnO without any external heating. A variety of MEMS structures such as cantilever beams, micro-bridges, diaphragms, etc. are demonstrated using bulk, surface and surface-bulk micromachining techniques.

Keywords. RF sputtering; dielectric films; piezoelectric films; MEMS; micromachining.

1. Introduction

Fabrication of Microelectromechanical Systems (MEMS) often requires deposition of thin film of dielectric, piezoelectric, semiconductor and metal such as silicon dioxide, silicon nitride, phosphosilicate glass (PSG), zinc oxide, polycrystalline/amorphous silicon,

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chromium, gold, platinum, titanium etc. These materials are used as structural and sacrificial layers, sensing elements and for interconnection in sensors/actuators. In the fabrication sequence, the sensors/actuators are often realized in post-CMOS processing steps and the deposition conditions must then be compatible with the circuits already realized on the silicon wafer. This puts a limit (usually below 400°C) on the processing temperature that can be used in sensor/actuator fabrication related steps. Furthermore, the sensors are sometimes fabricated on temperature-sensitive substrates (e.g. polymers) or use such materials as sacrificial layer (e.g. photoresist). This puts some additional restriction on the techniques, which can be used for deposition processes.

Silicon dioxide, silicon nitride, polycrystalline/amorphous silicon and PSG films are routinely used in IC fabrication process. Various types of chemical vapour deposition techniques are used for this purpose. Considering the requirement of deposition at low temperature (less than 400°C), plasma enhanced chemical vapour deposition (PECVD) and RF sputtering are potentially suitable techniques. PECVD is the most widely accepted process for the deposition of SiO_2, SiN, PSG and amorphous silicon films due to high throughput and excellent control of film properties. The RF sputtering process has some advantage in terms of: simple low-cost deposition system, absence of toxic/pyrophoric gases from the process and the possibility of sequential deposition of different films in the same system. These advantages have led to several recent research publications focusing on RF sputtering technique as a viable method of preparing dielectric/semiconductor films for MEMS applications (Folta *et al* 1994; Hurley & Gamble 2003) While RF sputtered piezoelectric films of ZnO are extensively investigated over the past 20 years (Chu *et al* 2003; Ondo-Ndong *et al* 2003; Mitsuyu *et al* 1980), the ferroelectric films of lead zirconate titanate (PZT) and its derivatives are also now being prepared by RF sputtering and their application in MEMS being explored. ZnO films have recently been investigated as a sacrificial layer also in surface micromachining process (Bhatt *et al* 2005). It is visualized that RF sputtering can be advantageously used for rapid prototyping of several MEMS devices.

In the present work, we report preparation of silicon dioxide, silicon nitride and piezoelectric ZnO films by RF sputtering process. The properties of these films relevant for MEMS applications have been evaluated. The application of these films in fabricating basic MEMS structures such as diaphragm, micro-cantilever beams, etc. has been demonstrated.

2. Experimental work

2.1 *Film preparation*

Thin films of silicon dioxide, silicon nitride and zinc oxide were prepared in RF (13·56 MHz) diode/magnetron system using 3-inch diameter stoichiometric targets of the respective materials. Most of the films were deposited on 1–10 ohm-cm, (100) oriented *p*-type silicon-wafer of 2-inch diameter. The ZnO deposition was also carried out on other substrates such as heavily boron diffused (P^+) silicon, oxidized silicon and metal-coated glass substrates. The sputtering for silicon dioxide and silicon nitride was carried out in diode mode at 100–300 W RF power in Ar ambient in the pressure range 5–20 mTorr at a fixed target-to-substrate separation of 45 mm. For ZnO deposition, a mixture of Ar–O_2 and the magnetron target was used. The target to substrate separation was also varied from 40–60 mm. Although no external substrate heating was provided during the deposition process, the substrate temperature rises due to self-heating in plasma and this was monitored by fixing a thermocouple on the substrate (Singh *et al* 2007). For ZnO deposition, the substrate heating due to plasma was exploited to

obtain highly *c*-axis oriented films, which is a requirement for these films to be piezoelectric in nature. In addition to the dielectric films, thin films of Cr, Au, Ti and Pt on silicon or glass substrates, (used for ZnO deposition) were also deposited by RF sputtering process.

2.2 *Film characterization*

The thickness (t), refractive index (n) and the absorption coefficient (k) of the transparent films were measured by spectroscopic measurement (Filmetrics F20, UV-visible thin film analyzer) while alpha-step (Tencor) was used for thickness measurement of other films. The crystallographic properties were evaluated using XRD analysis (CuK_α radiation, $\lambda = 1{\cdot}540'$; Brucker-AXS diffrometer, D8 Advance Model). The residual stress is an important parameter, when the films are to be used as structural material in MEMS. This was evaluated for SiO_2 and Si_3N_4 films using wafer curvature measurement technique (FSM Frontier Semiconductor). The effect of deposition parameters on the etch rates of SiO_2 films in buffered hydrofluoric acid (BHF), potassium hydroxide (KOH) and EPW (ethylenediamine pyrocatechol water) solutions was evaluated. The DC resistivity of the ZnO film is an important parameter for its application in piezoelectric based devices and the same was measured on a MOS/MIM (metal oxide semiconductor/metal-insulator-metal) capacitor structure using automated I–V measurement set-up. The surface morphology and root-mean-square (rms) surface roughness of the films were characterized using scanning electron microscope (SEM) and atomic force microscope (AFM).

2.3 *Microstructure fabrication*

To illustrate the process for realizing MEMS structures, RF sputtered silicon dioxide micro-cantilever beams and micro-bridges were fabricated on single-side polished *P*- or *n*-type (100) silicon wafer by bulk micromachining (BM), surface micromachining (SM) and surface-bulk micromachining (SBM) techniques.

Cantilever beams of RF sputtered SiO_2 were fabricated with varying widths and length using bulk micromachining process. The silicon anisotropic etching was carried out in EPW solution for approximately 1 h. The cantilever beams are released due to undercutting initiated from convex corners. The complete process sequence is given elsewhere (Bhatt & Chandra 2007a). For SiO_2 micro-bridge fabrication, the convex corners are not available to cause undercutting. For this reason, silicon was selectively etched using Reactive Ion Etching (RIE) process following patterning of SiO_2 film in BHF. This step exposes many planes in etched silicon surface (by RIE) and a short anisotropic etching step in KOH causes the structures to be released.

Cantilever beams were also fabricated using surface micromachining technique. For this purpose, RF sputtered silicon dioxide as a structural material and weakly-crystallized ZnO as sacrificial layer were used. A two-mask process was followed for this purpose (Bhatt & Chandra 2007a). Zinc oxide film of 4-μm thickness was deposited from ZnO target on (100) silicon wafer using the same RF sputtering system. The zinc oxide is then patterned using photolithography process. Special care was taken during photolithography of ZnO films and it is discussed in detail in our previous work (Bhatt *et al* 2005). It is a requirement that the etching of ZnO film during platform formation results in smooth gentle slope. This would lead to conformal step coverage of structural material layer in the subsequent steps. Etching in BHF at room temperature was found to produce a gentle slope ($\sim 45^\circ$) in the etched platform of ZnO (Bhatt *et al* 2005). After this step, the silicon dioxide of two-micron thickness was deposited at 300 W RF power and 5 mTorr pressure. Due to the 'steps' on the surface of wafer,

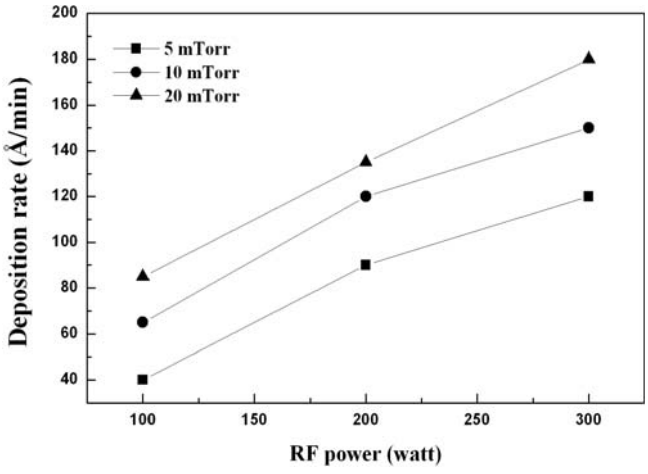


Figure 1. Deposition rate of SiO_2 as a function of RF power at different sputtering pressures.

normal photoresist was not suitable for step coverage during pattering. To overcome this problem, a thick photoresist coating (STR-1045, high viscosity) was used. The next masking step is carried out to define the micro-cantilever beam and the silicon dioxide was etched in BHF. Finally, the sacrificial layer is removed in 1% HCl and cantilever beam is completely released.

Completely planarized microstructures were also fabricated using a combination of surface and bulk micromaching process (SBM) involving chemical mechanical planarizations (CMP) step. The microstructures such as micro-cantilever beam, diaphragm supported on hinges and micro-bridge were fabricated by SBM technology using two-mask processes (Bhatt & Chandra 2007c). The sacrificial layer (ZnO film) is etched in 1% HCl for releasing the microstructures.

3. Results and discussion

Figure 1 shows the deposition rate of SiO_2 films as a function of sputtering power at 5, 10 and 20 mTorr sputtering pressure. The sputtering was done in diode mode. These deposition rates were measured on the centre of the wafer. Near the periphery of the wafer, the deposition rate falls by 10–15%. As expected, the deposition rate strongly depends on the RF power and increases with increasing power.

As mentioned earlier, the substrate temperature is important during deposition process. The wafer surface temperature as a function of deposition time is shown in figure 2. It is observed that an equilibrium temperature is reached after about 20 minutes from the starting of sputtering. The maximum temperature measured was about 280°C 160°C and 75°C for 300, 200 and 100 W RF power respectively. Substrate heating during sputtered deposition involves four basic independent heating processes namely: heat of condensation, sputtered atom kinetic energy, plasma radiation and cathode reflected neutrals (Thornton 1978).

Figure 3 shows the residual stress as a function of sputtering pressure. The films were deposited at 5, 10, and 20 mTorr at 300 W RF power. As seen from the figure, the stress of the films is compressive in the entire pressure range investigated, and increases gradually from approximately 90 to 300 MPa as the pressure is changed from 5 to 20 mTorr. The total stress in the film consists of the contribution from both intrinsic stress and thermal stress. The thermal

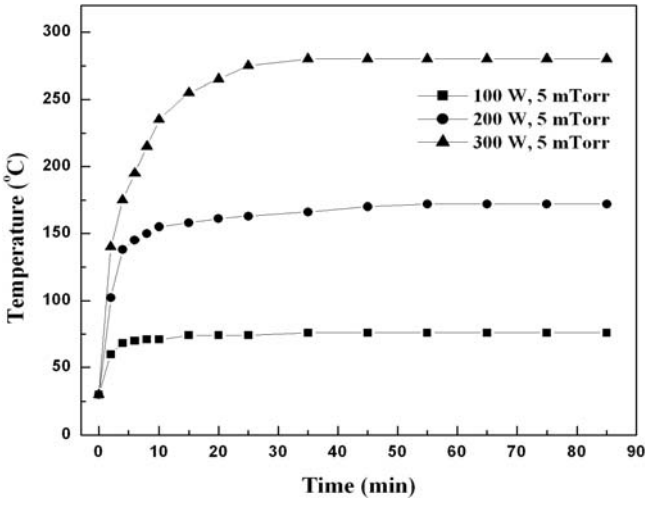


Figure 2. Variation of wafer temperature with sputtering time for different RF power at 5 mTorr pressure.

stress results from the mismatch of the thermal expansion coefficients of the film and the substrate as the sample cools from deposition temperature to room temperature. The maximum temperature rise during sputtering was 280°C with the applied power of 300 W, as shown in figure 2. Since all the films were deposited at 300 W RF power, it is safe to presume that rise in temperature remains constant during the deposition for all the films. Thus, we may assume that the thermal stress value in all the samples will remain identical and only intrinsic stress will change depending on the deposition parameters. Thus, the change in measured stress, as illustrated in figure 3 is largely due to varying intrinsic stress present in the film. The intrinsic stress is, however, different for samples prepared at different sputtering pressure. From the figure, it is clear that the intrinsic stress decreases with decreasing sputtering pressure and

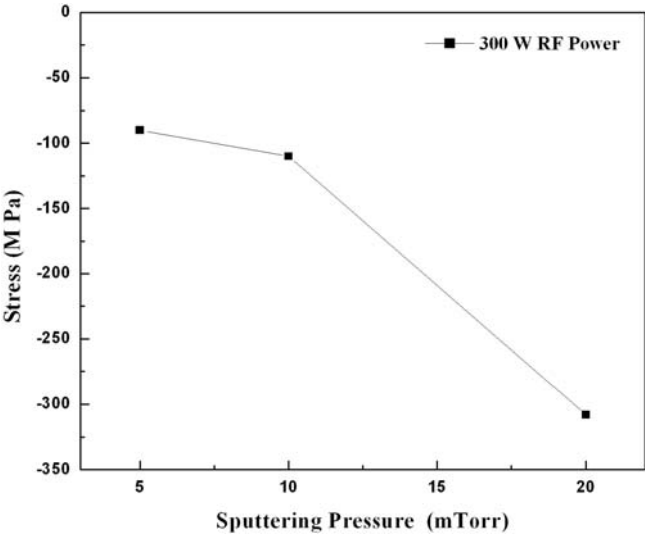
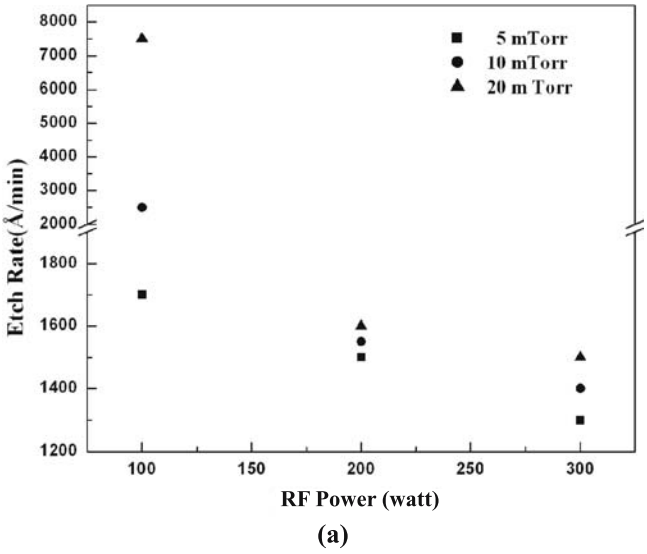


Figure 3. Dependence of residual stress in the SiO_2 films on the sputtering pressure.

this can be explained as follows: at lower deposition rate (at lower pressure, figure 1), the adatoms have sufficient time to migrate to low energy position before they are trapped by subsequently deposited atoms. This apparently results in a lower intrinsic stress. On the other hand, at higher deposition rate (at higher pressure, figure 1), the adatoms are trapped in their arrival position by subsequent incoming atoms. Detail study of stress in RF sputtered SiO_2 films are presented in our other work (Bhatt *et al* 2007b).

Figures 4a–c show the effect of sputtering parameters on etching characteristic of RF sputtered SiO_2 film in BHF, EPW and KOH respectively. The results of thermally grown SiO_2 are included for the purpose of comparison. The sputtered films produced at a low RF power (100 W) showed much higher etching rate compared to that of thermal oxide (figure 4a). However, the etch rate for the films sputtered at 300 watt RF power and low



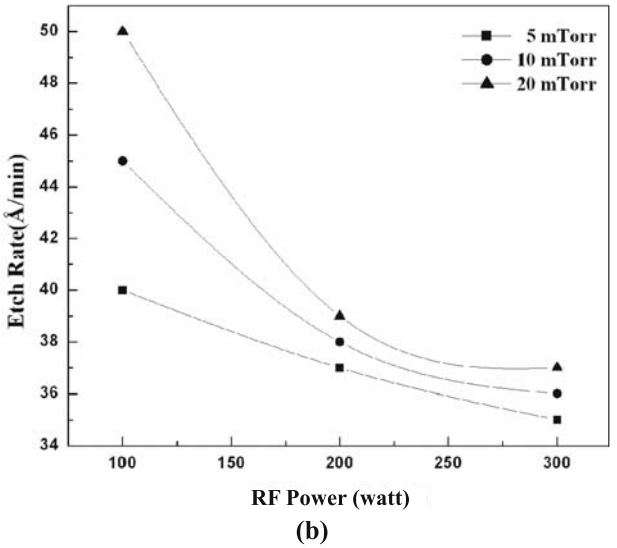
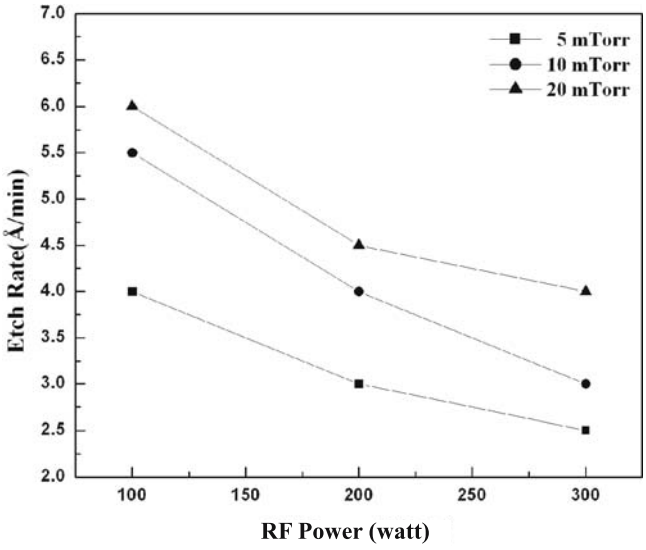


Figure 4. Effect of sputtering parameters (RF power and pressure) on etch rate of RF sputtered SiO_2 films in **(a)** BHF, **(b)** KOH (40% w/w, 70°C), **(c)** EPW. The etch rates of thermally grown SiO_2 are: (a) 1100Å/min, (b) 30Å/min and (c) 2Å/min for the corresponding solutions (Beadle *et al* 1985; Seidel *et al* 1990; Xian-Ping *et al* 1986).



(c)

Figure 4. (Continued).

pressure (5 mTorr in the present work) is comparable to that of the thermally grown silicon dioxide films (Beadle *et al* 1985).

As discussed earlier in § 2·3 (Microstructures fabrication), we aim to explore the RF sputtered silicon dioxide film as a structural layer material for fabricating MEMS structures. For this purpose, it is a requirement that the structural layer (RF sputtered SiO_2) should not be affected by EPW and KOH, which are used as a silicon anisotropic etchant in bulk micromachining process. The etch rates in KOH for sputtered SiO_2 as a function of RF power at different sputtering pressures are shown in figure 4b. From the figure, it can be inferred that the etch rate of the film deposited at lower RF power (100 W) is higher than the corresponding value for thermal oxide. However, the film deposited at higher RF power (300 W) shows almost same etch rate as that of thermal oxide (Seidel *et al* 1990).

Figure 4c shows the etch rate of RF sputtered SiO_2 in EDP as a function of RF power at different sputtering pressure. It is evident from the figure that the film deposited at higher power and lower pressure (300 W and 5 mTorr), has a etch rate very similar to that of the thermal oxide (Xian-Ping *et al* 1986).

Figure 5 shows the scanning electron microscopy (SEM) micrograph of an array of silicon dioxide cantilever beams (100 micron width and varying length) fabricated by bulk micromachining process. The beams are straight which confirms that these are free of any stress gradient.

SEM photograph of RF sputtered silicon dioxide micro-bridge, formed by above mentioned process is shown in figure 6. The film deposited at 300 W RF power at 5 mTorr pressure shows compressive stress of -92 MPa (figure 3). The buckling of micro-bridge further confirms the compressive nature of the stress in the SiO_2 film.

Figure 7 shows the SEM photograph of RF sputtered SiO_2 micro-cantilever beam fabricated by surface micromachining process using ZnO as sacrificial layer. This figure illustrates that RF sputtered ZnO can be used as sacrificial layer with RF sputtered SiO_2 as structural material in conventional surface micromachining process.

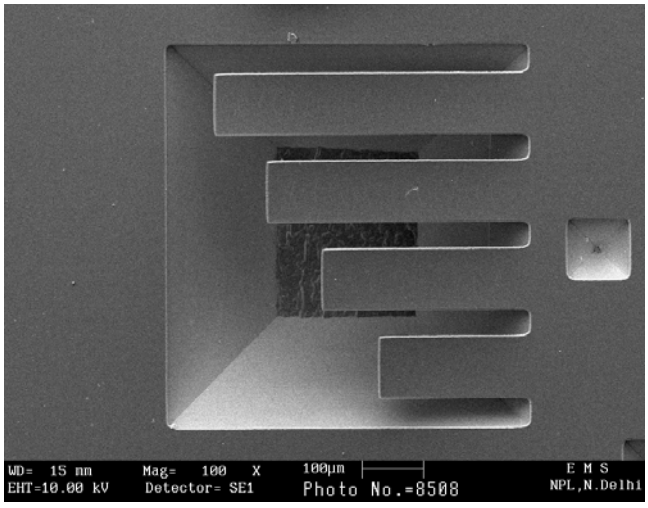


Figure 5. SEM photograph of an array of RF sputtered silicon dioxide micro-cantilever beams formed using bulk micromachining process.

Figures 8a–d show SEM photographs of the completely released planar diagonally supported micro-bridge, micro-cantilever beam, diaphragm supported on hinges and micro-cantilever beam with wider tip respectively, which are fabricated by the SBM technique.

The deposition rate for the silicon nitride under similar sputtering conditions is illustrated in figure 9. The stress measured as a function of sputtering pressure at 300 W power is shown in figure 10. The stress was observed to be compressive and decreases from 1360 to 390 MPa as the sputtering pressure is changed from 5 to 20 mTorr. At lower sputtering pressure, the inelastic collision probability between plasma particles decreases, enhancing the peening effects of the energetic plasma particles. Therefore, the intrinsic stress increases with decreasing pressure.

The substrate temperature during the sputter-deposition process is known to have a pronounced effect on its crystallographic properties of ZnO (Ondo-Ndong *et al* 2003; Lu *et al*

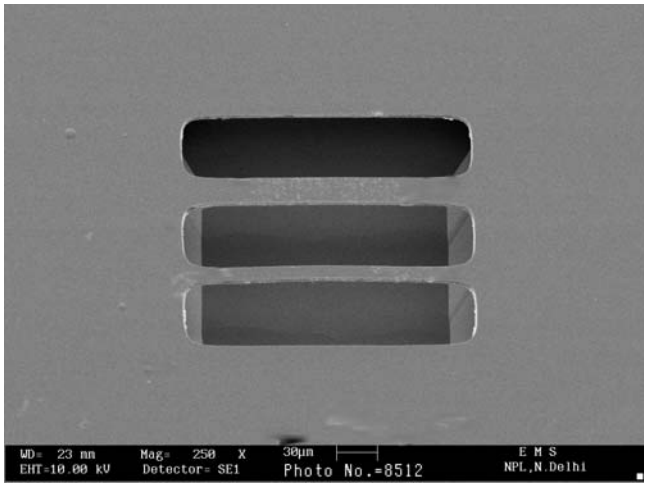


Figure 6. SEM photograph of RF sputtered SiO_2 micro-bridge formed using bulk micromachining process.

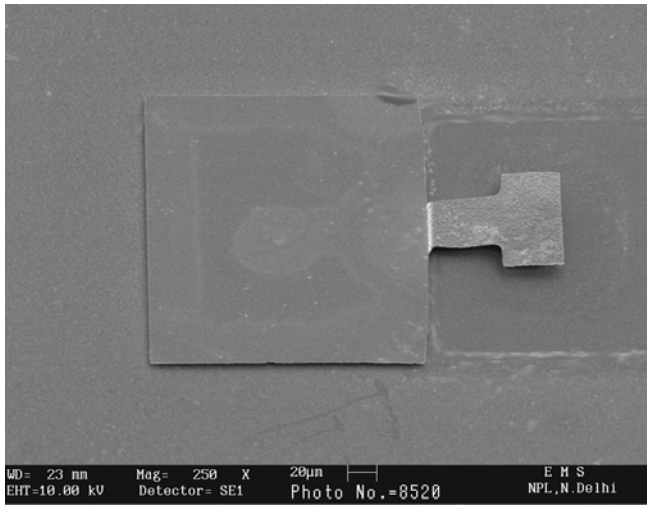


Figure 7. SEM photograph of RF sputtered SiO_2 micro-cantilever beam fabricated by surface micro-machining process.

2001). It is well known that, during the sputtering process, the substrate temperature rises (Maissel & Glang 1970). We have investigated whether this self-heating phenomenon can be exploited to obtain *c*-axis oriented ZnO growth. Figure 11 shows the change in substrate temperature with time during the sputtering (RF power: 100 W, target-substrate distance: 40, 50, and 60 mm, magnetron target) when no external heating was provided. The temperature rises gradually and stabilizes in about 50 min. The maximum substrate temperature is a function

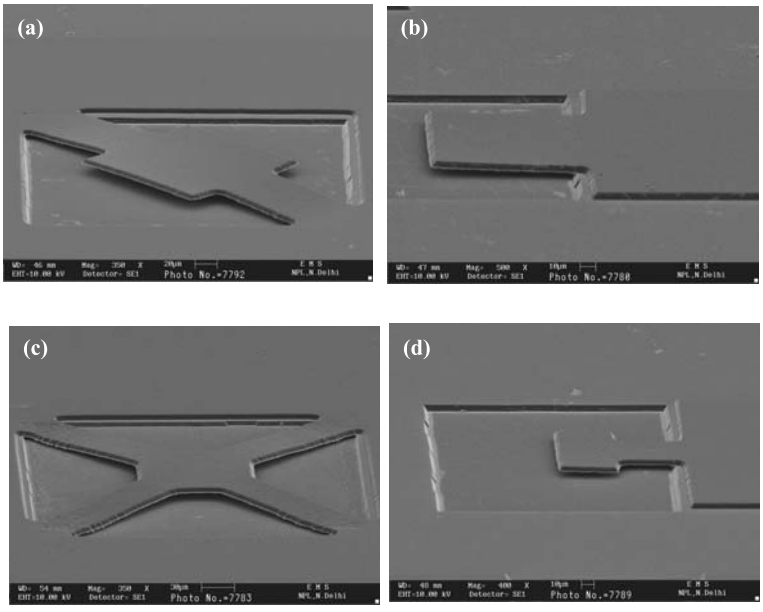


Figure 8. SEM photographs of the completely released planar structures: **(a)** diagonally supported micro-bridge, **(b)** micro-cantilever beam, **(c)** diaphragm supported on hinges and **(d)** micro-cantilever beam with wider tip.

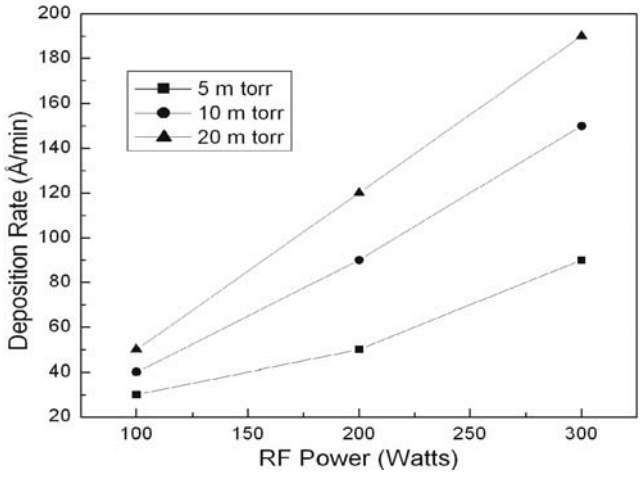


Figure 9. Deposition rate for silicon nitride versus RF power at different sputtering pressures.

of target-to-substrate spacing. For the 40, 50 and 60 mm spacing, its value is 138, 110, and 90°C respectively.

Figure 12 shows the XRD pattern of ZnO films prepared on a variety of substrates such as Si (100), p^+-Si (heavily boron diffused), SiO_2/Si, glass, Cu/Si, Al/Si, $Au/Cr/SiO_2/Si$ and $Pt/Ti/SiO_2/Si$. These films were prepared using optimized sputtering parameters (100 watt RF power, magnetron target, 50 mm target to substrate spacing, 10 mtorr sputtering pressure, and mixture of argon–oxygen 1:1, no external substrate heating). The deposition rate under these conditions was measured to be about 167 Å/min. It can be seen that the strong (002) peak corresponding to *c*-axis orientation appeared for all the films. The additional peaks were identified to be from the substrate. The intensities of the (002) peaks were not much different for these films. However, the FWHM varied from 0·3° to 0·72° and were minimum ($\sim$ 0·3°) in the case of glass, Cu/Si and $Pt/Ti/SiO_2/Si$ substrates. The 2θ values of (002) peak of the

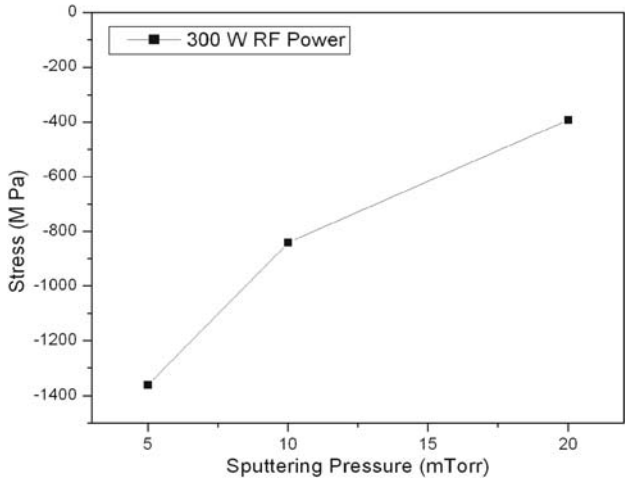


Figure 10. Variation in residual stress in silicon nitride films as a function of sputtering pressure.

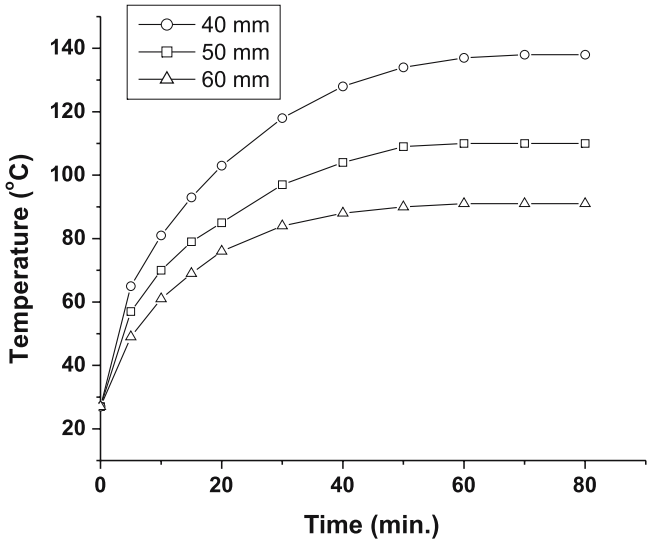


Figure 11. Change in substrate temperature with time during the sputtering at different target-to-substrate spacing (RF power: 100 W). No external heating was provided.

films prepared on Cu/Si and Pt/Ti/SiO_2/Si substrates were found to be 34·391 and 34·407° respectively, which are closer to the value corresponding to the bulk ZnO (34·44°). This indicates that these films have lower tensile stress than the films prepared on other substrates. However, further experiments are needed to confirm this. The location of (002) peaks and FWHM values for different substrates are summarized in table 1.

The surface morphology was investigated for the as-deposited and annealed ZnO films which were prepared using optimized sputtering parameters for *c*-axis orientation. Figure 13 shows the SEM images of these films. It appears from the figure that the grains of the as-deposited film are uniformly distributed with nearly similar size. This is further confirmed by AFM measurements, shown in figure 14. The average grain size calculated from these measurements was found to be 147 and 411 nm for as-deposited and annealed films respectively.

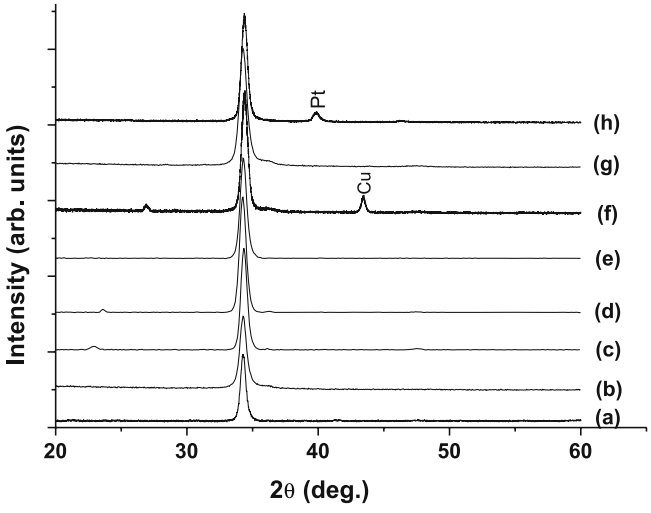


Figure 12. XRD pattern of ZnO films prepared using optimized sputtering parameters on various substrates: (a) glass, (b) Si (100), (c) SiO_2/Si, (d) p^+-Si, (e) Au/Cr/SiO_2/Si, (f) Cu/Si, (g) Al/Si, and (h) Pt/Ti/SiO_2/Si.

Table 1. The (002) peak positions and FWHM of ZnO films prepared on different substrates using optimized deposition parameters.

Substrate	Si (100)	p^+-Si (heavily boron diffused)	SiO_2/Si	Glass	Cu/Si	Al/Si	Au/Cr/ SiO_2/Si	Pt/Ti/ SiO_2/Si
(002) peak position, $2\theta(^\circ)$	34·283	34·252	34·337	34·275	34·391	34·268	34·296	34·407
FWHM(°)	0·492	0·612	0·541	0·312	0·315	0·72	0·66	0·306

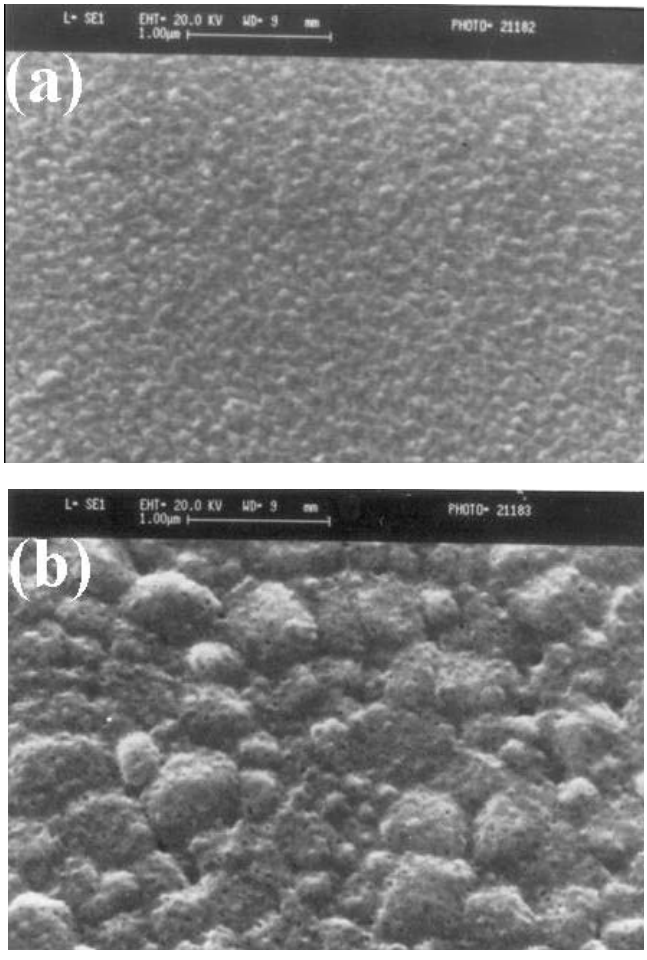


Figure 13. SEM of ZnO films **(a)** as deposited and **(b)** annealed at 900°C for 1 hr. The ZnO films were prepared at 100 W without external substrate heating in Ar + O_2.

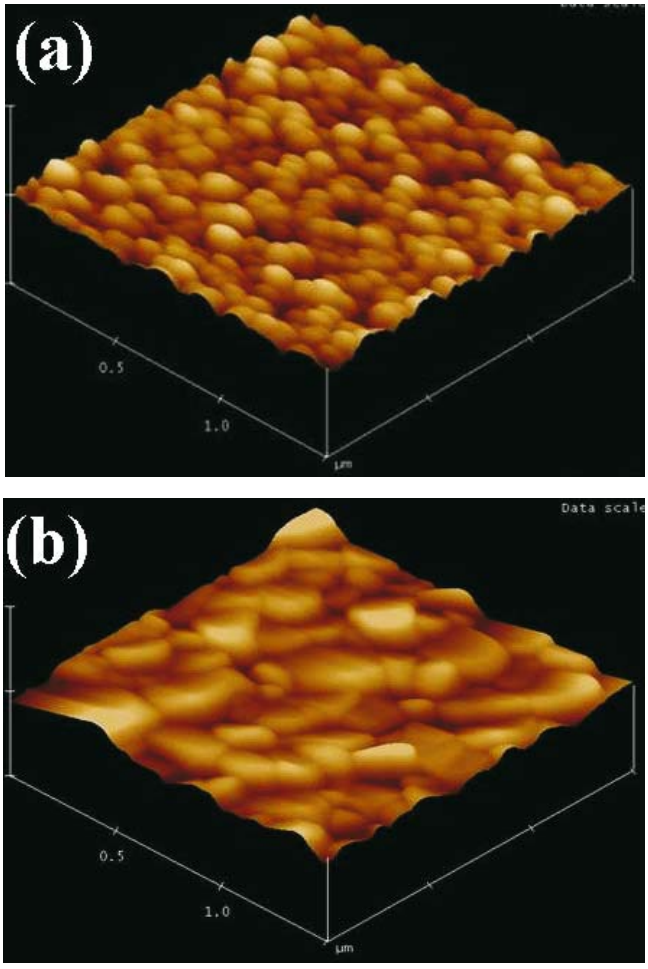


Figure 14. 3-D AFM of ZnO films **(a)** as deposited and **(b)** annealed at 900°C for 1 hr. The ZnO films were prepared at 100 W without external substrate heating in $Ar + O_2$.

Although the average grain size increased after annealing, the non-uniformity in the grain size also increased. The mean roughness was found to be 9·679 and 4·865 nm for as-deposited and annealed films respectively. These studies confirm that smooth ZnO films with uniform grain distribution can be prepared without external substrate heating. The annealing at 900°C for 1 hr enhances the grain size and smoothness of the film.

The DC resistivity of the films, calculated from I–V measurements, was found to be in the range of 10^{11}–$10^{12}\Omega$-cm at low electric fields ($\sim$ 10 kV/cm). This is much higher than the reported values (Chu *et al* 2003; Mitsuyu *et al* 1980).

4. Conclusions

The possibility of preparing dielectric films of silicon dioxide and silicon nitride by RF sputtering process for MEMS was explored. The characteristics of the films, which have bearing on MEMS fabrication, were investigated. For the films to be used as structural layer, the etching properties in KOH, BHF and EPW were investigated. The stress in the film was evaluated

as a function of deposition parameters to obtain low-stress films. The microstructures were realized using bulk micromachining, surface micromachining and surface- bulk micromachining techniques. Highly *c*-axis oriented ZnO films having high dc resistivity were prepared without external substrate heating on a variety of substrates. This has potential applications in MEMS. It is concluded that the RF sputtering process is a viable method of preparing films at relatively low temperatures for fast prototyping of MEMS.

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