

Design and development of high voltage high power operational amplifier using thick film technology

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Abstract. Applications of power operational amplifiers (opamps) are increasing day by day in the industry as they are used in audio amplifiers, Piezo transducer systems and the electron deflection systems. Power operational amplifiers have all the features of a general purpose opamp except the additional power handling capability. The power handling feature can be achieved using an external circuitry around a regular opamp. Normally power opamps can deliver current more than 50 mA and can operate on the supply voltage more than ± 25 V. This paper gives the details of one of the power opamps developed to drive the Piezo Actuators for Active Vibration Control (AVC) of aircraft/aerospace structures. The designed power opamp will work on ± 200 V supply voltage and can deliver 200 mA current.

Keywords. Power booster; power operational amplifier; thermal resistance.

1. Introduction

Power amplifier is a module which will repeat the weak input signal with magnification. The main objective of power amplifier is to meet the goals of repetition and amplification of input signal. Design high voltage power amplifiers to meet the applications which demand high voltage with very low harmonic distortion is a difficult task. There are different ways to address this challenge, a) Designing a discrete power opamp with high voltage devices like FETS, Transistors. b) Design a power booster around a monolithic opamp which can boost the voltage and current handling capabilities. This paper uses the second approach to build the high voltage opamp. These power boosters are placed in the feedback path of the opamp, retaining IC's stable gain characteristics.

2. Amplifier theory

Amplifier design relies on feedback mechanism. Offsets that accumulate in different stages of amplifier are corrected by feedback mechanism. Negative feedback will improve harmonic

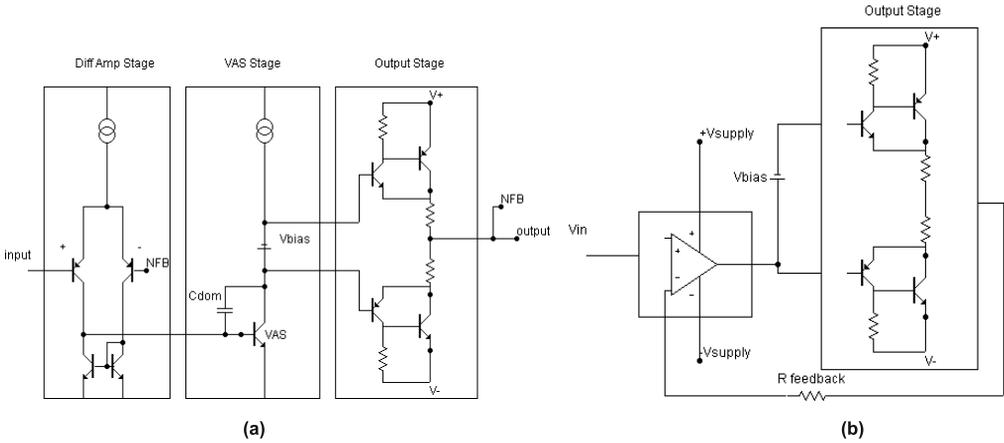


Figure 1. (a) Power opamp with discrete components having three stages. (b) Power opamp with Power Booster and input stage with opamp.

distortion, decreases output impedance, and increases amplifier stability. If no feedback is applied, DC drift would saturate an amplifier, and there would be no way to correct for offsets accumulating in amplifier blocks. More precisely, elementary feedback theory states that the factor of improvement from negative feedback is the open loop gain multiplied by the attenuation in the feedback network (i.e. the inverse of the closed loop gain). This improvement ratio also reduces crossover distortion in output stages of an amplifier.

2.1 Three stage amplifier

The three stage approach as shown in the figure 1a covers Differential Amplifier Stage, Voltage Amplification Stage (VAS), and Output Stage (MIT EDU 2002). The first two stages built from discrete transistors can replace the integrated opamp stage and allow a higher voltage swing. The first stage converts a differential voltage to a current output. The differential amplifier stage simulates an opamp (and is often used in opamp circuits).

The differential amplifier standard equation,

$$V_{out} = \text{Gain} \times (V^+ - V^-). \tag{1}$$

The second stage is a common emitter (CE) amplifier that takes a current signal and produces an amplified voltage. The final output stage, consisting of pre-driver and output transistors, is a unity-voltage-gain stage with current levels amplified. The main advantage of the three-stage model is modularity. The differential amplifier block, VAS, and output stage can be tested separately for the parameters like gain and stability. The main disadvantage of this approach is cost and availability of high voltage devices in chip form.

2.2 Amplifier with opamp input stage

The second approach as shown in figure 1b builds the power booster or adding a second stage to enhance the voltage and current handling capabilities around a normal opamp. The opamp provides voltage gain and a way to generate an error signal between its two input pins for feedback. An output stage must still amplify current levels. Output booster stage is placed

Table 1. Specifications of the designed high voltage opamp.

Parameter	Test conditions	Min.	Typ	Max.
Offset voltage	At $T_c = 25^\circ\text{C}$		$\pm 3\text{ mV}$	$\pm 5\text{ mV}$
Supply voltage		$\pm 100\text{ V}$	$\pm 180\text{ V}$	$\pm 200\text{ V}$
Quiescent current	At $T_c = 25^\circ\text{C}$		$\pm 25\text{ mA}$	$\pm 50\text{ mA}$
Power band width	At $T_c = 25^\circ\text{C}$ and $C_l = 1\text{ nF}$	13 KHz	20 KHz	22 KHz
Output voltage swing	At $T_c = 25^\circ\text{C}$ and $I_o = 25\text{ mA}$		$ \pm V_s - 10\text{ V}$	
Capacitive load				1.5 nF
Harmonic distortion			< 1%	
Thermal resistance Junction to case			2.7°C/W	3.5°C/W

within the feedback loop of the opamp so that the stability and gain characteristics of the amplifier are retained (Jim Williams 1986). Because the booster is a gain stage with its own dynamic characteristics, the challenges of phase shift, oscillation, and frequency response cannot be ignored if the booster and amplifier are to work together well. This approach is chosen because a) Opamps are available for supply rails of $\pm 45\text{ V}$. b) Design cycle time is less. c) Low cost.

3. Design approach

Boosting the voltage and current capabilities of the normal opamp, needs careful selection of the basic opamp to meet the desired specifications like open loop gain, slew rate, etc. of the power opamp. Second stage is the biasing stage to the output stage which provides sufficient DC gain so that out put device can swing at the maximum voltage and also ensures that output stage is biased as class A/B. Third stage is the buffer stage which can provide the proper current gain so that amplifier can provide the maximum voltage swing. The specifications of the designed power opamp are given in table 1. The schematic for the opamp designed is given in figure 2.

3.1 Input opamp

OPA445 (U2) is a FET based monolithic operational amplifier with a unity gain bandwidth of 4 MHz and capable of operation from power supplies up to $\pm 45\text{ V}$ and output currents of 15 mA. It is useful in a wide variety of applications requiring high output voltage or large common-mode voltage swings. The OPA445's high slew rate provides wide power bandwidth response, which is often required for high voltage applications. FET input circuitry allows the use of high-impedance feedback networks, thus minimizing their output loading effects. It operates from -55°C to $+125^\circ\text{C}$. This is taken as the prime opamp and the booster is built around it.

3.2 Output biasing stage

The biasing stage is built using high voltage MOSFETs IRF340 (M11) and IRF9310 (M25). This stage provides a DC gain of 14 with a local gain stage R3, R6 resistor network allowing the output MOSFETs to swing at $\pm 200\text{ V}$. Biasing the MOSFET based output stage for class A/B operation cannot be done with the traditional diodes or V_{be} multiplier of the BJT.

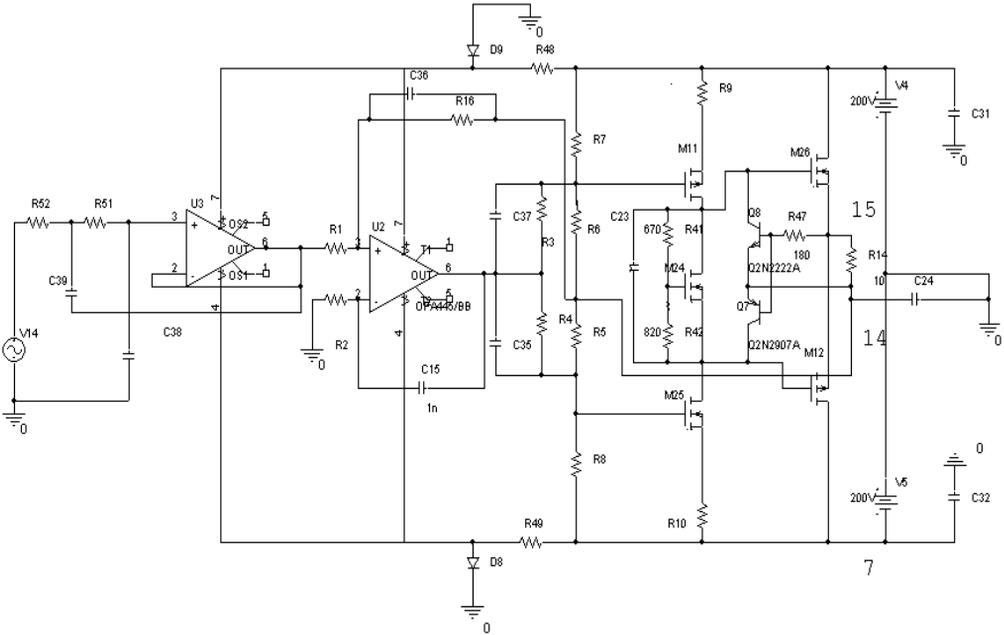


Figure 2. Schematic of the designed power opamp.

These schemes cannot properly compensate MOSFET gate voltage temperature coefficients. Thermal runaway can occur if the bias source’s temperature coefficient and MOSFETs V_{gs} threshold donot match (Jerry Steele & Dennis Eddlemon 1993). Using V_{gs} multiplier we can overcome this problem. V_{gs} multiplier reduces the distortion and improves the linearity. The design of V_{gs} multiplier can only be achieved with experimentation on actual working amplifier. The ratio of R41 and R42 in figure 3 is adjusted to provide the desired quiescent current.

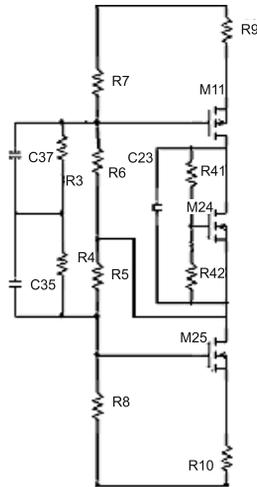


Figure 3. Output biasing stage.

3.3 Output stage

The MOSFET based output stage is used to avoid the second break down (SOA) limitations of the amplifier. And the output current limit can be set by varying the current limiting resistor R14. Frequency compensation will be done with the C15 capacitor at the OPA445 opamp stage. Since circuit operates in inverting mode so feed back will be given to the non inverting input of OPA445. The over all gain is set for 20 with the feedback network of resistors R16 and R1.

A pre unity gain low pass filter also included in the designed power opamp with a cut-off frequency of 30 KHz. This is basically to filter out the high frequency noise in the input signal due to its application of driving the Piezo Actuator. The capacitive loads and high gain will cause the oscillations. The closed loop gain and proper power supply decoupling will avoid the oscillations.

4. Simulation results

Spice simulation is done for the circuit and results are given in figures 4a–c. The simulation results show the maximum output swing of ± 185 V and the bandwidth of 25 KHz. The gain characteristics are also shown here.

5. Construction

The power opamp is realized in 16 pin Single in Line (SIP) package. The thick film hybrid power opamp, using chip passive components, semiconductor bare dice minimizes the size while increasing the reliability. Resistors and conductors are printed on the Alumina (Al_2O_3) substrate. Thick film resistors are reliable and stable. All the conductor tracks are realized with Silver palladium (PdAg) and covered with glass coating. Since this package is required to handle larger powers, the heat dissipated inside the package has to be drained out to the heat sink through a least thermal resistance path. Hence MOSFET bare dice are attached using solder attach technique. Other low power dissipating components and passive components are attached to the substrate using silver epoxy. The substrate is attached to the copper base using solder attach. The interconnections are done using 2 mil aluminum wire bonds on the power chips and 1 mil gold wire bonds on the low power connections. The ceramic substrate is encapsulated with the ceramic cap to provide the hermiticity.

The over all dimensions of the circuit is $40.6 \text{ mm} \times 27.18 \text{ mm} \times 7.6 \text{ mm}$. Figure 5 gives the pictorial view of the power opamp developed.

6. Thermal design

Theoretical thermal resistance (θ_{jc}) from junction to case is calculated and the same is evaluated experimentally using the 45° heat flow model which is shown in figure 6. Table 2 shows the thermal resistance of each interface from semiconductor junction to the package case. The basic formula for thermal resistance considering single chip 45° heat flow mode (Jerry Sergent & Al Krum 1998) is

$$\theta = \frac{1}{2K(b-a)} \ln \left(\frac{b}{a} \right) \left(\frac{a+2x}{b+2x} \right), \quad (2)$$

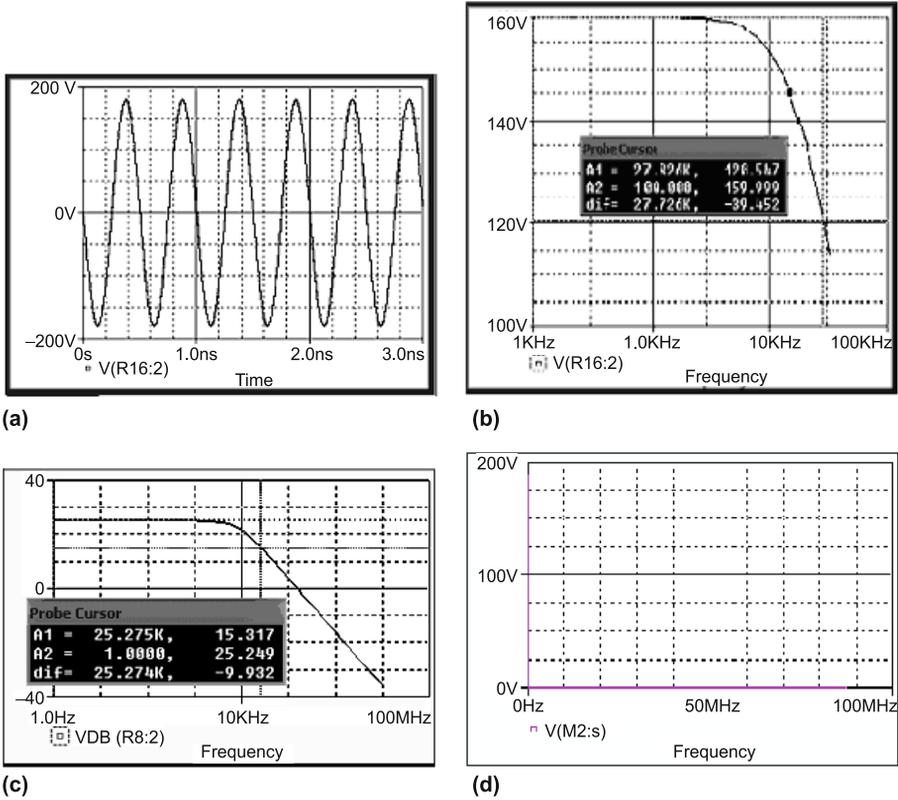


Figure 4. (a) Power opamp output. (b) Power opamp frequency response. (c) Gain plot of power opamp. (d) FFT plot of power opamp.

where: θ is thermal resistance in $^{\circ}\text{C}/\text{W}$, a is length of the die in inch, b is width of the die in inch, x is thickness of the die in inch, K is the thermal conductivity in $\text{W}/^{\circ}\text{C}\text{-inch}$.

The internal power dissipation of the opamp is dependent on the supply voltage and quiescent current. At maximum supply voltage of $\pm 200\text{ V}$ the power dissipation will be 20 W . Since the application is industrial the operating temperature range is -10°C to 85°C . With a power dissipation of 20 W the device junction temperature will rise by 50°C . So proper heat sinking is required to improve the reliability of the device.

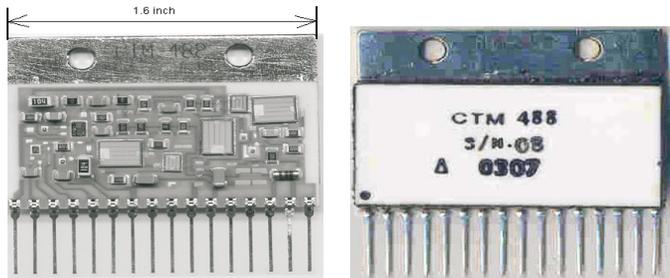


Figure 5. Pictures of developed power opamp.

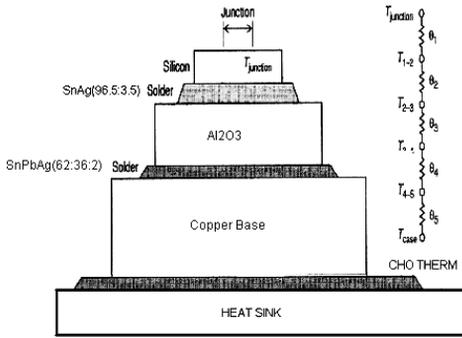


Figure 6. Thermal model of the power die.

7. Test results

The amplifier built is tested for all the electrical parameters like maximum output swing, linearity, power band width and harmonic distortion. Figures 7(a-c) and table 3 show the electrical test performance. The amplifier is successfully tested with a piezo actuator system. There is a good agreement between the simulation and the experimental results.

8. Conclusion

The power opamp designed and developed had achieved all the intended specifications and been successfully packaged using thick film power hybrid technique.

Table 2. θ_{jc} from die to package.

θ_1	0.4894°C/W
θ_2	0.0932°C/W
θ_3	1.6640°C/W
θ_4	0.0877°C/W
θ_5	0.1358°C/W
θ_{JC}	2.4700°C/W

Table 3. Test results of high voltage opamp.

Parameter	Test conditions	Expected	Measured
Offset voltage	At $T_c = 25^\circ\text{C}$	$\pm 3\text{ mV}$	$\pm 3.2\text{ mV}$
Quiescent current	At $T_c = 25^\circ\text{C}$	$\pm 25\text{ mA}$	$\pm 20\text{ mA}$
Power band width	At $T_c = 25^\circ\text{C}$ and $C_l = 1\text{ nF}$	20 KHz	25 KHz
Output voltage swing	At $T_c = 25^\circ\text{C}$ and $I_o = 25\text{ mA}$	$ \pm V_s - 10\text{ V}$	$ \pm V_s - 8\text{ V}$
Capacitive load		1 nF	2 nF
Thermal resistance		2.5°C/W	2.9°C/W
Junction to case			

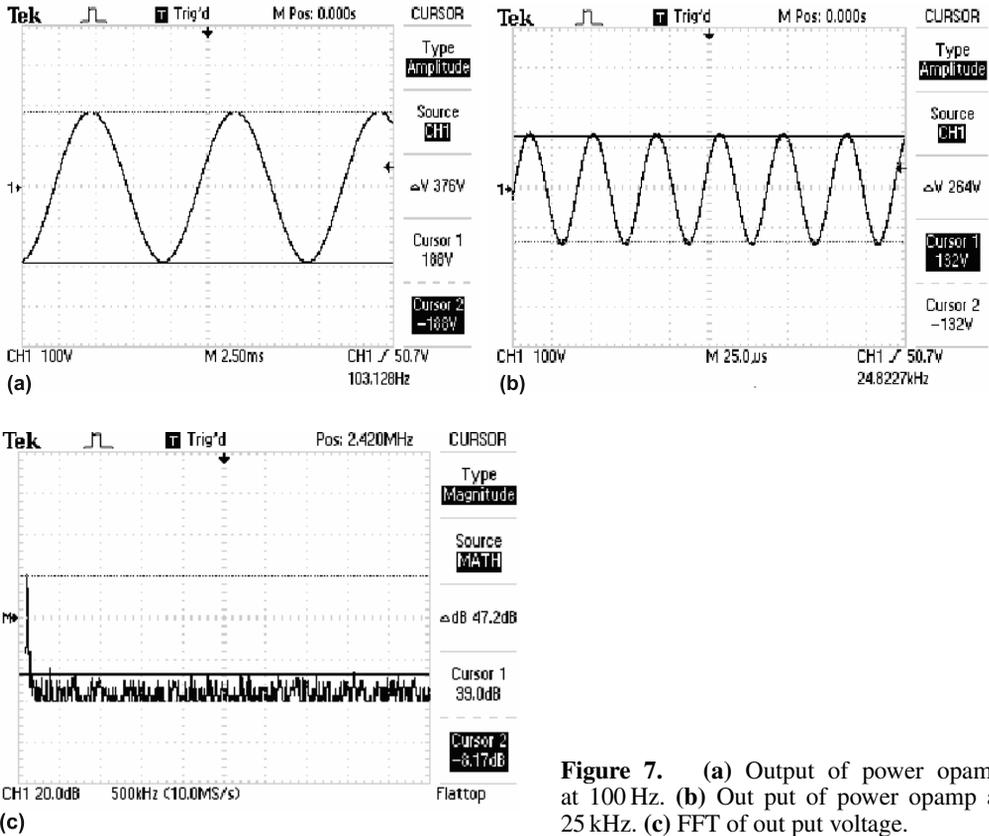


Figure 7. (a) Output of power opamp at 100 Hz. (b) Out put of power opamp at 25 kHz. (c) FFT of out put voltage.

The authors would like to thank Director, National Aerospace Laboratories for his encouragement and support. Thanks are also due to Head, Structures Division, National Aerospace Laboratories for giving an opportunity to carry out the high voltage operational amplifier design work. Authors would like to thank all the team members who are involved in this development. We thank Mr T Kanthimathinathan, for his guidance and to Mr. M V Appa Rao, Managing Director, Centum Electronics Ltd for the support.

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