Sādhanā Vol. 33, Part 5, October 2008, pp. 505–522. © Printed in India

Design and implementation of FPGA-based phase modulation control for series resonant inverters

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Abstract. Owing to the tremendous advances in the digital technology, and improved reliability and performance of the digital control mechanisms, this paper focuses on design and implementation of digital controller using FPGA-based circuit design approach. The digital controller proposed is designed for series resonant inverter used in DC–DC converter applications. Phase modulation technique is proposed for the realization of digital controller on FPGA. The Series Resonant Converter (SRC) is considered in this paper as a preferred converter topology for high power, high voltage power supplies. This paper studies the implementation of phase shift modulation technique using FPGA. The inverter designed, is IGBT based, and Zero Voltage Switching (ZVS) technique is implemented due to reduced stresses on devices and increased efficiency. The phase modulated series resonant inverters (PM-SRC) promotes ZVS operation when its switching frequency is greater than resonant frequency. The designed PM controller is realized using FPGA on which control algorithm and other features of a controller are developed. The series resonant inverter is built and tested for full load under open loop and closed loop conditions at a switching frequency of 20 kHz. The results are presented under varying load conditions. The simulation and the experimental results were found to match closely.

Keywords. Series resonant inverter; zero-voltage switching; phase modulation control; digital control; FPGA; limit cycle.

1. Introduction

Recent advances in modern power semiconductor device technologies have led to high utilization of power converters in a wide number of applications and have opened up a host of new converter topologies for many applications. Today, the power converter topology of choice for ac output applications is the dc/ac voltage source inverter. A key factor in reducing the size of reactive components used for filtering and energy storage, improving transient performance and meeting stringent harmonic specifications is the choice of switching frequency of the

inverter. In hard switched converters, switching losses occur during device turn-on and turn-off due to the existence of both voltage across, and current through the device over the transient period. These transient voltages and currents especially for high power applications, result in considerable losses in the devices and thus require significant derating of these devices, thus increasing the system cost. These stresses require significant device derating for switching frequencies in excess of 5–6 kHz, thus increasing system cost. In addition, IGBT losses are further increased at turn-on by the charge stored in the complementary switch's anti-parallel diode and at turn off by the energy trapped in the parasitic inductance of the IGBT package and device interconnections. Another issue is the transient on the inverter output voltage caused by IGBT switching, resulting in higher dv/dt. Also associated with the high switching speed is the electro-magnetic interference (EMI) that is generated at the inverter output. This EMI has frequency content spanning from 10 kHz to 30 MHz and is difficult to suppress.

In order to obtain additional system improvements, a fundamentally different approach is needed. One technique that is used is soft switching. Soft switching in dc/dc converters is simple to realize, because at any given operating point, power flow is unidirectional and the switching frequency is fixed for converter that is designed according to specification.

Advantages of soft switching and the use of zero voltage switching with IGBT power devices include:

- 100% power device utilization
- Low EMI which meet Mil-specs
- Enhanced robustness
- High power densities
- High switching frequencies
- High efficiencies.

The series resonant inverter (SRC) is a load resonant converter that finds application in DC–DC converters. The control of these inverters can be achieved either by changing the switching frequency with respect to the converter's resonant frequency or it can be achieved by varying the duty ratio. Such an SRC, having a fixed frequency of operation and varying duty ratio is called Phase Modulated Series Resonant Converter (PM-SRC).

Digital controllers offer many advantages over their analog counterparts: improved system reliability, flexibility, and ease of integration and optimization. Overall, they offer an elegant solution to many requirements in the power regulation specifications. All the components for the feedback loop are eliminated; the fine tuning of the components and selection according to design specification are replaced by software programming. The added capability of monitoring protection and prevention also increases the system reliability.

Although many closed loop control schemes were carried out using analog controllers, the flexibility rendered by analog controllers in terms of tuning of control system parameters to suit one's application is less as compared to its digital counterpart. Also, the overall loop gain is affected and hence the operating point of the series resonant inverter, when the controller components are affected due to aging, temperature, etc.

The use of software to change the controller functionality makes a system based on a digital controller very flexible. The digital controller offers the ability to add, eliminate or change any system parameter in order to meet new requirements, or to optimize the system. For example, the same DC–DC converter can be programmed to meet different specifications such as current or voltage requirements, without any hardware changes. Due to the ease of integration of monitoring systems (PC) with the digital controller, it also facilitates the ability to have better control of the system due to continuous monitoring.

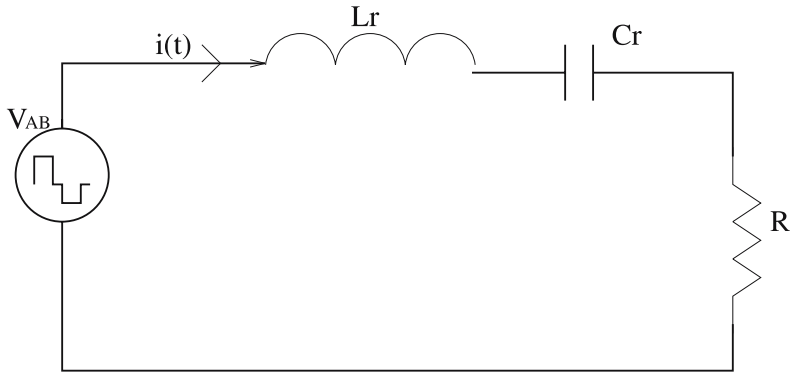

Figure 1. Resonant tank excited by Quasi square waveform.

In order to tightly regulate the output voltage and have control on the resonant current (which charges the output capacitor) during load variations, it may be necessary to implement multiple feedback control mechanisms to enhance the robustness and reliability of the system. Thus if the switching frequencies of the series resonant inverter is higher, of the order of hundreds of kilohertz or in megahertz range and multiple feedback controls such as outer voltage loop and inner current control are to be realized, where it becomes essential to sample the voltages and currents at a higher rate, using a DSP-based system may not be an optimum solution since most of the time, the resources of the die are utilized in data acquistion and processing and gating of signals and the available time and resource for actual computation of control algorithm is less (Shih-Liang Jung *et al* 1999).

Moreover, if the control requirements for a given application are more then, the DSP-based or any other higher end processor based system with limited resources become overloaded.

FPGA comprises of thousands of gate arrays which can be easily programmed to suit the one's application functionality. The logical cells are grouped together as a configurable logic blocks (CLB) and the interconnections between these logic gates are externally defined by programmable ROM. The ease of programmability of FPGA is the main reason for it to be used in digital systems (Shih-Liang Jung *et al* 1999).

The paper is organised as follows. Section 2 gives the PM-SRC operation, power converter specifications, modelling of the converter in SIMULINK using state-space techniques and digital controller design. Section 3 deals with the implementation process of the digital controller using FPGA. Section 4 discusses the experimental set-up and results. Conclusions are provided at the end.

2. PMSRC: Operation and modelling

The PM-SRC consists of a full bridge inverter feeding a quasi square voltage waveform to a series tank as shown in figure 1. The resonant tank consists of the resonant inductor (L_r) and the resonant Capacitor (C_r). The resonant inductor value is the sum of the transformer leakage inductance and external inductor present. Switching frequency (f_s) of the inverter is kept constant while the duty ratio (D) is varied using phase modulation technique. Therefore, the resonant tank is excited by a quasi-square waveform having frequency f_s and duty ratio D. The excitation results in a sinusoidal or near sinusoidal current in the resonant tank. The tank

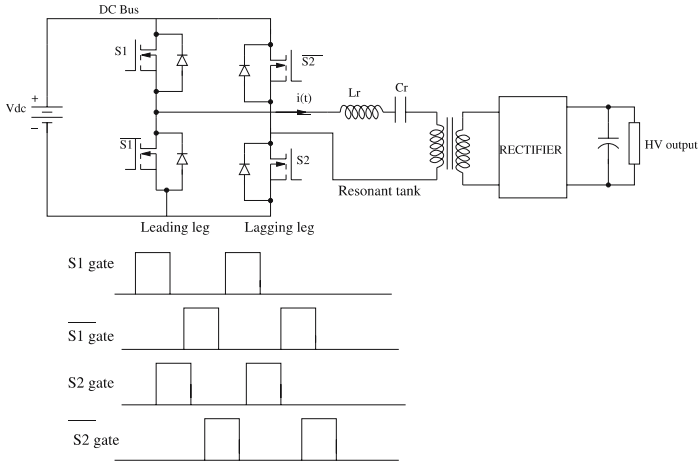

Figure 2. Schematic of the PM-SRC converter with gate pulses.

current $i(t)$ is rectified by a diode bridge rectifier and filtered using capacitive filter to get the required output voltage. The magnitude and wave shape of the resonant current depends on f_s, D and the load factor (Q) of the converter. Q is defined as the ratio of resonant tank characteristic impedance and the resistive load as seen from the resonant tank (Biju Nathan 1999).

The operating frequency (f_s) is generally close to the resonant frequency of the tank. Operation with $f_s < f_r$ is called sub resonant frequency operation. The input voltage then sees a net capacitive tank circuit. When $f_s > f_r$, the operation is termed super resonant frequency and the tank presents a net inductive circuit. The super resonant frequency operation facilitates ZVS for the inverter devices while the sub resonant frequency operation results in ZCS (Zero Current Switching).

For phase modulation, a full bridge inverter with fully controlled devices is required as shown in figure 2. Each device is switched at 50% duty ratio with the switching of the devices on the same leg being complementary. As shown in figure 2, conduction of switches on the leading leg of the inverter (S_1 and $\overline{S_1}$) is phase-shifted with respect to the conduction of switches on the lagging leg (S_2 and $\overline{S_2}$), resulting in the quasi-square input voltage. Here, the inverter containing the devices S_1 and $\overline{S_1}$ is termed as leading leg and the other is termed as lagging leg (Biju Nathan 1999).

One of the advantages of SRC is that the series capacitor eliminates the possible saturation of the HV transformer. The leakage inductance of the transformer is absorbed into the resonant tank circuit.This topology gives high efficiency over a wide range of load variations.

One of the critical design issues in any switched-mode power supply is achieving soft switching over the entire operating range of the converter. Though one of the positive features of SRC is that it enables soft switching, the soft switched operating regions are limited and depend on other parameter such as load. Proper design is therefore required to ensure soft switching over the defined operating range.

2.1 *Zero-voltage switching (ZVS)*

When the PM-SRC is operated such that its switching frequency is greater than the resonant frequency of the tank, zero-voltage turn-on of the inverter devices is possible because the

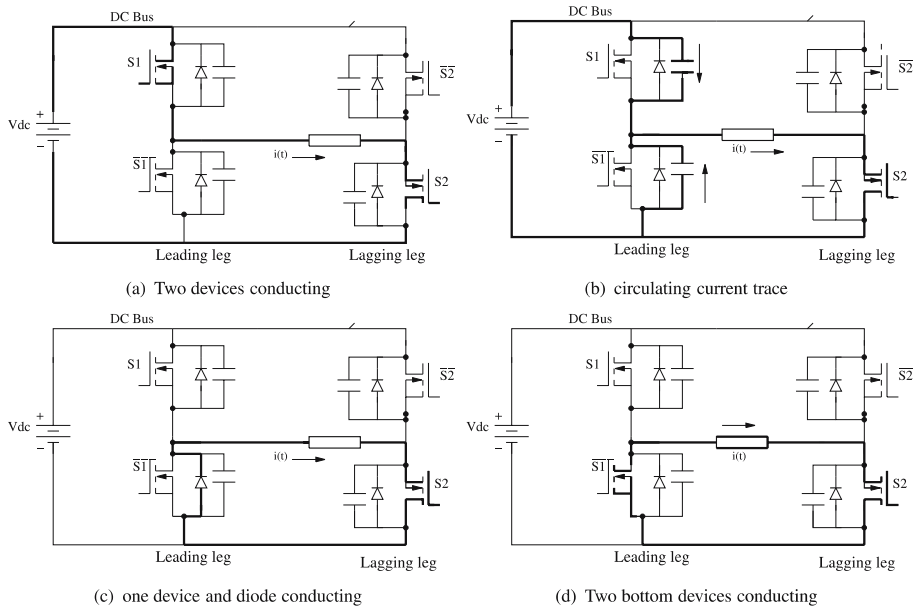

Figure 3. Zero-voltage turn-on sequence for $\overline{S_1}$ device. The current paths are shown in thickened lines.

effective impedance offered by the resonant tank is inductive. Tank current lags the input voltage. ZVS ensures the inherent output capacitance in the switching devices is discharged prior to switch turn-on, thus prevent turn-on losses and generated EMI. Figure 3 shows how ZVS is achieved for the switch $\overline{S_1}$.

When turning on a switch (figure 3), the snubber capacitor and the inherent S_1 output capacitance across that MOSFET must be completely discharged and clamped to nearly zero voltage. This is achieved if the other switch (S_1) on the same leg turns off with a positive current and by providing a time delay before giving the gate pulse to $\overline{S_1}$. During the time delay, the positive switch turn off current charges the capacitance across S_1 to V_{dc} and discharges the capacitance across $\overline{S_1}$ to zero. Subsequently, if the turn off current and delay time are large enough, the reverse diode across S_1 takes over the tank current. Thus the voltage across $\overline{S_1}$ is clamped to the diode forward drop. By applying gate pulse to $\overline{S_1}$ when its reverse diode is conducting, ZVS is ensured.

Thus the basic requirements for achieving ZVS and therefore low loss turn-on are:

- The device should turn off with a positive current flowing through it.
- The delay time and turn off current have to be large enough to completely charge/discharge the snubber capacitors and subsequent turn on of the reverse diode for conduction.
- The delay time has to be small enough to prevent the tank current from reversing before the switch turns on.

As the snubber capacitors are discharged by the load current prior to any switch turn on, there is no loss associated with it. Therefore, turn on is also nearly lossless. The primary advantage of the PM-SRC is the constant switching frequency. Besides optimum design of components, it can be synchronised with an external clock; The converter is short circuit proof if operated away from the resonant frequency. The disadvantages include large peak tank current and

voltages. The non-linear characteristics makes it difficult to analyse. The SRC does not take care of the transformer parasitic capacitance.

2.2 *Defining terms and assumptions*

The resonant tank has a natural frequency determined by the resonant capacitor and the resonant inductor.

f_s = switching frequency
f_r = Resonant frequency
P_{in} = Input power
P_{out} = Output power
η = efficiency
D = Duty ratio
J = Current density

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}}, \tag{1}$$

where L_r and C_r are resonant tank elements.

$$D = \frac{T_{on}}{\frac{T_s}{2}}, \tag{2}$$

where T_s = Switching period.
V_{dc} = Supply voltage
V_o = Output voltage

$$M = gain = \frac{V_o}{V_{dc}}. \tag{3}$$

The parameter Z_c called the characteristic impedance of the tank is defined as

$$Z_c = \sqrt{\frac{L_r}{C_r}}. \tag{4}$$

For a converter with a load resistance R_{pri}, the load factor, Q is defined as

$$Q = \frac{Z_c}{R_{pri}} \tag{5}$$

$$R_{pri} = R_{load}/n^2. \tag{6}$$

R_{pri} is the load seen by the resonant tank and n is the transformer turns ratio.

Instantaneous tank current and resonant capacitor voltage are represented by $i(t)$ and $v(t)$ respectively.

2.2a *Normalization:* For simplifying the analysis and making the analysis results valid for a generic design method, all the parameters associated with the PM-SRC are normalized with respect to base values. Table 1 summarizes the variables and the corresponding base values used in the analysis.

Table 1. Normalized variables.

Variables	Base value
Voltage	Input DC voltage, V_{dc}
Resistance	Characteristic impedance Z_c
Frequency (f_s)	Resonant frequency ω_r
Current	$\frac{V_{dc}}{Z_c}$
Capacitance C_r	$\frac{1}{\omega_r Z_c}$
Inductance L_r	$\frac{Z_c}{\omega_r}$

2.2b *Assumptions:* All components are assumed to be ideal. The output capacitive filter is large enough to approximate it as a constant voltage source under steady state, as seen by the resonant tank. For simplifying the analysis, the transformer and rectifier are not included. Effects of magnetising inductance and transformer parasitic capacitance are omitted. It is assumed to be lossless. Duty ratio is varied from zero to one. V_{dc} is taken to be a constant throughout the analysis (Biju Nathan 1999).

2.2c *Specifications:* The specifications of the inverter that is tabulated below is based on the lab set-up which uses series resonant topology.

$$i = \frac{V_{AB}}{\sqrt{(\omega L_r - \frac{1}{\omega C_r})^2 + R_{pri}^2}} \tag{7}$$

$$P_{out} = i^2 R_{pri} \tag{8}$$

$$Gain\ M = \frac{V_o}{V_{AB}}. \tag{9}$$

Using the above equations and the normalized table, the values are calculated and the following table lists the parameters that are directly involved in selection of the operating point of the inverter.

Table 2. Specifications of the converter.

Parameters	Value
Input voltage	350 V *DC*
Output voltage	600 V
Switching frequency (f_S)	20 kHz
Output power	200 W
Converter voltage gain	0·706
Frequency ratio f_s/f_r	1·1
Load factor (Q)	5·263

Table 3. Tabulated values of inverter parameters (in pu).

Q	Voltage gain	Current	Power
14·2857	0·3443	4·9179	1·6930
11·1111	0·4264	4·7380	2·0204
9·0909	0·4992	4·5386	2·2659
7·6923	0·5628	4·3296	2·4369
6·6667	0·6178	4·1188	2·5447
5·8824	0·6650	3·9119	2·6015
5·2632	**0·7054**	**3·7127**	**2·6190**
4·7619	0·7399	3·5235	2·6072
4·3478	0·7695	3·3455	2·5743

From the table it can be inferred that the maximum power occurs for a Q value of 5·26 and its corresponding voltage gain of the inverter at this operating point is 0·706, which are highlighted.

2.3 *Modelling of PM-SRC*

To aid the analysis of the SRC, a simulation model based on the state-space technique is developed in Matlab. The principal task of the simulation model is to generate the time response of the state variables of the circuit, from some initial conditions in the state-space, based on the circuit parameters such as capacitor voltages and inductor currents, operating parameters such as switching frequency (f_s), and simulation parameters such as time-step, integration method used, etc. The model should faithfully represent the system under operation to the desired accuracy. There is usually trade-off between the amount of accuracy obtainable and the complexity of the model; the more accurate the model, the greater its degree of complexity.

The simulation model comprises of the inverter and the rectifier for the power stage, error amplifier and phase modulator for the control stage. The values of the state variables are monitored in real time simulation. The state variables are the resonant current, and the tank capacitor voltage, V_c, and the output DC voltage. From figure 1 the various state space equations governing the modelling of PM-SRC are given by

$$\begin{bmatrix} i^o \\ v_{cr}^o \end{bmatrix} = \begin{bmatrix} \frac{R}{L_r} & \frac{1}{C_r} \\ \frac{1}{C_r} & 0 \end{bmatrix} \begin{bmatrix} i \\ v_{cr} \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \end{bmatrix} V_{AB}. \tag{10}$$

The dynamic modelling of the continuous time system is obtained through open loop step response of the actual converter. Figure 4 shows the step response of the converter under no load and full load. For this, the phase modulator is fed with a two units step input and for this step change in modulation index, the change in the DC output voltage is observed. The ratio of output voltage change at steady state for a given input step change determines the gain of the converter. The response is approximated to be first order response (Biju Nathan 1999) and the plant function $G(s)$ on load is given by

$$G(s) = \frac{150}{1 + s2{\cdot}5 \times 10^{-3}}, \tag{11}$$

where 2·5 msec represents the time constant of the plant and the numerator denotes the steady state gain of the plant.

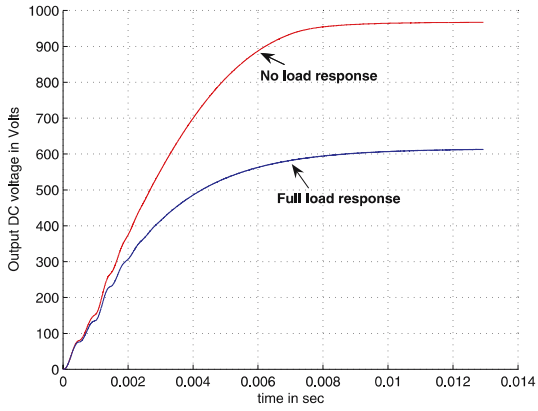

Figure 4. Open loop response of PM-SRC.

2.4 *Feedback loop design*

It is desirable that controller designed for any closed loop power converter meet the following criteria (Yao Wei *et al* 2005).

- The converter must be under regulation for a certain range of line and load variations.
- With a step load change,the settling time and peak overshoot of dynamic response must be less than a specified maximum.
- The steady state error should conform to the closed loop control specifications. Ideally it should be zero.
- The regulator must be stable under all possible component variations and under all conditions.

To achieve the above objectives, closed loop controller has to be designed. The steady state error is related to the loop gain $G(s)H(s)$ of the closed loop at dc (Notes from Ramanarayan's lecture). The steady state error is approximately $1/(G(s)H(s))$. If an integral controller is used then the steady state error is zero.

The settling time and transient overshoot are related to the 0 dB cross-over frequency of the loop gain and the phase margin. If ω_c is the 0 dB crossover frequency of the loop gain then the settling time (for a stable system) will be about $3/\omega_c$ to $4/\omega_c$ seconds. The bandwidth is selected to be nearly $1/2$ of the switching frequency i.e. 8·5 kHz. The analog compensator designed using 'SISO' tool in Matlab, is a PI compensator which meets the following specifications.

- Steady state error of zero
- Settling time of $< 50\,\mu$ sec.
- Transient overshoot $< 1\%$.

Figure 5 shows the bode plot response of the loop gain $G(s)H(s)$ which indicates the control system parameters like gain margin, phase margin and gain cross over frequency. The analog compensator has the transfer function given by

$$G_c(s) = 350\frac{s + 0{\cdot}67}{s}. \tag{12}$$

The two commonly used approaches to the design of a digital control systems are direct digital design and digital redesign (Dum & Jin 1999). In the first approach, the objective

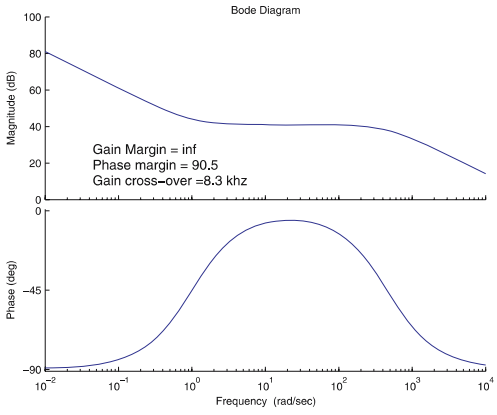

Figure 5. Bode diagram of $G(s)H(s)$.

is to carry out all the design steps in the discrete-time (DT) domain, where the behaviour of the continuous-time (CT) plant is considered only at the sampling instants i.e. the plant function is discretized and the controller is designed in the discrete-time domain. The second approach is to obtain a digital controller by discretizing a pre-designed analog controller. One of the important advantages of this approach is that there are many transformation techniques by which the continuous time model can be converted to discrete controller using classical methods. Moreover, unlike the direct approach, the sampling period can be selected after the analogue control system is designed and, thus, the CT closed-loop bandwidth is known. This method of designing a discrete controller is called the direct redesign approach. However, the performance of this method is significantly affected by the selected discretization method and the sampling interval. The digital controller designed here is based on the first approach where the digital controller is designed for discretized plant model after a detailed study of the other discretization techniques.

2.5 *Direct digital design approach*

In this approach, the plant function is discretized using Zero Order Hold (ZOH) approach (Dum & Jine 1999), and the controller is designed directly in the z-domain using methods such as discrete time frequency response method, root-locus method. The discretized plant transfer function is given by

$$G(z) = \frac{0{\cdot}409}{z - 0{\cdot}995}. \tag{13}$$

2.5a *Transformation to w-plane:* The discrete w-transform is used to retain the design features of the continuous systems (Gene Franklin *et al* 1990). The discrete model of the plant, $G(z)$ is transformed to w-plane by the mapping function

$$\cong \frac{2(z-1)}{T(z+1)}. \tag{14}$$

The resulting compensation is then converted back to z-plane, and discrete PI controller implemented. The digital controller is designed on this plane with the control system specifications

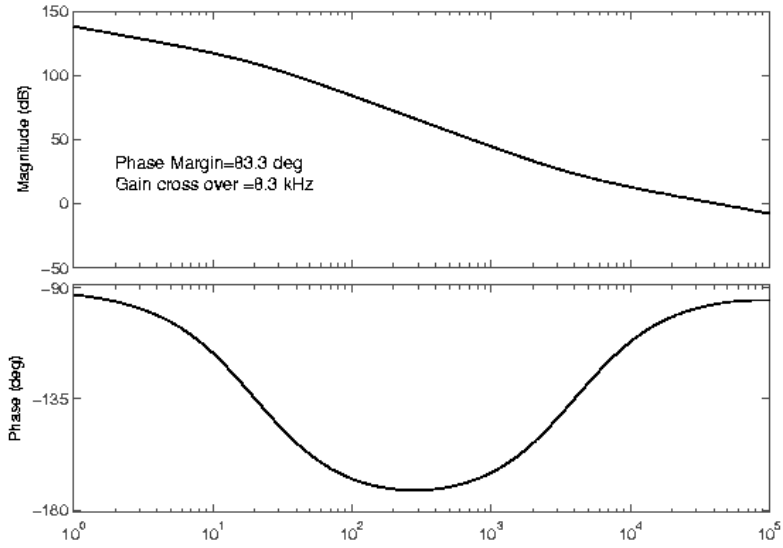

Figure 6. Bode plot of $G(z)H(z)$.

as mentioned above. It is given by

$$G_c(w) = \frac{(0{\cdot}409 - 2{\cdot}55 \times 10^{-6}w)}{(5 \times 10^{-3} + 12{\cdot}47 \times 10^{-6}w)} \tag{15}$$

$$G_c(z) = \frac{234{\cdot}5(z - 0{\cdot}996)}{z - 1}. \tag{16}$$

The loop gain characteristic with the digital controller is shown in figure 6 and the parameters such as phase margin, bandwidth and gain margin are indicated.

3. Design of FPGA-based controller

The use of software to change the controller functionality makes a system based on a digital controller flexible. Spartan 3 XC3S200 FPGA from Xilinx Corporation has been chosen for implementing the controller. Spartan 3 FPGA uses eight independent I/O banks to support 24 different single-ended and differential I/O standards and also the cost per gate is low. Spartan 3 has 33K logical cells, dedicated multipliers, 64 Kbits of internal RAM and improved clock management functions which are essential to achieve high resolution of the controller. Figure 7 identifies the main blocks of the schematic diagram of the designed hardware. The voltage sample from the rectifier of the DC–DC converter is fed to 12 bit A/D converter through an isolation amplifier. The A/D converter samples the voltage and current at the rate of 80 kHz and feeds to FPGA through appropriate timing and control signalling. The FPGA processes the fedback voltage, through PI controller and gives phase shifted pulses such that the output DC voltage is maintained under regulation. The switching frequency, inverter voltages and currents are monitored on the host controller through USB device, and when fault occurs in the system, the gate pulses are withdrawn and the status is sent to the host controller.

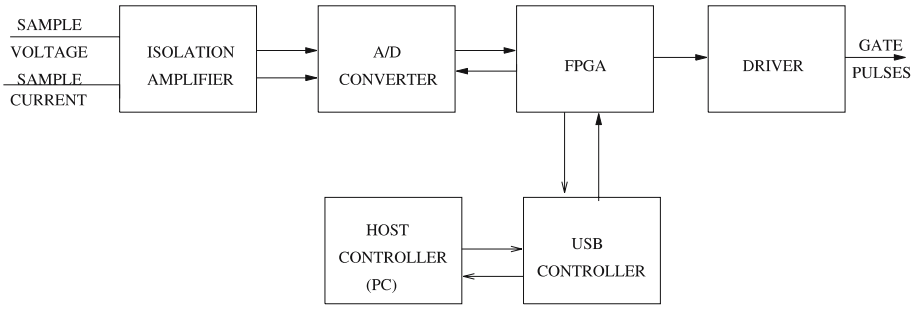

Figure 7. Configuration of the digital controller board.

Figure 8 shows the functional block diagram of the proposed phase shifter. It consists of various registers for storing the voltage and current samples from 12 bit A/D converter, dead-time registers, through which dead-time of the PM-SRC can be adjusted to achieve ZVS and avoid shoot through, switching frequency register which is used to adjust the switching frequency of the inverter, so that the ratio of switching to resonant frequency is maintained. The voltage and current samples are given to the computational block, which has the PI controller developed in it. The softstart mechanism proves to reduce the transients that occurs when the output voltage capacitor charges initially. The ramp generator produces pulses at twice that of the switching frequency. The 12 bit value obtained from the computational block, which carries the phase shift information is compared with the ramp to generate the final phase shifted pulses. The lockout circuit checks for any anomalies and passes the gate pulses to the respective drivers. The detailed implementation of various blocks of figure 8 is shown in figures 9–12. Figure 9 shows the control and data flow between A/D converter and FPGA which is coded in Hardware Description Language as finite state machine model. The state

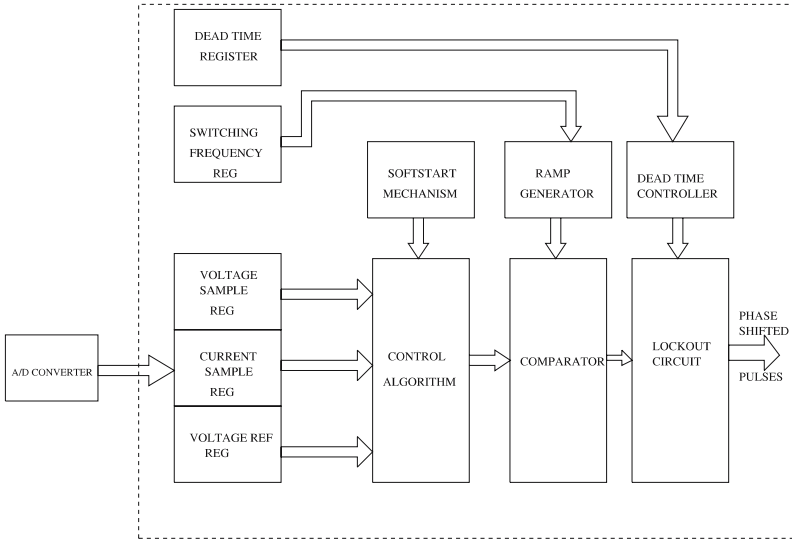

Figure 8. Functional block diagram of phase-shift controller.

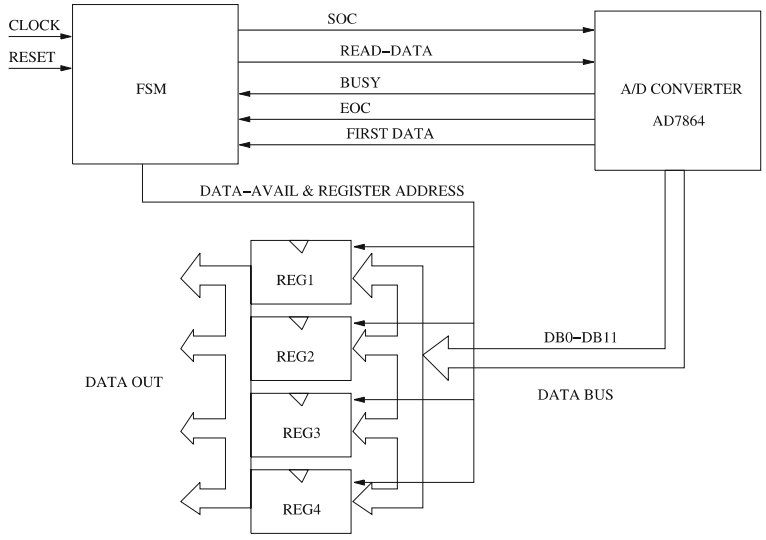

Figure 9. Finite state machine model for A/D conversion.

transition diagram of A/D conversion process is shown in figure 10. The flow of the realization of PI controller is shown in figure 11. The dead time controller implementation is shown in figure 12. Provision is given on the hardware through DIP switches to adjust the dead time from 100 ns up to $1{\cdot}6\,\mu$sec for each device leg independently.

The functions that the phase-shift controller is intended to perform are identified. These individual entities like PI controller, dead time controller, ramp generator, interlocking and protection are then coded using any hardware description language VHDL or Verilog. The modules are individually tested by writing test benches and all the modules are combined and tested by giving the required inputs to the device under test i.e. here the phase shift controller. The synthesis of the code and its conversion to a format compatible for downloading onto

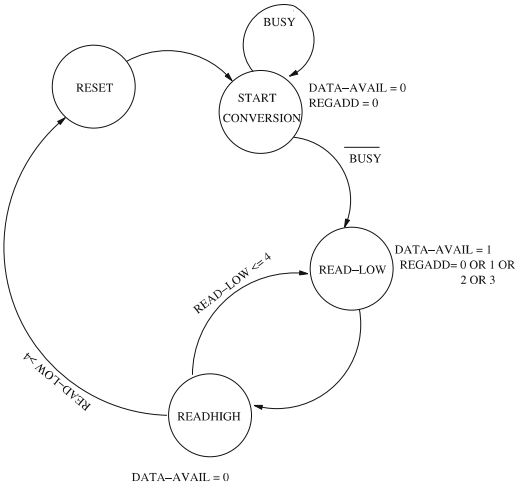

Figure 10. State transition diagram.

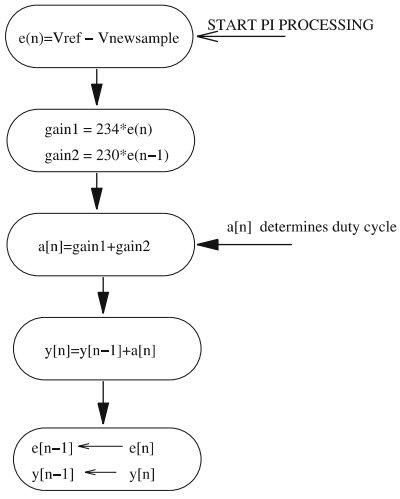

Figure 11. PI controller realization.

FPGA and PROM was done using Xilinx synthesis tool. For stand-alone operation of the controller, the bit stream file is downloaded into the EEPROM present in the digital hardware board. The hardware consists of Spartan 3 FPGA, A/D converter, USB controller and other power supply sequencing circuits for the devices.

3.1 *Effect of finite word length*

Due to quantization, and representation of the duty cycle ratios in a fixed point arithmetic format, there arises a difference between continuous control system and discrete controller system implementation. Thus it becomes essential to study the effects of finite word representation in digital control systems. The optimum design will have smaller number of bits of resolution and also meets the control system specifications for a given converter. For 8 bit representation of duty ratio, the number of CLB's occupied on FPGA is lesser, but it would result in the phenomena called limit cycle oscillation. Thus 12 bit representation is opted, and resources present in Spartan 3 FPGA is found to suit this application. The resource utilization for the implementation of phase shift controller is as follows. It uses 25% of Digital Clock Managers (DCM's), 16% of multiplier blocks, 12% of LUT's and 20% of slice registers.

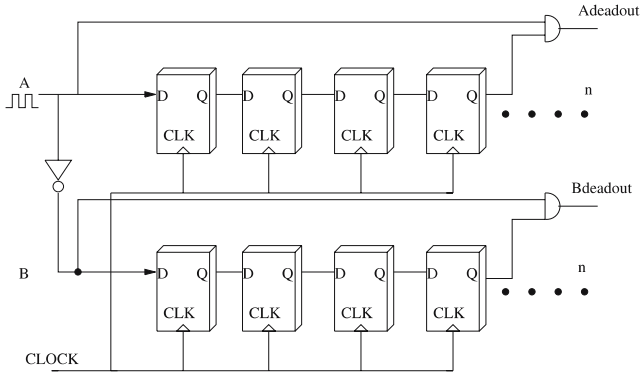

Figure 12. Dead time control realization.

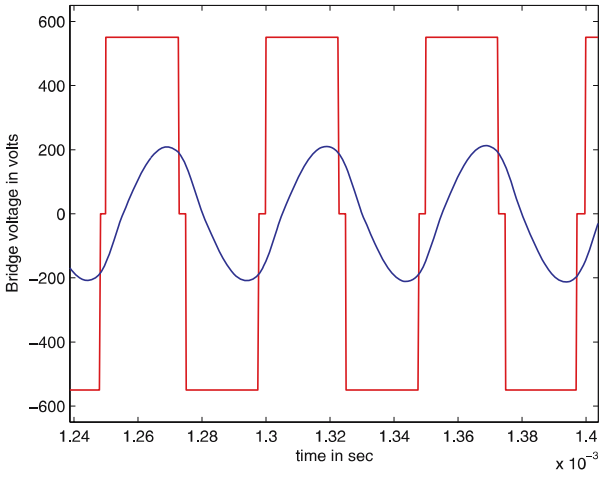

Figure 13. Full load.

3.2 *Computational algorithm realization*

The resolution of ADC is determined such that one LSB of ADC must be lesser than ΔV_o, the output ripple voltage and based on the ripple voltage requirements, 12 bit ADC is chosen for this application. The sampling frequency of the control loop must be determined so that the switching frequency should be an integral multiple of the sampling frequency of the digital controller (Shih-Liang Jung *et al* 1997). Thus the sampling of the control loop is done at 40 kHz which is twice of the switching frequency.

Digital phase shift modulator produces a discrete set of duty ratio values. This means that in steady state only a discrete set of output voltage values can be obtained. If the desired output voltage value does not belong to one of these discrete values, the feedback controller will switch among two or more discrete values of the duty ratio. In digital control systems, this type of oscillation is known as the limit cycle. A necessary condition to avoid the limit cycle oscillation is that the change in the output voltage caused by one LSB change in the duty ratio has to be smaller than the analog equivalent of the LSB of the A/D converter. Limit cycle is alleviated here by appropriate resolution of duty cycle. The PI compensator realized using direct digital design technique is converted to time domain equation as follows.

$$V_o(n) = V_o(n-1) + 235e(n) - 230e(n-1). \tag{17}$$

Dedicated adders and multipliers present in Spartan 3 FPGA are the resources needed to build the controller.

Figures 13 and 14 show the simulated result under full load and 50% load conditions with discrete controller using MATLAB/SIMULINK. The resonant current value is scaled by nearly 175 times.

4. Dynamics of PM-SRC and experimental results

The transients observed under variations of load and line voltages are simulated and the controller's operation is established. During the start-up transient, since the capacitor is uncharged, it acts as a short circuit, thereby offering a low impedance. As a result, the peak current drawn is

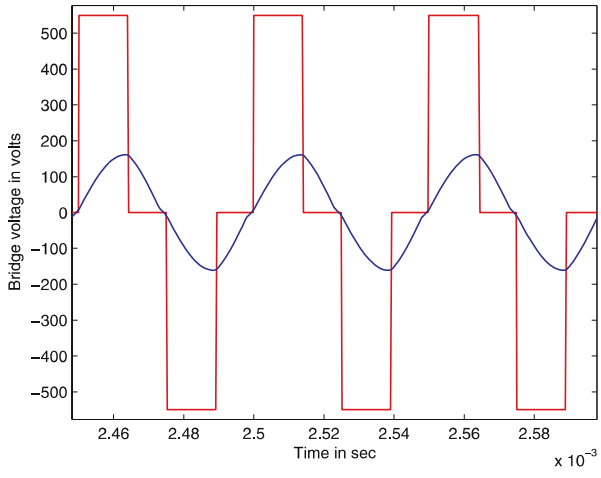

Figure 14. Half load.

many times higher than the steady state current. Soft-start feature of the phase shift controller can be used to prevent the transient current. The experimental results after implementing the controller on FPGA, and building the series resonant inverter with the given specification are shown in figures 15 and 16. To limit the peak current during start-up, average current mode control method may be employed, which limits the transient current, figure 17 shows the initial start-up current in simulation. It is seen that under full load conditions ZVS is maintained undoubtedly. The transformer used in the design has turns ratio of 1:3 with primary turns of 100 and secondary turns of 300. The transformer is of ferrite core type. The secondary of the transformer is connected to bridge rectifier, the diodes whose t_{rr} is 200 ns.

4.1 *Dead time calculation*

From the MATLAB simulated result, the current at which device switches off is 1 A. As there are no additional snubber capacitors across IGBT's, the dead time is calculated based

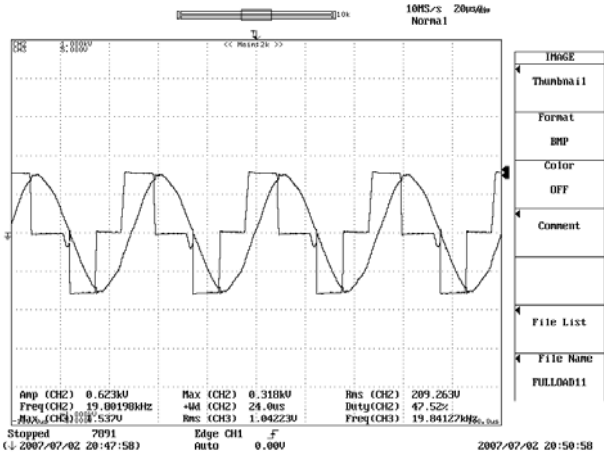

Figure 15. Bridge voltage and current during softstart.

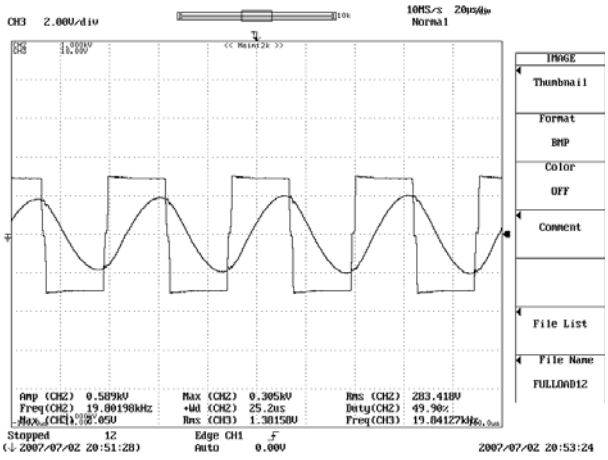

Figure 16. Bridge voltage and current under full load.

on the device capacitance which is around 1 nF. For a bridge voltage of 300 V, the dead time is calculated as

$$I = C_{device} \times \frac{dv}{dt}. \tag{18}$$

Thus the dead time obtained is 300 nsec. The fall time and turn off delay time of the device is around 500 nsec. Thus dead time for each leg was set to around 1 μ sec.

5. Conclusion

The objective of this work was to identify and evolve a design methodology for a suitable power converter for dc-dc generation using digital controller and phase-modulation technique. Soft switching of the converter devices was needed for realising high efficiency and low generated EMI. Thus ZVS technique was adopted. The FPGA based control of phase modulation

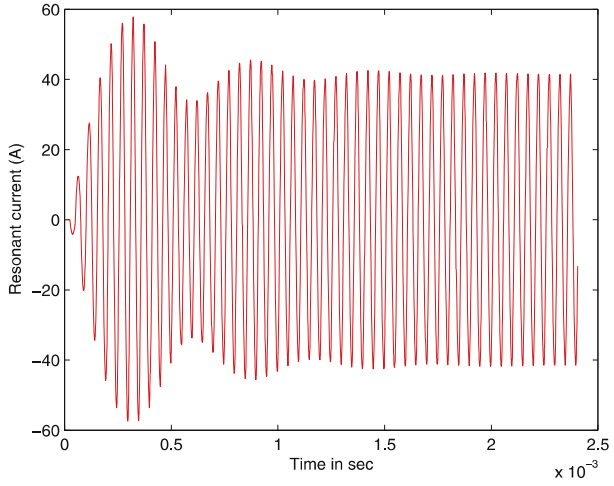

Figure 17. Initial startup current.

proved to be a novel method of control of series resonant inverter. Design and experiments were carried out and the results obtained through simulation were found to match with the experimental one to a large extent. The efficiency obtained was about 83%. Prudent choice of operating frequency, operation of converter either below resonance or above resonance, method of control, various mechanisms required to build a digital controller, the A/D converter selection, isolation amplifier selection such that bandwidth of operation was preserved were some of the issues involved in building the converter.

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