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Electrical features in AlGaN/GaN high electron mobility transistors with recessed gate and undoped region in the barrier

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Abstract. This study considers electrical parameters of AlGaN/GaN high electron mobility transistor (HEMT) with the recessed gate and un-doped region (URG-HEMT) in the barrier layer. We have investigated the main electrical factors such as the lateral electric field, breakdown voltage (V_B), drain current (I_D), threshold voltage (V_T), output conductance (g_o) and gate capacitance (C_g). Simulation findings compare these parameters in the single heterostructure (SH-HEMT), recessed gate (RG-HEMT) and the proposed (URG-HEMT) structures. Regarding the simulation outcomes, the maximum lateral field in the URG is less than those in the SH and RG HEMTs. This improves the breakdown voltage of the suggested device up to 160 V, while the breakdown voltage in the SH and RG transistors is about 90 V. Therefore, breakdown voltage of the reported device is about 80% larger than that of the other transistors. Also, undoped region in the novel transistor reduces the output conductance and gate-to-drain capacitance. But, the recessed gate and undoped regions in the URG structure decrease in 2-DEG electron density and then reduce drain current.

Keywords. AlGaN/GaN high electron mobility transistor; electric field; breakdown voltage; drain current; gate to drain capacitance.

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1. Introduction

To fabricate high electron mobility transistors (HEMTs), gallium nitride (GaN) and its alloys (AlGaN, InGaN) are very important and ideal candidates. AlGaN/GaN HEMTs can be used in both high-power and high-frequency switching due to their extremely good material features. For example, large band gap and high critical field increase breakdown voltage and output power density. High saturated electron velocity improves saturated drain current, strong spontaneous and piezoelectric polarization fields increases the electron density of 2-DEG, and suitable radiation immunity. It is worth noting that due to the superior material characteristics of GaN, AlGaN/GaN HEMTs are used in high power and frequency circuits compared to AlGaAs/GaAs based HEMTs [1–10].

Structural changes in a field effect transistor (FET) can be used to improve its electrical factors. For example, the recessed gate or undoped region inserting in a MESFET enhances its direct current (DC) and RF characteristics [11–13]. So, in this research, we suggest a new HEMT with recessed gate and undoped region in the barrier (URG-HEMT). We simulate some important electrical features in this structure and compare those with conventional (SH-HEMT) and recessed gate (RG-HEMT) structures. These are: the lateral field, breakdown voltage, drain current, threshold voltage, output conductance and gate capacitance. Simulation results in this study are extracted by means of ATLAS software.

The dimensions of the new and conventional structures are explained in §2. In this section, we clarify models activated in the simulator. In the next section, we consider the effect of recessed gate and undoped region by simulating some electrical features mentioned in the above paragraph. The characteristics in the proposed device will be evaluated with those in the conventional and RG transistors.

2. Device structure

In figure 1, the detailed structures of the URG, RG and conventional [14] transistors are shown. The recessed

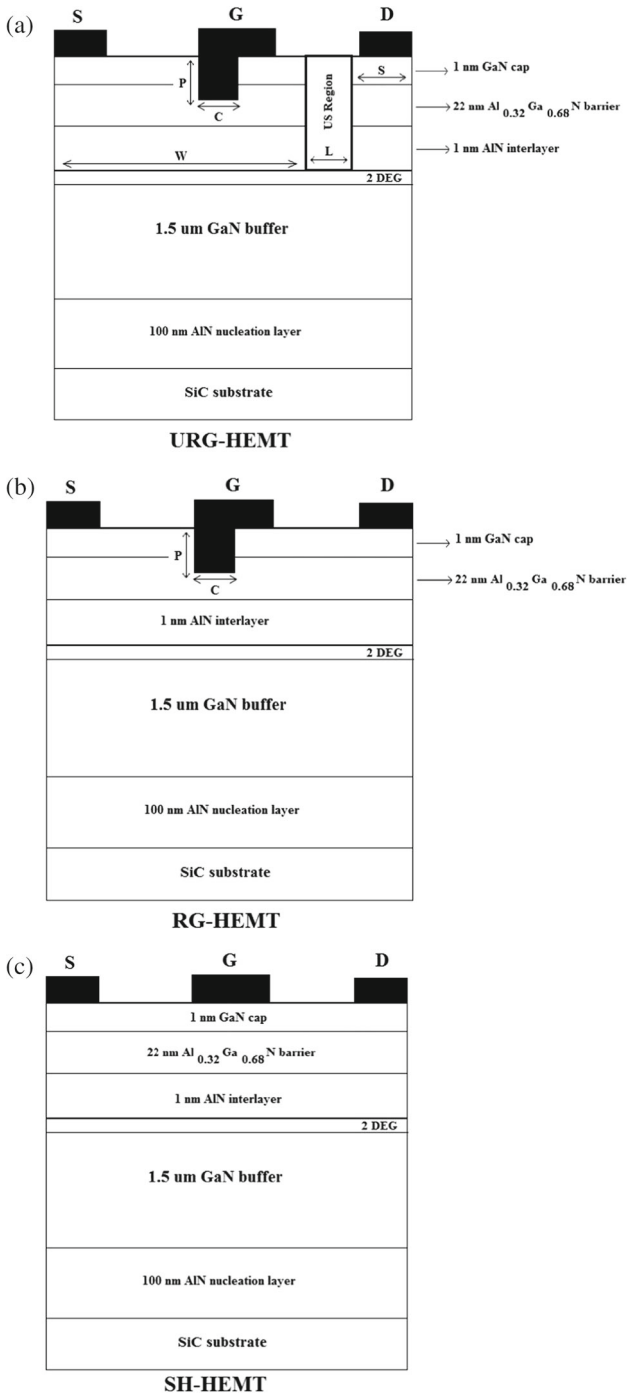

Figure 1. Cross-section view of the (**a**) URG, (**b**) RG and (**c**) SH transistors.

gate length and thickness in the URG and RG devices are equal. For the three structures, the gate length is 0.5 μm, the gate-to-source distance is 1 μm, gate drain spacing is 1 μm and source and drain length is 0.5 μm. The recessed length and thickness in the URG and RG transistors are $C = 0.25\,\mu$m and $P = 5$ nm, respectively. The length of the undoped region of the URG device is $L = 0.3\,\mu$m. Gate to US region distance is 0.2 μm and drain to US region distance is 0.5 μm. W and S parameters in the URG structure are 2.2 and 0.8 μm, respectively. Nickel with 5.1 eV work function has been chosen for the gate. The material used for the barrier layer in this research is $Al_{0.32}Ga_{0.68}N$ (n-type) that has been heavily doped and the barrier width is 22 nm. Undoped GaN of 1.5 μm thicknesses is the buffer region. Si_3N_4 is used as an insulator in these devices with the parameters reported in [15]. ATLAS software has been used to extract simulation results [16]. The software can help to achieve more realistic results by the activation of some models. Hence, in this work, we use 'SRH' model for Shockley–Read–Hall recombination, the 'fldmob' model for parallel electric field-dependent mobility [11,17] and the 'bgn' model for band gap narrowing. In this study, three structures can be fabricated using the process reported in [18].

3. Results and discussion

Figure 2a illustrates the lateral electric field distribution in the channel of the SH, RG and URG devices.

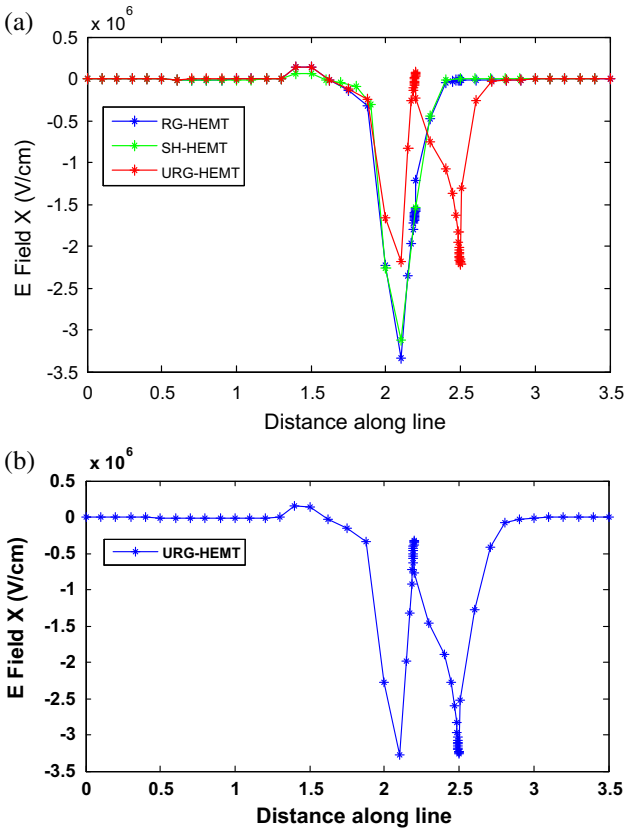

Figure 2. Lateral electric field distribution at (**a**) $V_{GS} = -4$ V and $V_{DS} = 80$ V for three structures and (**b**) at $V_{GS} = -4$ V and $V_{DS} = 150$ V at URG.

In this figure, the gate-to-source bias is −4 V and drain–source voltage is 80 V. This figure shows the electric field dependence as a function of the source-to-drain distance. It is clear that increasing the drain–source space can reduce the maximum electric field and improves breakdown voltage. The maximum electric field in the URG structure has two peaks near the drain. It is due to the undoped region in this transistor that breakdown voltage increases compared to the SH and RG structures. In this work, we have used the critical electric field (E_C) to determine breakdown voltage. E_C in a semiconductor is the maximum electric field that can be applied on a semiconductor. For GaN, E_C is about 3.5 MV/cm. The breakdown voltage in a transistor is a drain voltage that leads to equalisation of the field of the channel with the critical field [19]. Maximum electric field in a junction field effect transistor (JFET) is usually at the gate corner close to the drain. As depicted in figure 2a, the maximum field of the SH and RG HEMTs is almost equal to the critical field of GaN. But, in the proposed structure this value is less than E_C. The increasing drain voltage in URG can be used to reach E_C. Electric field distribution of URG at $V_{GS} = -4$ V and $V_{DS} = 150$ V is shown in figure 2b. The maximum electric field of URG reaches the critical value in the drain voltage. Simulation results show that the breakdown voltage of the SH, RG and URG devices are 95 V, 90 V and 160 V, respectively. The URG reduces the electric field distribution in this transistor due to the introduction of the region without doping. It can be concluded that the breakdown voltage of the suggested device is about 80% larger than those in the SH and RG transistors.

Drain currents vs. the drain biases of the SH and RG transistors are displayed at $V_{GS} = 0$ V in figure 3. The product of the barrier concentration and thickness ($N \times a$) is a vital parameter to improve the drain current [12]. The net density of the two-dimensional electron gas (2-DEG) in an HEMT is a very important factor to increase the drain current. The undoped and the recessed gate region of the novel device reduces the density of the net donor impurities in the barrier. This causes a decrease in the 2-DEG electron density and a reduction in the drain current of the suggested transistor. It is clear from figure 3 that the SH structure has the largest drain current among these three devices because SH does not have undoped and recessed gate region, and this structure has a larger net electron density in the 2-DEG compared to other structures.

Equation (1) can be used to compute output conductance (g_o) in a transistor [20]. According to this equation, g_o shows the drain current dependence to the drain bias at a constant gate bias.

$$g_o = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{gs}=\text{const}}. \tag{1}$$

In an HEMT, electron velocity and density (n_s) of the 2-DEG is effectively controlled by the lateral electric field in this region. Drain–source bias creates this lateral field, and the drain current depends on n_s. Therefore, g_o reveals the impact of this field on the 2-DEG carriers. The DC g_o vs. the drain bias at $V_{GS} = -8$ V is plotted in figure 4. The larger g_m/g_o ratio is a crucial factor in transistors. Hence, smaller g_o in a transistor enhances the device performances. Figure 4 shows that g_o in the suggested device is less than that of the SH and RG structures. This is due to the smaller lateral electric field in the URG that can be seen in figure 2. So, the proposed device reduces lateral field control on 2-DEG velocity and concentration. This can be considered as an advantage compared to other devices.

The charge variation due to the change in gate voltage in the channel of a FET is revealed by gate capacitance. In an HEMT, this charge is collected in the

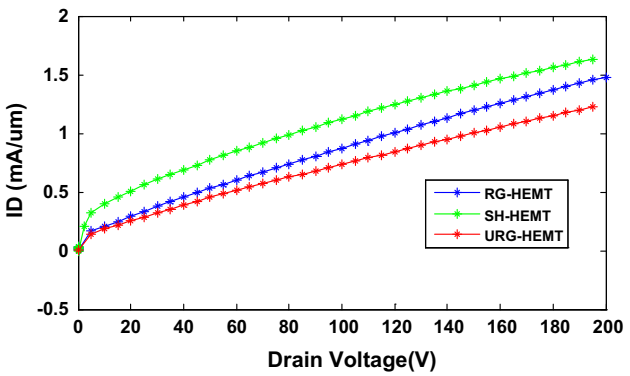

Figure 3. The drain currents with respect to the drain voltages at $V_{GS} = 0$ V.

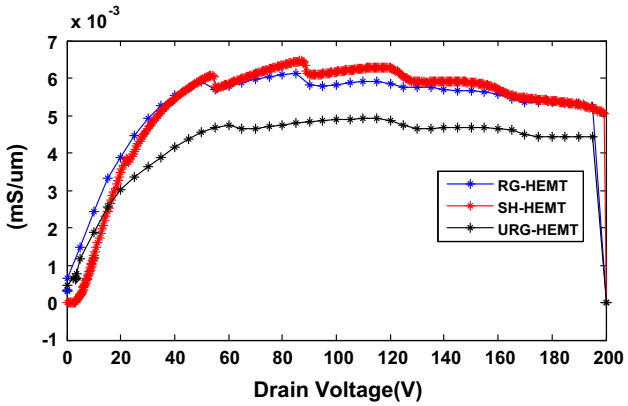

Figure 4. Output conductance depending on drain bias at $V_{GS} = -8$ V.

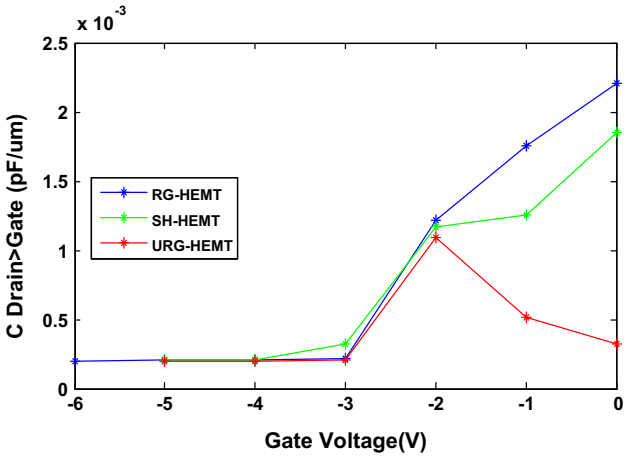

Figure 5. Gate-to-drain capacitance (C_{gd}) with respect to the gate voltage at a frequency of 1 MHz.

2-DEG. Therefore, in these transistors, 2-DEG density can affect the gate capacitance. According to figure 5, the gate-to-drain capacitance changes with respect to the gate–source voltage at a frequency of 1 MHz. As evident from this figure, the URG device has smaller C_{gd} compared to those in the SH and RG structures. It is due to the insertion of the undoped region in the barrier of URG structure at the drain side. This reduces the 2-DEG charge density of the URG at that side and then decreases gate–drain capacitance in the suggested transistor [14]. The maximum difference in C_{gd} occurs at $V_{GS} = 0$ V for all transistors. In this voltage, the RG-HEMT has larger gate–drain capacitance than the other structures because the recessed gate of this transistor is located at the source side. Therefore, it is obvious that charge density of the 2-DEG at the drain side is an important factor in the gate-to-drain capacitance. It can be decided that the proposed structure shows better performance in high-frequency applications.

Figures 6a–6c show the drain current with respect to gate–source voltages at different drain biases (2 V, 4 V and 6 V). These figures illustrate threshold voltages in the SH, RG and URG structures. The recessed gate and undoped regions in the RG and URG transistors reduce 2-DEG electron density and then decrease the drain current in contrast with SH device. Increasing drain bias increases drain current and causes a negative shift in threshold voltage. It is due to increasing horizontal electric field in the channel that can improve the electron velocity and then increases the drain current. Regarding figures, the threshold voltage in SH is more negative than in other structures because of the existence of a recessed gate and undoped layer in the RG and URG devices. This change reduces 2-DEG electron density and then these transistors turn on in a larger gate voltage compared to SH. The threshold voltage in the SH

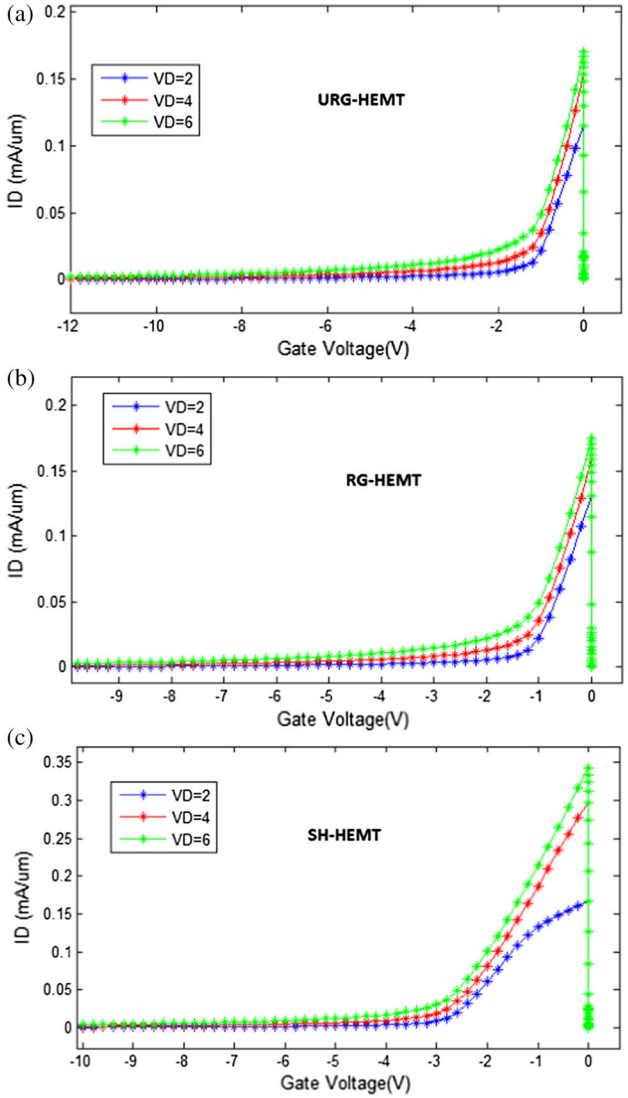

Figure 6. The drain current as a function of gate–source voltages at different drain biases (2 V, 4 V, and 6 V) in the three devices.

is about −3 V, but, this voltage in the RG and URG structures is about −1 V at $V_{DS} = 2$ V. The drain current in the URG is less than that in the RG structure due to the undoped region in URG that decreases the electron density in the 2-DEG.

4. Conclusion

This research considers electrical features in a new AlGaN/GaN HEMT with the recessed gate and undoped region in the barrier region. In the novel device, the undoped region and a recessed gate change the electric field distribution and then increase some electrical parameters. The proposed structure reduces the maximum lateral field in the gate corner and improves the

breakdown voltage compared to RG and SH transistors. The suggested device reduces the output conductance and gate–drain capacitance. RG and URG structures have smaller drain current than SH. The positive shift in the threshold voltage of RG and URG transistors is due to the undoped region that decreases the 2-DEG electron density.

References

[1] B Das, R Goswami and B Bhowmick, *Pramana – J. Phys*. **86(4)**, 723 (2016)

[2] R Swain, K Jena and T R Lenka, *Pramana – J. Phys*. **88(3)**: 723 (2017)

[3] P C Chou, S H Chen, T E Hsieh, S Cheng, J A Alamo and E Y Chang, *Energies* **233**, 1 (2017)

[4] S Garcia, I I Torre, J Mateos, T Gonzalez and S Perez, *Semicond. Sci. Technol.* **31(6)**, 065005 (2016)

[5] J Luo, S L Zhao, M H Mi, W W Chen, B Hou, J C Zhang, X H Ma and Y Hao, *Chin. Phys. B* **25(2)**, 027303 (2016)

[6] M Juncai, Z Jincheng, X Junshuai, L Zhiyu, L Ziyang, X Xiaoyong, M Xiaohua and H Yue, *J. Semicond.* **33(1)**, 14002 (2012)

[7] W Chong, H Yunlong, Z Xuefeng, H Yue, M Xiaohua and Z Jincheng, *J. Semicond.* **33(3)**, 34003 (2012)

[8] J Liu, Y Zhou, J Zhu, Y Cai, K M Lau and K J Chen, *IEEE Trans. Electron Devices* **54(1)**, 2 (2007)

[9] R Gupta, S Rathi, M Gupta and R S Gupta, *Superlattices Microstruct.* **47**, 779 (2010)

[10] K Nomoto, Y Toyoda, M Satoh, T Inada and T Nakamura, *Nucl. Instrum. Methods Phy. Res. B* **272**, 125 (2012)

[11] A A Orouji, S M Razavi, S E Hosseini and H A Moghadam, *Semicond. Sci. Technol.* **26**, 115001 (2011)

[12] C L Zhu, Rusli, C C Tin, G H Zhang, S F Yoon and J Ahn, *Microelectron. Eng.* **83**, 92 (2006)

[13] J Zhang, X Luo, Z Li and B Zhang, *Microelectron. Eng.* **84**, 2888 (2007)

[14] S M Razavi, S H Zahiri and S E Hosseini, *Physica E* **54**, 24 (2013)

[15] T R Lenka and A K Panda, *Pramana – J. Phys.* **79(1)**, 151 (2012)

[16] ATLAS user's manual: Device simulation software, Silvaco International (2005)

[17] S E J Mahabadi, A A Orouji, P Keshavarzi and H A Moghadam, *Semicond. Sci. Technol.* **26**, 95005 (2011)

[18] L Pang, Y G Lian, D S Kim, J H Lee and K Kim, *IEEE Trans. Electron Devices* **59(10)**, 2650 (2012)

[19] S M Razavi, S H Zahiri and S E Hosseini, *Pramana – J. Phys.* **58**, 1362 (2017)

[20] M K Verma and B B Pal, *IEEE Trans. Electron Devices* **48(9)**, 2138 (2001)