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Short-channel drain current model for asymmetric heavily/lightly doped DG MOSFETs

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Abstract. The paper presents a drain current model for double gate metal oxide semiconductor field effect transistors (DG MOSFETs) based on a new velocity saturation model that accounts for short-channel velocity saturation effect independently in the front and the back gate controlled channels under asymmetric front and back gate bias and oxide thickness. To determine the front and the back-channel velocity saturation, drain-induced barrier lowering is evaluated by effective gate voltages at the front and back gates obtained from surface potential at the threshold condition after considering symmetric and asymmetric front and back oxide thickness. The model also incorporates surface roughness scattering and ionized impurity scattering to estimate drain current for heavily/lightly doped channel for short-channel asymmetric DG MOSFET and a good agreement has been achieved with TCAD simulations, with a relative error of around 3–7%.

Keywords. Asymmetric double gate; drain current; drain-induced barrier lowering; velocity saturation; drain saturation voltage.

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1. Introduction

Shrinking down metal oxide semiconductor field effect transistors (MOSFETs) is a good practice for semiconductor industry to achieve higher packing density and better circuit performance. But down-scaling has some disadvantages also. These small scaled devices suffer from various types of short channel effects like velocity saturation, drain-induced barrier lowering (DIBL), gate-induced drain leakage (GIDL), threshold voltage roll-off, etc. Compared to bulk MOSFETs, DG MOSFETs provide superior electrostatic control over channel which provide low short channel effect, 60 mV/dec subthreshold swing, lower output conductance and higher drive current [1–6]. It also improves the performance of logic [7–9] as well as analog applications [10–12]. Previously, various types of drain current models of DG MOSFETs have been demonstrated but they are not so much impressive. Brews [13] demonstrated charge sheet approximation technique for the development of drain current model of bulk MOSFET using Pao-Sah's double integral method based on gradual channel approximation (GCA) technique. However, the charge sheet model cannot capture volume inversion characteristics of DG MOSFETs in the subthreshold regime [14]. Lu and Taur [15] showed a surface potential-based analytical drain current model of undoped or lightly doped symmetric and asymmetric DG MOSFETs based on GCA without considering charge sheet approximation technique. However, to observe some unfavourable effects like mobility degradations and random microscopic fluctuations for a doped channel, consideration of depletion charge in Poisson's equation is also required. Compact models only with depletion charge are not attractive as it is only valid in subthreshold regime and cannot capture strong inversion characteristics [16–19]. As one moves to the short-channel regime, accurate modelling of the mobility degradation due to velocity saturation effects is needed as reported in [20,21]. Drain current in ID-DG MOSFETs after considering both the depletion

and inversion charges is reported in [22] while most of the other models consider only the inversion charges or the depletion charges [23–28]. A surface potential-based drain current model for doped/undoped ID-DG MOSFETs is reported in [29] but it cannot address the short-channel effects.

In this paper, we report a surface potential-based analytical model for short-channel DG MOSFETs with asymmetric front and back gate bias and oxide thickness for both lightly and heavily doped silicon channel scenarios. For simplicity, the quantum mechanical effects that are dominant for channel thicknesses below 20 nm have not been included. First, drain current expression based on the Pao-Sah's double integration method for a long-channel DG MOSFET is obtained from 1D Poisson's equation based on an iterative approach. Then, the model is extended for short-channel devices under the effective gate voltages based on the threshold voltage to include DIBL effect in the subthreshold region. The threshold voltage for short-channel asymmetric DG MOSFET is derived from the surface potential solution obtained from the 2D Poisson's equation based on the iterative approach [30]. Also the mobility model based on velocity saturation, surface roughness scattering and ionized impurity scattering are implemented for both the front and back channel and a good agreement has been achieved with the simulated results from Sentaurus TCAD for a wide variation of doping concentrations, back gate voltages and other structural parameters.

2. Drain current model for short-channel devices

The cross-section of the asymmetric MOSFET is shown in figure 1 where x $(0 \le x \le t_{\rm Si})$ and y $(0 \le y \le L)$ denote the coordinates along the thickness of the silicon film and the length of the channel respectively.

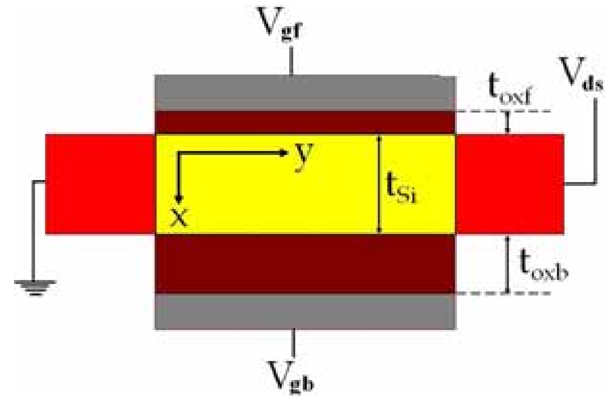

Figure 1. Cross-sectional view of a short-channel asymmetric DG MOSFET.

where $N_{\rm a}$ denotes the channel doping concentration, $\epsilon_{\rm Si}$ is the silicon permittivity, $V_{\rm T} = KT/q$ is the thermal voltage and V is the channel voltage that varies from 0 at the source end to $V_{\rm ds}$ at the drain end. The boundary conditions at the front and back surfaces of the DG MOSFET can be obtained by applying the Gauss law as

$$\epsilon_{\rm Si}\left.\frac{{\rm d}\phi}{{\rm d}x}\right|_{x=0} = -\epsilon_{\rm Si}E_{\rm sf} = \epsilon_{\rm ox}\frac{\phi_{\rm sf}-(V_{\rm gf}-V_{\rm ffb})}{t_{\rm oxf}} \tag{2a}$$

$$\epsilon_{\rm Si}\left.\frac{{\rm d}\phi}{{\rm d}x}\right|_{x=t_{\rm Si}} = -\epsilon_{\rm Si}E_{\rm sb} = \epsilon_{\rm ox}\frac{(V_{\rm gb}-V_{\rm bfb})-\phi_{\rm sb}}{t_{\rm oxb}}, \tag{2b}$$

where $\phi_{\rm sf}$ $(\phi_{\rm sb})$, $V_{\rm gf}(V_{\rm gb})$ and $V_{\rm ffb}$ $(V_{\rm bfb})$ are the surface potential, gate voltage and flat band voltage at the front (back) gate respectively. The front and back surface potentials at source $V = 0$ and drain ends $V = V_{\rm ds}$ are obtained from [29] using second-order solution. Following our model as reported in [29], the drain current in asymmetric heavily doped long-channel DG MOSEFT can be expressed in terms of the front and back surface potentials $\phi_{\rm sf}$ and $\phi_{\rm sb}$ at the source and drain end as

$$I_{\rm ds} = \frac{\mu W\epsilon_{\rm Si}}{L}\left[\begin{array}{l} -\frac{t_{\rm Si}\alpha}{2} - \frac{qN_{\rm a}t_{\rm Si}V_{\rm T}}{\epsilon_{\rm Si}}\left[{\rm e}^{\left(\frac{-2\phi_{\rm F}-V_{\rm ds}}{V_{\rm T}}\right)} - {\rm e}^{\left(\frac{-2\phi_{\rm F}}{V_{\rm T}}\right)}\right] \\ +\frac{C_{\rm oxf}}{\epsilon_{\rm Si}}\left[V_{\rm gf}\phi_{\rm sf} - \frac{\phi_{\rm sf}^2}{2}\right] + \frac{C_{\rm oxb}}{\epsilon_{\rm Si}}\left[V_{\rm gb}\phi_{\rm sb} - \frac{\phi_{\rm sb}^2}{2}\right] \\ +2V_{\rm T}\left[\frac{C_{\rm oxf}\phi_{\rm sf}}{\epsilon_{\rm Si}} + \frac{C_{\rm oxb}\phi_{\rm sb}}{\epsilon_{\rm Si}}\right] - \frac{2qN_{\rm a}t_{\rm Si}}{\epsilon_{\rm Si}}\left[2V_{\rm T}{\rm e}^{\frac{-\phi_{\rm sb}}{V_{\rm T}}} + \phi_{\rm sb}\right] \end{array}\right]\Bigg|_{\alpha_0,\phi_{\rm sf0},\phi_{\rm sb0}}^{\alpha_{\rm L},\phi_{\rm sfL},\phi_{\rm sbL}}, \tag{3}$$

Based on the gradual channel approximation (GCA), the channel potential along the x direction can be obtained by solving the 1D Poisson–Boltzmann equation with the depletion charge, inversion charge and the hole charge as shown in (1)

$$\frac{{\rm d}^2\phi}{{\rm d}x^2} = \frac{qN_{\rm a}}{\epsilon_{\rm Si}}\left[1 + {\rm e}^{\frac{\{\phi-(2\phi_{\rm F}+V)\}}{V_{\rm T}}} - {\rm e}^{-\frac{\phi}{V_{\rm T}}}\right], \tag{1}$$

where $\mu = 1417\ {\rm cm^2/V\text{-}s}$ is the low-field bulk mobility and $C_{\rm oxf(b)}$ is the front (back) gate oxide capacitance. By scaling down the channel length, eq. (3) does not provide satisfactory result for which developing a drain current model for a short-channel asymmetric DG MOSFET by including all the probable charges is highly required. To incorporate short-channel effect in drain current modelling, we need to find out the virtual source,

the point along the channel near the source side where the potential becomes minimum. The position of the virtual source varies between the two gates depending on the gate voltages applied to the terminals. If same gate voltages are applied to the front and the back gates, minimum potential is obtained at the middle of the device thickness. In asymmetric condition, virtual source moves towards opposite direction of a gate terminal having higher gate voltage compared to the other terminal. According to our electrostatic potential model in [29], l is the normalized value of x and the minimum potential, $\phi_{\min}$ $(l, y = 0)$ is obtained by solving $\mathrm{d}\phi\,(l, y = 0)/\mathrm{d}l|_{l=l_{\min}} = 0$. Considering first-order solution, one can obtain an approximate model of electrostatic potential along the channel thickness in terms of the back surface potential from which $l_{\min}$ is defined as

$$l_{\min} = \sqrt{\frac{2\epsilon_{\mathrm{Si}}(\phi_{\mathrm{sf0}} - \phi_{\min})}{qN_{\mathrm{a}}t_{\mathrm{Si}}^2\left[1 + \mathrm{e}^{\frac{(\phi_{\min} - 2\phi_{\mathrm{F}})}{V_{\mathrm{T}}}} - \mathrm{e}^{-\frac{\phi_{\min}}{V_{\mathrm{T}}}}\right]}}. \tag{4}$$

To model short-channel drain current, different second-order effects have to be incorporated as shown in the following subsections.

2.1 *Drain-induced barrier lowering*

Drain-induced barrier lowering effect plays an important role in the subthreshold region for short-channel asymmetric DG MOSFET. By increasing the drain voltage, a significant field penetration occurs from the drain to the source and as a result, the potential barrier at the source side decreases with the increment of drain voltage. In this model, DIBL effect is included by applying effective front and back gate voltages with a subsequent increase in the front and the back surface potentials at the source and the drain ends for an asymmetric DG MOSFET defined by eqs (5a) and (5b) [31]. However, this increment is linearly dependent on gate bias in the subthreshold region and less in the strong inversion region to hold model accuracy.

$$V_{\mathrm{gf}}^{\mathrm{L}} = \frac{1}{\alpha\beta}\log[1 + \alpha\beta\gamma\exp[\beta(V_{\mathrm{gf}} - V_{\mathrm{th}}^{\mathrm{L}})] + \exp[\alpha\beta(V_{\mathrm{gf}} - V_{\mathrm{th}}^{\mathrm{L}})]] \tag{5a}$$

$$V_{\mathrm{gb}}^{\mathrm{L}} = \frac{1}{\alpha\beta}\log[1 + \alpha\beta\gamma\exp[\beta(V_{\mathrm{gb}} - V_{\mathrm{th}}^{\mathrm{L}})] + \exp[\alpha\beta(V_{\mathrm{gb}} - V_{\mathrm{th}}^{\mathrm{L}})]]. \tag{5b}$$

Here α controls the transition from below to above the threshold, β controls the slope of the subthreshold characteristics, γ controls the magnitude of the subthreshold current and $V_{\mathrm{th}}^{\mathrm{L}}$ is the threshold voltage for short-channel DG MOSFET defined from our previous work [30]. The values of α, β and γ for channel length $L = 45$ nm are considered as 1.38, 5.6 and 7.8 respectively to obtain smoothness of the graph in the subthreshold region. To determine the threshold voltage, the 2D Poisson's equation can be written as the sum of 1D Poisson's equation and 2D Laplace equation as follows:

$$\phi(x, y) = \phi_{1\mathrm{D}}(x) + \phi_{2\mathrm{D}}(x, y), \tag{6}$$

where $\phi_{1\mathrm{D}}(x)$ and $\phi_{2\mathrm{D}}(x, y)$ are obtained from [29] and [30] respectively.

$$\phi_{2\mathrm{D}}(x, y) = \left[\cos\left(\frac{\lambda x}{t_{\mathrm{Si}}}\right) + A\sin\left(\frac{\lambda x}{t_{\mathrm{Si}}}\right)\right] \times \left[C_0\mathrm{e}^{\frac{\lambda(y-L)}{t_{\mathrm{Si}}}} + C_1\mathrm{e}^{\frac{-\lambda y}{t_{\mathrm{Si}}}}\right]. \tag{7}$$

The parameters C_0, C_1 and λ are defined in [30]. To obtain the minimum point $y = y_{\min}$, potential expression (7) is differentiated with respect to y and making it to zero, the following relation is obtained:

$$y_{\min} = \frac{L}{2} + \frac{t_{\mathrm{Si}}}{2\lambda}\log\left(\frac{C_1}{C_0}\right). \tag{8}$$

To determine threshold voltage, minimum front surface potential $\phi_{\min}$ (0) is made equal to $2\phi_{\mathrm{F}}$, i.e. $\phi_{\mathrm{s0_th}} + \phi_{2\mathrm{Dmin}}(0) = 2\phi_{\mathrm{F}}$. Applying this condition, $\phi_{\mathrm{s0_th}}$ is defined as [30]

$$\phi_{\mathrm{s0_th}} = \frac{2\phi_{\mathrm{F}} - \frac{1}{1-\mathrm{e}^{-\frac{2\lambda L}{t_{\mathrm{Si}}}}}\left[\left\{V_{\mathrm{ds}} - V_{\mathrm{bi}}\left(\mathrm{e}^{-\frac{\lambda L}{t_{\mathrm{Si}}}} - 1\right)\right\}\mathrm{e}^{\frac{\lambda(y_{\min}-L)}{t_{\mathrm{Si}}}} + \left\{V_{\mathrm{bi}}\left(1 - \mathrm{e}^{-\frac{\lambda L}{t_{\mathrm{Si}}}}\right) - V_{\mathrm{ds}}\mathrm{e}^{-\frac{\lambda L}{t_{\mathrm{Si}}}}\right\}\mathrm{e}^{\frac{-\lambda y_{\min}}{t_{\mathrm{Si}}}}\right]}{\left[1 + \frac{1}{1-\mathrm{e}^{-\frac{2\lambda L}{t_{\mathrm{Si}}}}}\left(\mathrm{e}^{\frac{\lambda(y_{\min}-L)}{t_{\mathrm{Si}}}} + \mathrm{e}^{-\frac{\lambda y_{\min}}{t_{\mathrm{Si}}}}\right)\left(\mathrm{e}^{-\frac{\lambda L}{t_{\mathrm{Si}}}} - 1\right)\right]}. \tag{9}$$

With the help of boundary condition (2a) and 1D front surface potential at the threshold condition, threshold voltage V_{th} for an asymmetric heavily doped DG MOSFET is defined as [30]

$$V_{\mathrm{th}}^{\mathrm{L}} = V_{\mathrm{ffb}} + \phi_{\mathrm{s0_th}} + \left(\frac{\epsilon_{\mathrm{Si}}}{C_{\mathrm{oxf}}}\right)E_{\mathrm{sf}}. \tag{10}$$

2.2 *Velocity saturation model*

For modelling velocity saturation effects in asymmetric DG structure, one need to visualize the effects of both

the front and back gates on the drain saturation voltage. Thus, we have to define two separate drain saturation voltages $V^{\rm f}_{\rm ds_sat}$ and $V^{\rm b}_{\rm ds_sat}$ corresponding to the front and back surface potentials. The front and back surface charge densities can be expressed as [20]

$$V^{\rm f/b}_{\rm ds_sat} = \left(-Q^{\rm f/b}_{\rm seff}/C_{\rm ox,f/b}\right)\frac{v}{v_{\rm sat} - Q^{\rm f/b}_{\rm seff}\frac{\mu_{\rm eff}}{2LC_{\rm ox,f/b}}}, \tag{11a}$$

where

$$Q^{\rm f/b}_{\rm seff} = Q^{\rm f/b}_{\rm s} - 2V_{\rm T}C_{\rm ox,f/b}\frac{v_{\rm sat}}{v_{\rm sat} - V_{\rm T}\frac{\mu_{\rm eff}}{\rm L}},$$

$v_{\rm sat}$ is the saturated electron velocity and $\mu_{\rm eff}$ is the effective mobility. The surface charges $Q^{\rm f}_{\rm s}$ and $Q^{\rm b}_{\rm s}$ can be obtained from the electric field at the front and back gates. The smooth variation of the drain voltage at the transition of $V^{\rm f/b}_{\rm sat}$ can be effectively expressed as in [31]

$$V_{\rm ds_eff_frnt(back)} = V^{\rm f/b}_{\rm ds_sat} - V^{\rm f/b}_{\rm ds_sat}\frac{\log\left(1 + {\rm e}^{A\left(1 - V_{\rm ds}/V^{\rm f/b}_{\rm ds_sat}\right)}\right)}{\log(1 + {\rm e}^{A})}, \tag{11b}$$

where A is a fitting parameter.

2.3 *Channel length modulation (CLM)*

The channel length modulation effects can be incorporated by considering the Gaussian Box in the saturation region as depicted in [32]. However, in asymmetric structure, due to different values of $V^{\rm f}_{\rm sat}$ and $V^{\rm b}_{\rm sat}$, we consider two adjacent Gaussian Boxes as shown in figure 2 where the interface corresponds to the minimum potential as calculated in the previous section. In this procedure, we can obtain two different values of saturation region lengths, namely ΔL_1 and ΔL_2. Following [32], one can obtain ΔL_1 and ΔL_2 as

$$\Delta L_{1(2)} = l_{1(2)}\ln\left[\frac{V_{\rm ds_eff_frnt(back)} - V^{\rm f/b}_{\rm sat}}{l_{1(2)}\xi_{1(2)}} + \sqrt{\left(\frac{V_{\rm ds_eff_frnt(back)} - V^{\rm f/b}_{\rm sat}}{l_{1(2)}\xi_{1(2)}}\right)^2 + 1}\right], \tag{12a}$$

where the lengths

$$l_1 = \sqrt{\frac{\epsilon_{\rm Si}}{\epsilon_{\rm oxf}}t_{\rm oxf}t_{\rm Si}l_{\rm min}}$$

and

$$l_2 = \sqrt{\frac{\epsilon_{\rm Si}}{\epsilon_{\rm oxb}}t_{\rm oxb}t_{\rm Si}\left(1 - l_{\rm min}\right)}$$

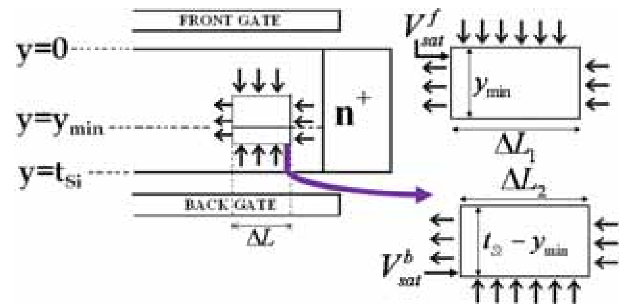

Figure 2. Proposed velocity saturation model for asymmetric DG MOSFET showing two Gaussian Boxes corresponding to the front and back gates based on the minimum channel potential at $l_{\rm min}$.

are the front and back gate characteristic lengths respectively. One issue arises at this point whether to calculate the surface potential values at the front and back with different $V_{\rm ds_eff}$ as should be the case. This is because the effective voltages at the left end of the Gaussian Boxes in the velocity saturation regions are $V^{\rm f}_{\rm sat}$ and $V^{\rm b}_{\rm sat}$ as shown in figure 2. Due to coupling effects between the gates, it is not possible to compute surface potential values at different drain ends at the front and back channels. Thus, we made an assumption where the surface potential values are calculated at an equivalent drain voltage $V_{\rm ds_equiv}$ and not at $V_{\rm ds_eff_frnt}$ and $V_{\rm ds_eff_back}$ where $V_{\rm ds_equiv}$ can be expressed as

$$V_{\rm ds_equiv} = -\frac{1}{2}\left(\frac{Q^{\rm f}_{\rm seff}}{C_{\rm oxf}} + \frac{Q^{\rm b}_{\rm seff}}{C_{\rm oxb}}\right) \times \frac{v_{\rm sat}}{v_{\rm sat} - \frac{\mu_{\rm eff}}{4L}\left(\frac{Q^{\rm f}_{\rm seff}}{C_{\rm oxf}} + \frac{Q^{\rm b}_{\rm seff}}{C_{\rm oxb}}\right)}. \tag{12b}$$

All the short-channel effects are computed with the effective drain voltages $V_{\rm ds_eff_frnt}$ and $V_{\rm ds_eff_back}$. With this assumption, a good agreement with device simulation results has been obtained.

2.4 *Mobility models*

The mobility in MOSFETs depends mainly on the phonon scattering, ionized impurity scattering and surface roughness scattering. Apart from these factors, the mobility also degrades due to the velocity saturation effects in the short-channel devices. Thus, the effective mobility due to the former factors can be expressed from the Matthiessen's rule as

$$\frac{1}{\mu_{\rm eff}} = \frac{1}{\mu} + \frac{1}{\mu_{\rm srs}} + \frac{1}{\mu_{\rm iis}}, \tag{13}$$

where $\mu_{\rm srs}$ is the mobility due to surface roughness scattering and $\mu_{\rm iis}$ is due to the ionized impurity scattering. In our model, at room temperature and for the low doped channel, $\mu_{\rm iis}$ is not a significant component. $\mu_{\rm srs}$ in the

front and back channel at $T = 300$ K can be expressed from the model by Nishida and Sah [33] as follows:

$$\mu_{\text{srs_frnt}} = 7.95 \times 10^{10}/(E_{\text{sf}})^{1.31} \tag{14a}$$

$$\mu_{\text{srs_back}} = 7.95 \times 10^{10}/\left(-E_{\text{sb}}\right)^{1.31}, \tag{14b}$$

where $E_{\text{sf}}/E_{\text{sb}}$ are having values greater than 1×10^{6} V/cm. Apart from surface roughness scattering, the presence of impurity ions also results in randomly deflected electrons and holes that result in mobility degradation. The mobility degradation due to ionized impurity scattering can be expressed as reported in [33],

$$\mu_{\text{iis}} = 90(1 + (2.0 \times 10^{18}/N_{\text{a}})(T/300)), \tag{15}$$

where N_{a} is the channel doping concentration. After calculating effective mobility from (13), the longitudinal electric field-dependent mobility [20] at the front and back gates can be incorporated as shown in (16) and (17)

$$\mu_{\text{frnt}} = \frac{\mu_{\text{eff_frnt}}}{\left[1 + \left(\frac{\mu_{\text{eff_frnt}}}{v_{\text{sat}}} \frac{V_{\text{ds_sat}}^{\text{f}}}{(L-\Delta L_1)}\right)^{n_m}\right]^{\frac{1}{n_m}}} \tag{16}$$

$$\mu_{\text{back}} = \frac{\mu_{\text{eff_back}}}{\left[1 + \left(\frac{\mu_{\text{eff_back}}}{v_{\text{sat}}} \frac{V_{\text{ds_sat}}^{\text{b}}}{(L-\Delta L_2)}\right)^{n_m}\right]^{\frac{1}{n_m}}}, \tag{17}$$

where $v_{\text{sat}} \approx 7 \times 10^{6}$ cm/s is the saturation velocity and n_m is the fitting parameter. Thus, the short-channel drain current in asymmetric heavily doped DG MOSFET at the effective front and back gate voltages defined by eqs (5a) and (5b) can be expressed as the sum of the front current $I_{\text{ds_frnt}}$ and back current $I_{\text{ds_back}}$ as shown in (18) and (19) where

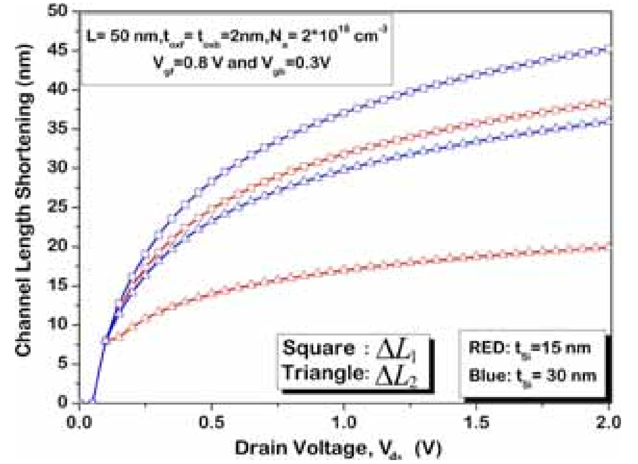

Figure 3. Channel length shortening ΔL_1 and ΔL_2 for heavily doped asymmetric DG MOSFET with varying channel thicknesses.

in figure 2, two different mathematical models of ΔL_1 and ΔL_2 are shown in figures 3 and 4 for different values of channel doping and thicknesses. It is evident that the channel length modulation effect is more sensitive to drain-to-source voltage for higher values of thickness or gate voltage. The channel length dependence of the drain saturation voltage at the front and back gates are shown in figure 5 for a heavily doped channel. The variation of the drain saturation voltage with channel length is prominent for higher gate voltages, i.e. for strong inversion regime. For asymmetric DG operation with higher channel lengths, the gate terminal with a higher voltage will experience a higher drain saturation voltage and thus may pose a serious challenge for analog circuit designers. As the proposed model is

$$I_{\text{ds_frnt}} = \frac{\mu_{\text{frnt}} W \epsilon_{\text{Si}}}{L - \Delta L_1} \left[\begin{array}{l} -\frac{l_{\min} t_{\text{Si}} \alpha}{2} + \frac{C_{\text{oxf}}}{\epsilon_{\text{Si}}}[(V_{\text{gf}} + 2V_{\text{T}})\phi_{\text{sf}}] \\ -\frac{C_{\text{oxf}} \phi_{\text{sf}}^2}{2\epsilon_{\text{Si}}} - \frac{2qN_{\text{a}} l_{\min} t_{\text{Si}}}{\epsilon_{\text{Si}}} \left[2V_{\text{T}} \left(\mathrm{e}^{\frac{-2\phi_{\text{sb}}}{V_{\text{T}}}} + \phi_{\text{sb}} \right) \right] \end{array} \right] \Bigg|_{\alpha_0, \phi_{\text{sf0}}, \phi_{\text{sb0}}}^{\alpha_{\text{L}}, \phi_{\text{sfL}}, \phi_{\text{sbL}}} \tag{18}$$

$$I_{\text{ds_back}} = \frac{\mu_{\text{back}} W \epsilon_{\text{Si}}}{L - \Delta L_2} \left[\begin{array}{l} -\frac{(1 - l_{\min}) t_{\text{Si}} \alpha}{2} + \frac{C_{\text{oxb}}}{\epsilon_{\text{Si}}}[(V_{\text{gb}} + 2V_{\text{T}})\phi_{\text{sb}}] \\ -\frac{C_{\text{oxb}} \phi_{\text{sb}}^2}{2\epsilon_{\text{Si}}} - \frac{2qN_a(1 - l_{\min}) t_{\text{Si}}}{\epsilon_{\text{Si}}} \left[2V_{\text{T}} \left(\mathrm{e}^{\frac{-2\phi_{\text{sb}}}{V_{\text{T}}}} + \phi_{\text{sb}} \right) \right] \end{array} \right] \Bigg|_{\alpha_0, \phi_{\text{sf0}}}^{\alpha_{\text{L}}, \phi_{\text{sbL}}}. \tag{19}$$

3. Results and discussion

In this section, the I_{d}–V_{ds} characteristics will be discussed for asymmetric channel operation with heavily/lightly doped channel. The width W is fixed at 1 μm and the metal gate work function is fixed at 4.61 eV unless otherwise specified. Based on our proposed model of channel length modulation as shown based on division of the channel into front and back parts along the minimum potential contour, an accurate prediction of $l_{\min}$ is necessary as is shown in figure 6. The variation of $l_{\min}$ with respect to varying front gate voltage at a fixed back bias is shown where the absolute relative error between the proposed model and numerical simulation is within 4%. The drain current for heavily and lightly doped channel is plotted in figures 7 and 8 respectively with mobility depending only on the

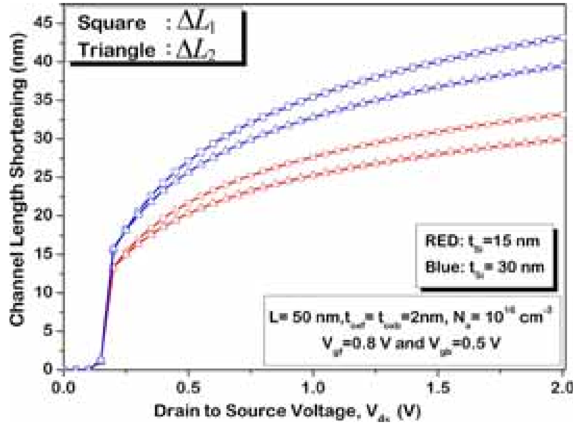

Figure 4. Channel length shortening ΔL_1 and ΔL_2 for lightly doped asymmetric DG MOSFET with varying channel thicknesses.

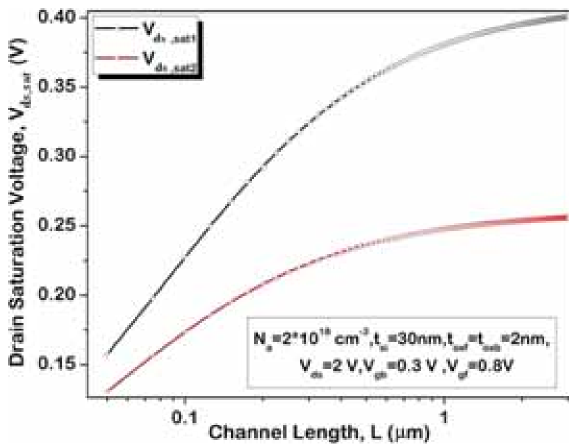

Figure 5. Front and back channel drain saturation voltages for heavily doped asymmetric DG MOSFET as a function of channel length.

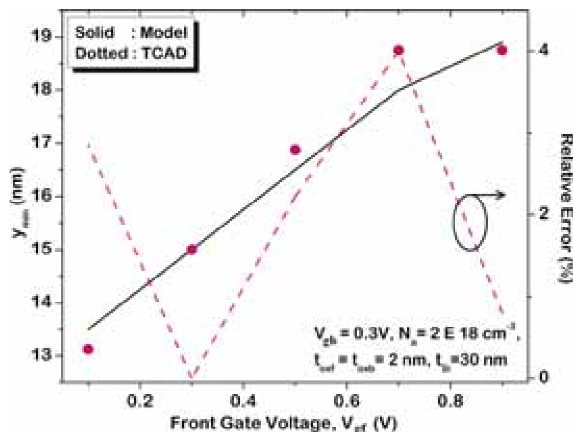

Figure 6. $l_{\min}$ as a function of front gate voltage compared with simulation results for heavily doped asymmetric DG MOSFET.

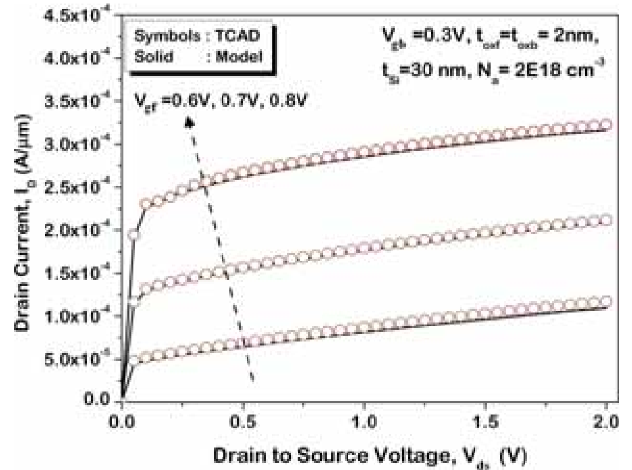

Figure 7. Drain current as a function of drain voltage for heavily doped asymmetric DG MOSFET with front gate voltage as the parameter. The mobility is fixed at 0.1417 cm^2/V-s and only the velocity saturation effect is included.

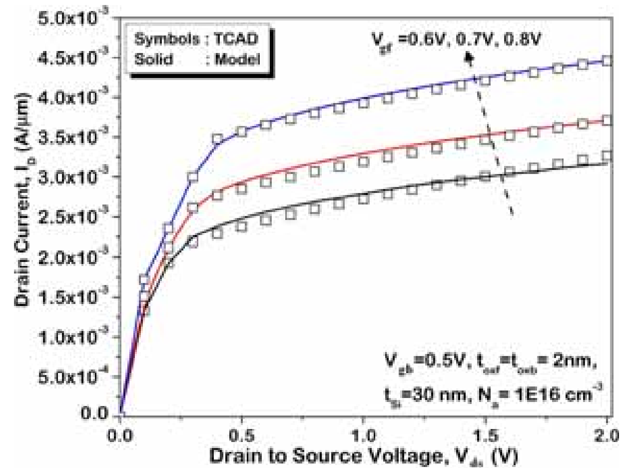

Figure 8. Drain current as a function of drain voltage for lightly doped asymmetric DG MOSFET with front gate voltage as the parameter. The mobility is fixed at 0.1417 cm^2/V-s and only the velocity saturation effect is included.

velocity saturation effects where it is evident that the saturation drain voltage as well as the effective current values increase for the lightly doped case. Finally, the effect of silicon thickness on the drain current is shown in figure 9 where it is observed that the channel length modulation effect is prominent in devices with high thickness. Here, the mobility is kept dependent on the velocity saturation, surface roughness scattering and ionized impurity scattering effects. A detailed analysis of this curve shows that at near saturation region, the current values are quite low in higher t_{Si} devices but as V_{ds} increases, the rate of increase of the drain current is much more due to a large increase in the channel length modulation effects in these devices.

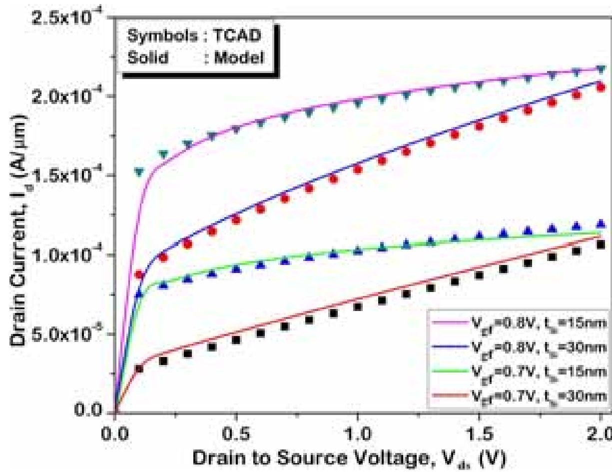

Figure 9. Drain current as a function of drain voltage for heavily doped asymmetric DG MOSFET with front gate voltage as the parameter. The mobility is dependent on velocity saturation, ionized impurity scattering as well as on surface roughness scattering.

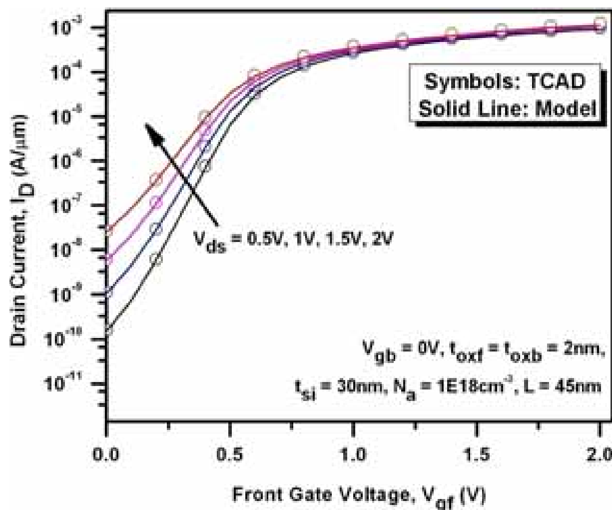

Figure 10. Drain current as a function of front gate voltage for heavily doped asymmetric DG MOSFET with drain voltage as the parameter at a constant back gate voltage for the same front and back oxide thickness. The mobility is dependent on velocity saturation, ionized impurity scattering as well as on surface roughness scattering.

Again as V_{ds} increases, the mobility degradation due to velocity saturation becomes dominant as evident from (16) and (17). But from the increased rate of current with drain voltage, it can be concluded that the channel length modulation is a dominant factor over mobility degradation by velocity saturations. The drain current for heavily doped channel is plotted in figures 10 and 11 for the same and different front and back oxide thickness at different front gate voltages

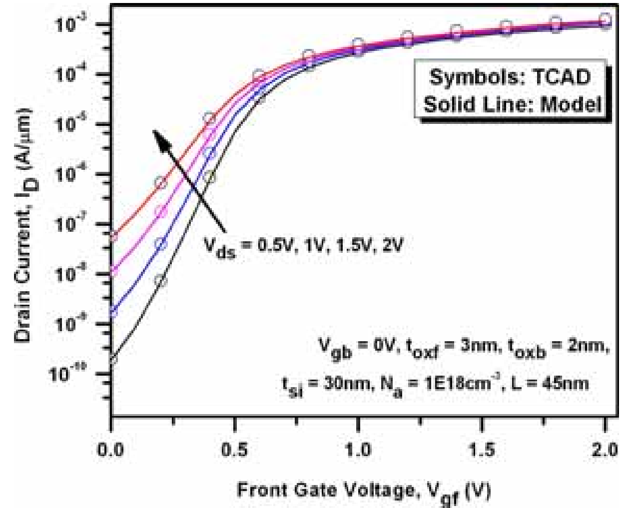

Figure 11. Drain current as a function of front gate voltage for heavily doped asymmetric DG MOSFET with drain voltage as the parameter at a constant back gate voltage for different front and back oxide thicknesses.

for different drain biases. It is observed that the increment of drain current is more significant in subthreshold region than in strong inversion region due to DIBL effect.

4. Conclusion

In this work, it has been observed that channel doping does play an important role in the drain current modelling for short-channel double gate devices. A complete drain current model with mobility degradation due to various factors as well as channel length modulation has been proposed and verified with the simulated results from Sentaurus TCAD for a wide variation of doping concentrations, back gate voltages and other structural parameters. The model is efficiently able to capture all the I–V characteristics for all gate voltage ranges with a relative error percentage within 3–7%. The only disadvantage of the model is that the execution time is slightly higher due to its iterative technique which can be certainly improved by means of an efficient N-R algorithmic approach.

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