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Recessed insulator and barrier AlGaN/GaN HEMT: A novel structure for improving DC and RF characteristics

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Abstract. In this study, a gallium nitride (GaN) high electron mobility transistor (HEMT) with recessed insulator and barrier is reported. In the proposed structure, insulator is recessed into the barrier at the drain side and barrier is recessed into the buffer layer at the source side. We study important device characteristics such as electric field, breakdown voltage, drain current, maximum output power density, gate-drain capacitance, short channel effects and DC transconductance using two-dimensional and two-carrier device simulator. Recessed insulator in the drain side of the proposed structure reduces maximum electric field in the channel and therefore increases the breakdown voltage and maximum output power density compared to the conventional counterpart. Also, gate-drain capacitance value in the proposed structure is less than that of the conventional structure. Overall, the proposed structure reduces short channel effects. Because of the recessed regions at both the source and the drain sides, the average barrier thickness of the proposed structure is not changed. Thus, the drain current of the proposed structure is almost equivalent to that of the conventional transistor. In this work, length (L_r) and thickness (T_r) of the recessed region of the barrier at the source side are the same as those of the insulator at the drain side.

Keywords. AlGaN/GaN high electron mobility transistor; breakdown voltage; output power density; short channel effect; gate-drain capacitance.

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1. Introduction

High electron mobility transistors (HEMTs) have heterostructures such as AlGaN/GaN and AlGaAs/GaAs which are used in high-power and high-frequency applications extensively. This is due to their superior material characteristics such as large band gap, high saturated electron velocity, high breakdown electric field, strong spontaneous and piezoelectric polarization fields and good radiation protection. Application of GaN-based HEMTs in high-power and high-frequency circuits is more than that of GaAs-based HEMTs due to its excellent material properties [1–5]. Structural variation is one of the most important ways to improve the DC and RF characteristics in transistors. Recessed gate or channel changes electric field lines, thereby improving the breakdown voltage of MESFETs [6–8]. This motivates us to think that recessed barrier and insulator may increase the performance of a HEMT device. Therefore, in this paper, we propose a new structure with recessed insulator and barrier. The length and thickness of the recessed insulator at the drain side of the proposed structure are equivalent to those of the recessed barrier into the buffer layer at the source side. Important electrical characteristics such as electric field, breakdown voltage, output power density, gate-drain capacitance and short channel effects of the proposed structure are studied and compared with those in the conventional structure using two-dimensional ATLAS device simulator. Gate length reduction can be used to improve the transconductance and gate capacitance in a transistor. However, it is worth noting that decrease in gate length causes short channel effects such as drain-induced barrier lowering (DIBL). DIBL is an effect that changes the threshold voltage of a FET by increasing the drain voltage instead

of gate voltage. Therefore, DIBL is an important factor that affects the electrical performances of a FET with small gate length [9–12]. In this paper, this effect in the proposed structure is compared with that in the conventional structure.

The dimensions of the proposed and conventional structures and the physical models activated in the simulator are explained in §2. In §3, we first study the effect of the recessed insulator in the barrier on the electric field and breakdown voltage. Also, in this section the crucial electrical characteristics of the proposed and conventional structures such as saturated drain current, output power density, short channel effect, gate-drain capacitance, threshold voltage and transconductance for different recessed length and thickness are reported and compared.

2. Device structure

Schematic cross-sections of the proposed and conventional [1] structures are shown in figures 1a and 1b, respectively. The dimensions of the proposed and conventional structures are as follows: gate length $L_g = 0.5\ \mu$m, gate-drain spacing $L_{gd} = 1\ \mu$m, gate-source spacing $L_{gs} = 1\ \mu$m. Barrier layer and channel thicknesses are $T_B = 22$ nm and $T_C = 1.5\ \mu$m, respectively. Si_3N_4 is used as the insulator layer with the parameters mentioned in ref. [13]. The barrier layer is an n-type heavily doped $Al_{0.32}Ga_{0.68}N$ while the buffer layer is an intrinsic GaN. The recessed barrier length (L_r) and thickness (T_r) in the source side is equal to those in the recessed insulator in the drain side of the proposed structure. Therefore, to get a meaningful comparison, the average barrier thickness of the proposed structure is made equal to that of the conventional structure so that average barrier thickness is equal to that of the conventional structure. Thus, the drain current of the proposed structure is almost equal to that of the conventional transistor which makes the comparison of the two structures more meaningful. Nickel is chosen as the gate Schottky contact with a work function of 5.1 eV. The devices are simulated using two-dimensional device simulator ATLAS software [14]. In order to achieve more realistic results, several models are activated in simulations, including the 'SRH' model for Shockley–Read–Hall recombination, the 'fldmob' model for parallel electric field-dependent mobility [6,15] and the 'bgn' model for band gap narrowing.

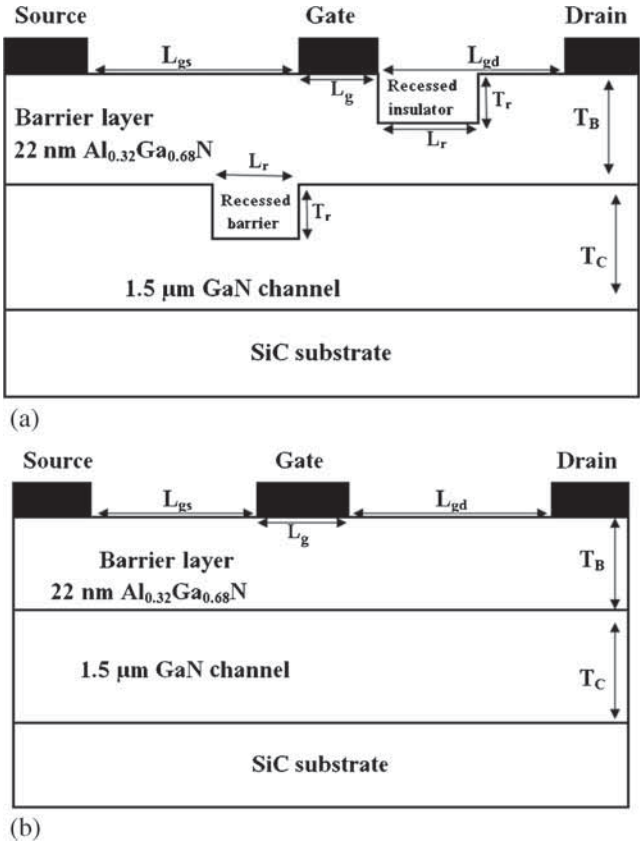


Figure 1. Cross-section of the (**a**) proposed and (**b**) conventional structures.

It is worth noting that the conventional structure can be fabricated as reported in [16]. To fabricate the proposed structure, at first, the substrate and GaN channel (buffer) can be created by metal-organic chemical vapour deposition (MOCVD) [16]. Ion implantation process can be used to produce the barrier recess into the buffer. Post annealing is used to reduce the degradation of ion implantation. To create the insulator recess into the barrier layer, the easiest way is to pattern recess the location with PR in the barrier layer and deposit the insulator at room temperature using sputtering. Contact formation for the source, gate and drain and device isolation can be as similar as the process reported in [16].

3. Results and discussion

Lateral electric fields of the proposed and conventional structures for different T_r and L_r at $V_{DS} = 80$ V and $V_{GS} = -5$ V are illustrated in figures 2a and 2b. The breakdown usually happens in the gate corner near the drain due to electric field crowding [7,8]. Lateral electric field in the barrier or buffer layer has a direct relation with the two-dimensional electron gas (2-DEG) concentration (n_s). Recessed insulator in the

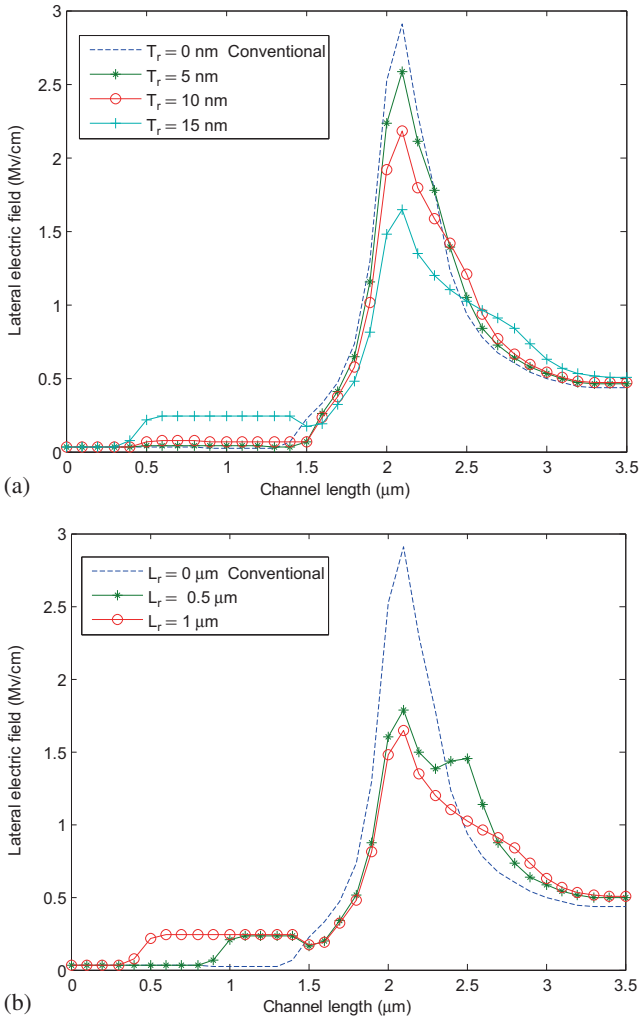


Figure 2. Lateral electric field as a function of the channel length for (**a**) different T_r at a fixed L_r (1 μm) and (**b**) different L_r at a fixed T_r (15 nm) in the proposed and conventional structures at $V_{GS} = -5$ V and $V_{DS} = 80$ V.

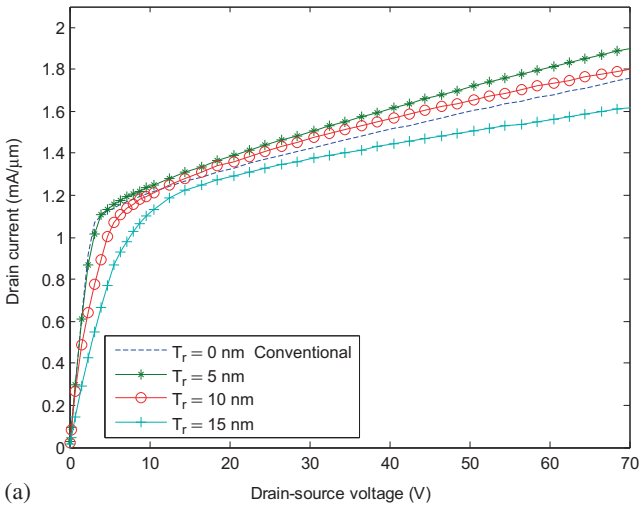
proposed structure is located in the drain side. So, this recessed insulator can reduce n_s and then decrease maximum lateral electric field in the drain side compared to the conventional structure. Consequently, this can improve the breakdown voltage. Maximum lateral electric field is increased by increasing the drain voltage. Breakdown is the drain voltage at which the maximum electric field reaches its critical value. Critical electric field of GaN is about 3.5 MV/cm [9]. As evident from these figures, increasing L_r and T_r reduces the maximum lateral electric field in the channel. In this condition ($V_{DS} = 80$ V and $V_{GS} = -5$ V), maximum lateral electric field of the structures is less than the critical electric field. Therefore, breakdown voltage of the proposed and conventional structures is larger than 80 V. Moreover, simulation results demonstrate that the breakdown voltage of the proposed structures is larger than that of the conventional structure. The breakdown voltages of the proposed structures with $L_r = 0.5$ μm and 1 μm at a fixed T_r (15 nm) are about 280 V and 300 V, respectively. The lateral electric field with $T_r = L_r = 0$ μm corresponds to the conventional structure. Breakdown voltage of the conventional structure is about 120 V. Also, the breakdown voltages of the proposed structures with $T_r = 5$ nm, 10 nm and 15 nm at a fixed L_r (1 μm) are about 170 V, 230 V and 300 V, respectively. It can be concluded that the proposed structures with different L_r and T_r have higher breakdown voltages than that in the conventional structure. The largest breakdown voltage is obtained at $L_r = 1$ μm and $T_r = 15$ nm. In summary, it can be stated that recessed insulator in the barrier of the proposed structures decreases the maximum electric field and consequently increases the breakdown voltage. The breakdown voltage of the proposed structure (~300 V) is significantly improved compared to the conventional transistor (~120 V).

Drain currents with respect to the drain-source voltages of the proposed structures for different L_r and T_r are plotted and compared with that of the conventional structure at $V_{GS} = 0$ V in figures 3a and 3b. Product of the barrier doping and thickness ($N \times a$) is an important factor in determining the drain current [7]. Recessed length and thickness of the insulator in the barrier is the same as those of the barrier in the buffer layer in the proposed structures. So, average thickness of the channel in the proposed structures is equal to that in the conventional structure. However, it is worth noting that recessed barrier is located at the source side while the recessed insulator is in the drain side. Thus, the barrier thickness in the source side of the proposed structures is larger than that of the conventional structure. It is clear from figures 3a and 3b that the proposed structures change drain currents slightly compared to the drain currents in the conventional structure. The saturated drain current of the proposed structures is increased by decreasing T_r at a fixed L_r (1 μm). The maximum saturated drain current is obtained for the proposed structure with $L_r = 1$ μm and $T_r = 5$ nm.

The maximum theoretical output power density (P_{max}) for a Class A amplifier is given as [6]

$$P_{max} = \frac{I_{Dsat}(V_B - V_{knee})}{8}, \quad (1)$$

where I_{Dsat} is the saturated drain current, V_{knee} is the knee voltage and V_B is the breakdown voltage. Using the above equation, the maximum output power density can be calculated. As shown in figures 3a and 3b, the saturated drain currents of the proposed structures



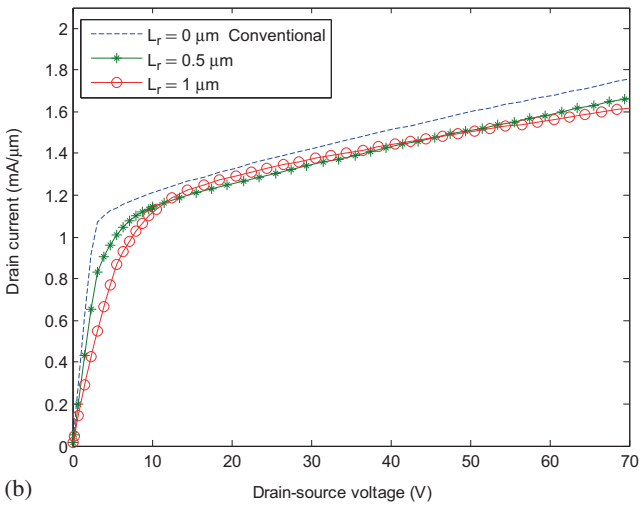
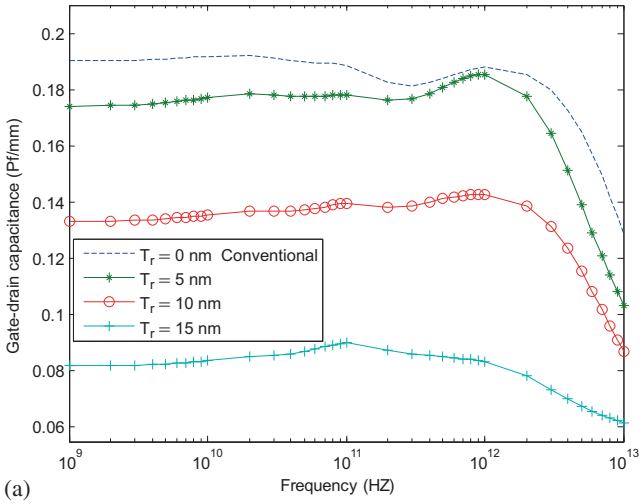


Figure 3. Drain current as a function of drain voltage for (**a**) different T_r at a fixed L_r (1 μm) and (**b**) different L_r at a fixed T_r (15 nm) in the proposed and conventional structures at $V_{GS} = 0$ V.



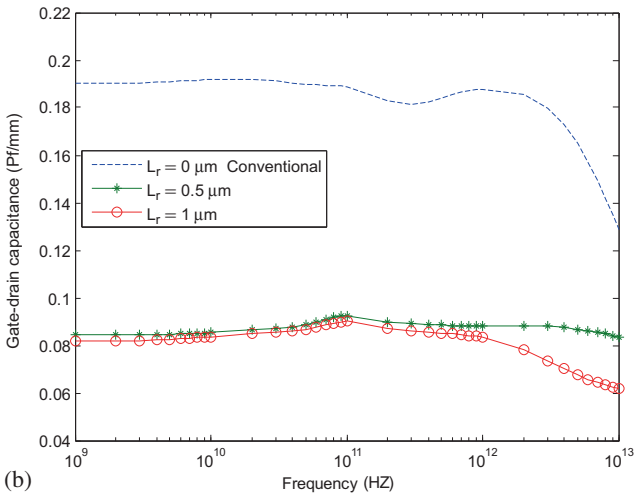


Figure 4. Gate-drain capacitance as a function of frequency for (**a**) different T_r at a fixed L_r (1 μm) and (**b**) different L_r at a fixed T_r (15 nm) in the proposed and conventional structures at $V_{GS} = 0$ V and $V_{DS} = 20$ V.

are equivalent to that in the conventional structure. But as discussed above, the breakdown voltage of the proposed structure is about 150% larger than that of the conventional structure. As a result, the maximum power density of the proposed structure is significantly (∼150%) larger than that in the conventional structure. Therefore, it can be concluded that the proposed structure has superior power and breakdown performances compared to the conventional structure.

Gate-drain capacitances as a function of frequency for different L_r and T_r for the proposed structure are shown in figures 4a and 4b at $V_{GS} = 0$ V and $V_{DS} = 20$ V. Recessed insulator in the drain side reduces the barrier thickness and consequently decreases net electron density in this side of the channel. This decreases the gate-drain capacitance of the proposed structure compared to that of the conventional structure [9]. According to these figures, increasing L_r and T_r in the proposed structures reduces the gate-drain capacitance. It is worth noting that the reduction in gate-drain capacitance due to an increase in T_r is more significant than that due to an increase in L_r. The minimum gate-drain capacitance is achieved for the proposed structure with $L_r = 1$ μm and $T_r = 15$ nm. Therefore, the high-frequency performance of the proposed structure is better than the conventional one.

Drain current vs. gate-source voltage of the proposed and conventional structures at $V_{DS} = 10$ V is shown in figure 5. L_r and T_r for the proposed structure are 1 μm and 15 nm, respectively. For these values, the threshold voltages of the proposed and conventional structures are about −12 V and −13 V, respectively. This is due to the thickness and length of the recessed insulator

and barrier that decreases net electron density in the barrier of the proposed structure and so increases the threshold voltage slightly compared to the conventional structure.

The negative shift of the threshold voltage by increasing the drain voltage is known as DIBL. The negative shift of the threshold voltage with respect to the increase in the drain voltage in the proposed and conventional structures is plotted in figure 6. L_r and T_r of the proposed structure are 1 μm and 15 nm, respectively. According to this figure, the negative shift of the threshold voltage in the proposed structure is less than that of the conventional structure. Thus, it can be deduced that the proposed structure is more robust against short channel effects such as DIBL. As can be seen in the figure, the negative shifts in the threshold voltage of the proposed and conventional structures are about -8.5 V and -10.5 V, respectively. This is due to the existence of the recessed insulator in the proposed structure that reduces the lateral electric field and then decreases the threshold voltage dependence on the drain voltage. Also, it is worth noting that we determine the threshold voltage using the conventional definition involving an abrupt transition between turn-on and turn-off operations [17].

The DC transconductance (g_m) can be calculated by differentiating the drain current with respect to the

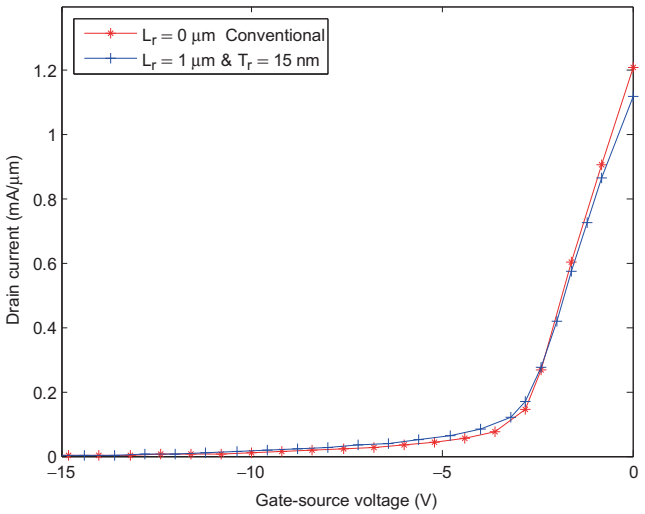


Figure 5. Drain current as a function of gate-source voltages in the proposed ($L_r = 1$ μm and $T_r = 15$ nm) and conventional structures at $V_{DS} = 10$ V.

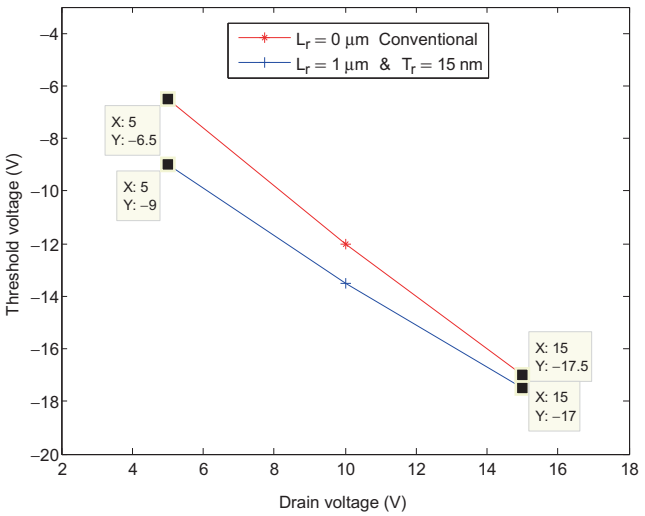
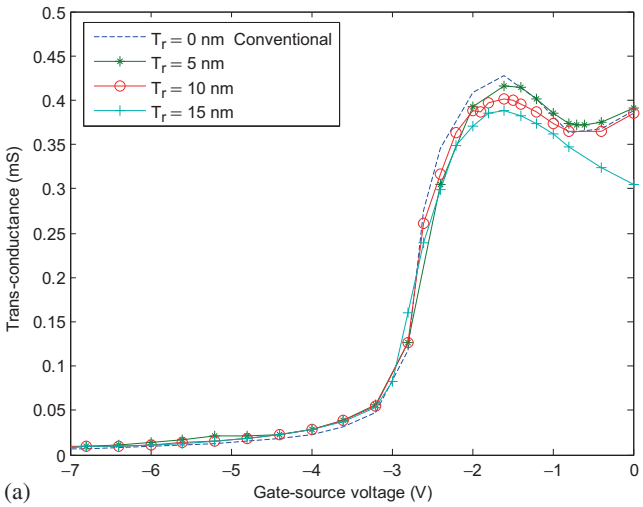


Figure 6. Threshold voltage as a function of drain voltage in the proposed ($L_r = 1$ μm and $T_r = 15$ nm) and conventional structures.



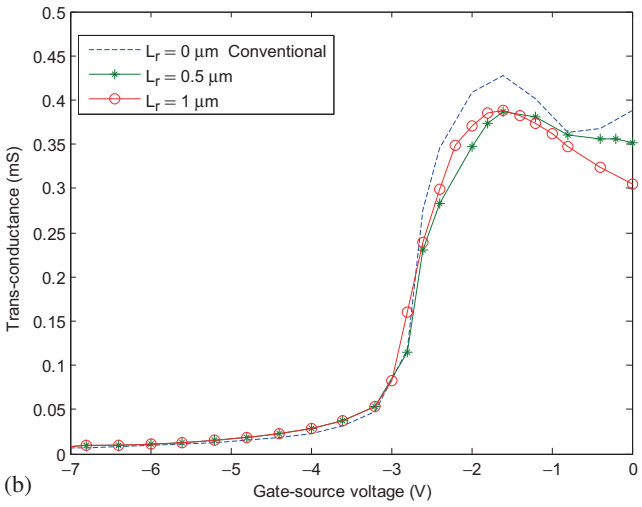


Figure 7. DC transconductance as a function of gate-source voltages for (**a**) different T_r at a fixed L_r (1 μm) and (**b**) different L_r at a fixed T_r (15 nm) in the proposed and conventional structures at $V_{DS} = 10$ V.

gate-source voltage at a constant drain-source voltage [18]:

$$g_{\mathrm{m}} = \left.\frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}}\right|_{V_{\mathrm{DS}}=\mathrm{const}}. \quad (2)$$

g_{m} shows the dependence of the drain current on the gate-source voltage at a fixed drain-source voltage. The DC transconductance vs. the gate-source voltages for different L_{r} and T_{r} in the proposed and conventional structures at $V_{\mathrm{DS}} = 10$ V are plotted in figures 7a and 7b. As evident from figure 7a, decreasing T_{r} in the proposed structure improves the maximum DC transconductance. Also, figure 7b reveals that increasing L_{r} reduces DC transconductance. But, the proposed structure with different L_{r} and T_{r} exhibits slightly lower g_{m} compared to the conventional one. This is due to thicker barrier in the source side of the proposed structure that reduces the electron flow dependence to the gate-source voltage. Drain current in a HEMT is effectively related to the electron motion and concentration (n_{s}) of 2-DEG. Gate-source voltage produces a vertical electric field on the carriers moving in 2-DEG from source to drain contact. Therefore, g_{m} indicates the effect of vertical electric field on the 2-DEG electrons. In the proposed structure, 2-DEG has a stepping shape and is located away from the gate at the source side. So, the electric field produced by the gate-source voltage in the source side is reduced in 2-DEG which consequently decreases g_{m}. The maximum g_{m} for the proposed structure is obtained at $L_{\mathrm{r}} = 1$ μm and $T_{\mathrm{r}} = 5$ nm.

4. Conclusion

In this work, we proposed a new AlGaN/GaN HEMT structure that improves electrical characteristics compared to those of the conventional structure. Recessed insulator in the drain side of the proposed structure reduces the maximum lateral electric field and therefore improves the breakdown voltage. Increasing breakdown voltage of a transistor improves output power density. The breakdown voltage of the proposed structure is about 300 V that is 150% larger than that in the conventional structure (∼120 V). Also, the proposed structure reduces short channel effects and gate-drain capacitance significantly compared to those of the conventional structure.

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