PRAMANA — journal of physics

Vol. 85, No. 6
December 2015
pp. 1221–1232

Impact of oxide thickness on gate capacitance – Modelling and comparative analysis of GaN-based MOSHEMTs

KANJALOCHAN JENA, RAGHUNANDAN SWAIN and T R LENKA*
Department of Electronics and Communication Engineering, National Institute of Technology, Silchar 788 010, India
*Corresponding author. E-mail: trlenka@gmail.com

MS received 23 April 2014; revised 20 September 2014; accepted 26 September 2014
DOI: 10.1007/s12043-015-0948-1; ***e*Publication:** 20 May 2015

Abstract. In this paper, we have developed a mathematical model to predict the behaviour of gate capacitance and threshold voltage with nanoscale variation of oxide thickness in AlInN/GaN and AlGaN/GaN metal oxide semiconductor high electron mobility transistor (MOSHEMT). The results obtained from the model are compared with the TCAD simulation results to validate the model. It is observed that AlInN/GaN MOSHEMT has an advantage of significant decrease in gate capacitance up to 0.0079 pF/μm^2 with increase in oxide thickness up to 5 nm as compared to conventional AlGaN/GaN MOSHEMT. This decrease in gate capacitance in AlInN/GaN MOSHEMT reduces the propagation delay and hence improves the RF performance of the device.

Keywords. Two-dimensional electron gas; GaN; metal oxide semiconductor high electron mobility transistor; quantum capacitance; TCAD.

PACS Nos 70; 60

1. Introduction

GaN-based high electron mobility transitors (HEMTs) are the most preferred devices for high-power and high-frequency applications due to their suitable material properties such as high breakdown voltage, high saturation velocity, low effective mass, high thermal conductivity and high two-dimensional electron gas (2DEG) density of the order of 10^{13} cm^{-2} at the heterointerface [1–4].

However, recently GaN-based MOSHEMT has played very important roles in high-frequency applications due to the role of MOS capacitor in device operation whereas in conventional HEMT, Schottky barrier diode is formed at the gate electrode. The MOS capacitor formed in MOSHEMT has equivalent gate capacitance which is the series combination of oxide capacitance (C_{ox}) and inversion-layer capacitance (C_{inv}) [2]. The inversion-layer capacitance is inherent to all MOSHEMT structures and this capacitance has a significant influence on the performance of scaled-down devices with thin gate

oxide [3]. The gate capacitance determines the RF performance and propagation delay in MOSHEMT which is limited by the inversion-layer capacitance. However, the inversion-layer capacitance is primarily contributed by the quantum capacitance (QC) formed in the 2DEG [3]. Therefore, in this context the researchers are keen to observe the influence of variation of oxide thickness on threshold voltage and gate capacitance relating QC and hence have developed a mathematical model which is presented in this paper.

The distinction between conventional AlGaN/GaN and AlInN/GaN MOSHEMTs along with the effect of QC and its influence on device performance has been explained in §2. A mathematical model has been developed by establishing the relationship between gate capacitance and oxide thickness relating QC is presented in §3. The dependence of threshold voltage model on oxide thickness for MOSHEMT is presented in §4. The results and discussion are presented in §5 and finally, the conclusion is drawn in §6.

2. Quantum capacitance in heterostructures

For an unintentionally doped AlGaN/GaN MOSHEMT structure the 2DEG is formed largely as a result of piezoelectric and spontaneous polarization effects which arise at the heterointerface of the AlGaN/GaN layer [4]. But for scaled devices, as the oxide thickness, barrier thickness and gate lengths are reduced, the sheet carrier density decreases due to the proximity of the heterointerface to the negatively charged surface [5]. To further increase the 2DEG density as well as the breakdown field in AlGaN structure, high Al mole fraction is desirable as it increases the strength of polarization. But high Al content will affect the transport properties in the AlGaN/GaN heterostructure [6].

To solve this problem, a thin lattice-matched $Al_{0.83}In_{0.17}N$ layer is grown over GaN which eliminates the strain in the conventional AlGaN-based MOSHEMT. The band gap of AlInN is larger than that of AlGaN and has larger spontaneous polarization charges. This large conduction band discontinuity leads to the formation of high 2DEG density at the heterointerface resulting in high current density compared to conventional AlGaN/GaN MOSHEMT [7].

Figure 1 shows a schematic diagram of the AlInN/GaN heterostructure used in this study. It consists of a metal gate followed by the Al_2O_3 layer, $Al_{0.83}In_{0.17}N$ barrier layer of 6 nm thickness, an unintentionally doped GaN channel of thickness 500 nm,

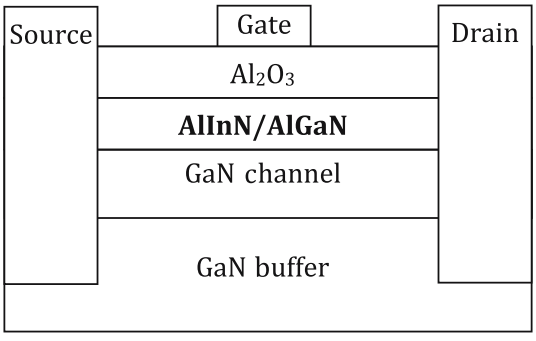

Figure 1. The proposed MOSHEMT structure.

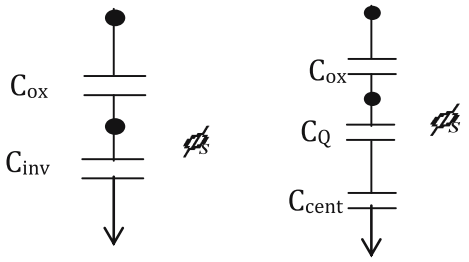

Figure 2. Equivalent circuit diagrams for gate capacitance in AlInN/GaN MOSHEMT.

and semi-insulating GaN buffer layer of 1 μm thickness. The total gate capacitance of the AlInN/GaN MOSHEMT can be expressed as a series combination of oxide capacitance C_{ox} and inversion capacitance C_{inv} [1]. The inversion layer capacitance C_{inv} can be represented as a series combination of the QC, C_Q and centroid capacitance, C_{cent}.

From figure 2 it is well understood that the total gate capacitance C_G can be determined by the smallest gate capacitance components such as C_{ox}, C_Q and C_{cent}. However, the oxide capacitance is inversely proportional to the oxide thickness.

Ideally, the inversion layer capacitance C_{inv} is much larger than the oxide capacitance C_{ox} in strong inversions and gate capacitance C_G approaches the oxide capacitance C_{ox} in large-scaled devices. However, in nanoscale devices, as the oxide thickness approaches the nanometer regime, the oxide capacitance C_{ox} becomes comparable to the inversion layer capacitance C_{inv} which means that the quantum capacitance C_Q and the centroid capacitance C_{cent} start to affect the gate capacitance [8]. The centroid capacitance C_{cent} is related to the average physical distance of the electrons present in the quantum well/2DEG from the metal gate [2]. In the case of AlInN/GaN MOSHEMT, the carriers are confined better in the 2DEG and all charge carriers are assumed to be located at the same position inside the quantum well and hence the centroid capacitance C_{cent} can be neglected.

The concept of QC was first introduced by Luryi [9] and it originates from the penetration of Fermi energy level (E_F) into the conduction band. Therefore, the channel material plays a very significant role in determining QC.

In AlInN/GaN MOSHEMT, a 2DEG is formed in the heterostructure quantum well as shown in figure 3 due to the finite density of states (DoS). As a result, Fermi level needs

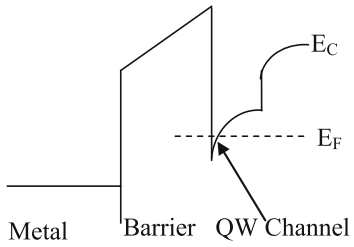

Figure 3. Quantum well/2DEG formation due to the conduction band discontinuity.

to move up above the conduction band edge as the charge in the quantum well increases. This movement of Fermi level requires energy and it corresponds to the origin of QC. To induce channel charge in a MOS structure we need to deliver an amount of energy equal to $Q_s^2/2C_{ox} + Q_s^2/2C_Q$, where Q_s is the total electron charge in 2DEG. The first term corresponds to the energy required for the electric field in the oxide layer and the second term is related to the energy required to create 2DEG. But as C_{ox} is comparable, even bigger than C_Q, as the device scaling approaches a few nanometers, C_Q should be considered carefully in the scaled-down devices to indicate gate capacitance. The problem is especially severe in III–V MOSHEMT due to their relatively small effective mass which reduces the QC.

3. Model development

For MESFET the sheet charge density is given by [7,10]

$$n_s = \sigma_{pol} - \frac{\varepsilon_{AlInN}}{qd_{AlInN}}\left[\phi_s + E_F - \Delta E_C\right], \tag{1}$$

where σ_{pol} is the induced charge concentration due to spontaneous polarization, ε_{AlInN} is the permittivity for AlInN, d_{AlInN} is the barrier thickness, E_F is the Fermi potential of GaN layer, ϕ_s is the surface potential and ΔE_C is the discontinuity of the conduction band at the interface between the AlInN and the GaN layers.

3.1 *Dependence of n_s on oxide thickness*

Figure 4 demonstrates the energy band diagram of a MOSHEMT structure. The levels above the neutral level are acceptor states and levels below are the donor states.

As per the classical approach, all the levels above the Fermi level are considered to be devoid of electrons, i.e., donors, while those below are filled. This results in the ionized

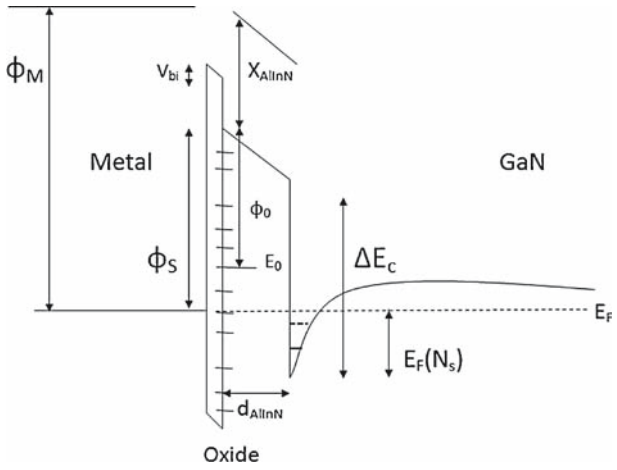

Figure 4. Conduction band profile for a metal/oxide/AlInN/GaN interface.

state of the donor traps while the acceptor traps are neutral. It causes an extra positive interface charge to be contributed by these states which is given by

$$Q_{\text{it}} = D_{\text{it}} q^2 \left(E_0 - E_{\text{F}}\right). \tag{2}$$

Here D_{it} is the interface density of states, Q_{it} is the interface charge, E_0 and E_{F} are the neutral and Fermi level potentials, respectively, which denote that all the states between E_0 and E_{F} are ionized.

This donor charge along with the polarization charge results in a residual potential V_{bi} which can be given by

$$V_{\text{bi}} = \frac{Q_{\text{D}} + Q_{\text{it}}}{C_{\text{oxide}}}, \tag{3}$$

where Q_{D} is the depletion charge and $C_{\text{oxide}} = \varepsilon_{\text{oxide}}/t_{\text{oxide}}$ is the oxide capacitance. t_{oxide} is the Al_2O_3 layer thickness and $\varepsilon_{\text{oxide}}$ is the dielectric constant of the Al_2O_3 layer. The depletion charge can be formulated as

$$Q_{\text{D}} = q N_{\text{D}} d_{\text{AlInN}}. \tag{4}$$

Using eqs (2)–(4) we obtain

$$V_{\text{bi}} = \frac{q N_{\text{D}} d_{\text{AlInN}} + D_{\text{it}} q^2 \left(E_0 - E_{\text{F}}\right)}{C_{\text{oxide}}}. \tag{5}$$

From figure 4 it is clear that the surface potential $\phi_{\text{s}} = \phi_{\text{M}} - \chi_{\text{AlInN}} - V_{\text{bi}}$ and $E_0 - E_{\text{F}} = \phi_{\text{s}} - \phi_0$, where ϕ_{M} is the metal work function, χ_{AlInN} is the electron affinity for AlInN, V_{bi} is the residual interface potential and ϕ_0 is the potential difference between the neutral level and the conduction band edge. Introducing these terms in eq. (5), a relation between the surface potential and barrier thickness can be obtained as

$$\phi_{\text{s}} = \gamma(\phi_{\text{M}} - \chi_{\text{AlInN}}) + (1 - \gamma)\phi_0 - \frac{\gamma q N_{\text{D}} d_{\text{AlInN}}}{C_{\text{oxide}}}, \tag{6}$$

where

$$\gamma = \frac{1}{1 + D_{\text{it}} q^2 / C_{\text{oxide}}}.$$

The dependence of 2DEG sheet charge density and thickness on surface potential can be seen from eqs (1) and (6). Using these equations one can obtain the 2DEG sheet charge density with respect to eq. (7) as

$$n_{\text{s}} = \sigma_{\text{pol}} - \frac{\varepsilon_{\text{AlInN}}}{q d_{\text{AlInN}}} \left[\gamma(\phi_{\text{M}} - \chi_{\text{AlInN}}) + (1 - \gamma)\phi_0 - \frac{\gamma q N_{\text{D}} d_{\text{AlInN}}}{C_{\text{oxide}}} + E_{\text{F}} - \Delta E_{\text{C}} \right]. \tag{7}$$

The self-consistent solution of Schrödinger and Poisson equations provides two discrete energy levels (E_0 and E_1) to be occupied in the 2DEG resulting in the following relation [4,10]:

$$n_{\text{s}} = DkT \sum_{i=0,1} \ln\left(1 + \exp\left(\frac{E_{\text{F}} - E_{\text{i}}}{kT/q}\right)\right), \tag{8}$$

where $D = 4\pi m^*/h^2$ is the conduction band density of states of a 2D system, m^* is the electron effective mass, h is the Planck's constant, k is the Boltzmann's constant, T is the ambient temperature, $E_0 = c_0 n_s^{2/3}$ (eV) and $E_1 = c_1 n_s^{2/3}$ (eV) are the allowed energy levels in the quantum well. Here c_0 and c_1 are determined by the Robin boundary conditions [11,12].

However, the Fermi level can be expressed by a second-order expression as given by Kola *et al* [13], which gives a good fitting to the numerical solution of eq. (1), where E_F is defined as

$$E_F = k_1 + k_2 n_s^{1/2} + k_3 n_s. \tag{9}$$

k_1, k_2 and k_3 have been calculated as in [13]. Using eqs (9) and (1) and solving for n_s, we get

$$n_s = \left[-A + \sqrt{A^2 - (B + C\phi_s - F)}\right]^2, \tag{10}$$

where

$$A = \frac{\varepsilon k_2}{2\,(\varepsilon k_3 + qd)}, \tag{11}$$

$$B = \frac{\varepsilon\,(k_1 - \Delta E_C)}{(\varepsilon k_3 + qd)}, \tag{12}$$

$$C = \frac{\varepsilon}{(\varepsilon k_3 + qd)}, \tag{13}$$

$$F = \frac{dq\sigma}{(\varepsilon k_3 + qd)}. \tag{14}$$

3.2 *Calculation of gate capacitance (C_G)*

By omitting the centroid capacitance C_{cent}, the quantum capacitance C_Q can be obtained as

$$C_Q = \frac{\partial(qn_s)}{\partial\phi_s}. \tag{15}$$

Calculating the above differentiation we obtain

$$C_Q = q\frac{C\left[-A + \sqrt{A^2 - (B + C\phi_s - F)}\right]}{\sqrt{A^2 - (B + C\phi_s - F)}}. \tag{16}$$

The gate capacitance due to series combination of C_Q and C_{ox} can be given as

$$C_G = \frac{C_Q \times C_{ox}}{C_Q + C_{ox}}. \tag{17}$$

4. Threshold voltage model for MOSHEMT

The threshold voltage model of MOSHEMT can be derived in relation with the oxide thickness and other device parameters. In order to completely cut-off the MOSHEMT it is required to make the 2DEG devoid of electrons, for which external potential has to be applied from the gate terminal. As can be seen in figure 5, under this condition the difference in Fermi energy level and the lowest energy level of electrons in the 2DEG reduces to zero. Hence the 2DEG density n_s and $E_F(n_s)$ becomes zero. Using these two conditions and replacing ϕ_s with $\phi_s = \phi_{s0} - V_T$ in eq. (1) and solving for V_T we obtain the expression for threshold voltage as shown in eq. (18), where ϕ_{s0} can be derived from eq. (6)

$$V_T = \gamma(\phi_M - \chi_{AlInN}) + (1-\gamma)\,\phi_0 - \frac{\gamma q N_D d_{AlInN}}{C_{oxide}} - \Delta E_C - \frac{\sigma_{pol} q d_{AlInN}}{\varepsilon_{AlInN}}. \quad (18)$$

5. Results and discussion

The proposed model is validated by comparing the results with the Silvaco ATLAS device simulator [14]. In the device simulation, parameters such as the operating temperature as 300 K, gate voltage step as 0.2 V, an initial gate voltage of -1 V and final gate voltage of 3 V, respectively for a 6 μm gate length device are considered which are kept constant for all the device simulations with various oxide thicknesses.

The threshold voltage derived in eq. (18) is plotted in figure 6 by MATLAB and validated by TCAD simulation results. It is observed that the threshold voltage decreases from 0.3 V with an oxide thickness of 2 nm to approximately -1.1 V at about 10 nm of oxide thickness. The obtained threshold voltage is characteristic with the variation of oxide thickness and is in good agreement with the experimental results obtained by Bera *et al* [15].

Then, eq. (17) is plotted in MATLAB by using the necessary parameter values for AlInN/GaN and AlGaN/GaN MOSHEMT to graphically check the dependence of gate

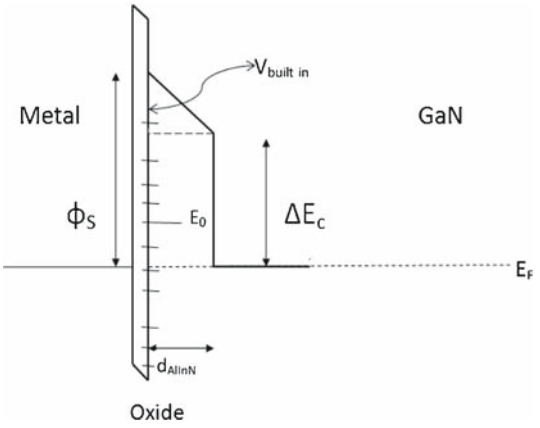

Figure 5. Conduction band at pinch-off.

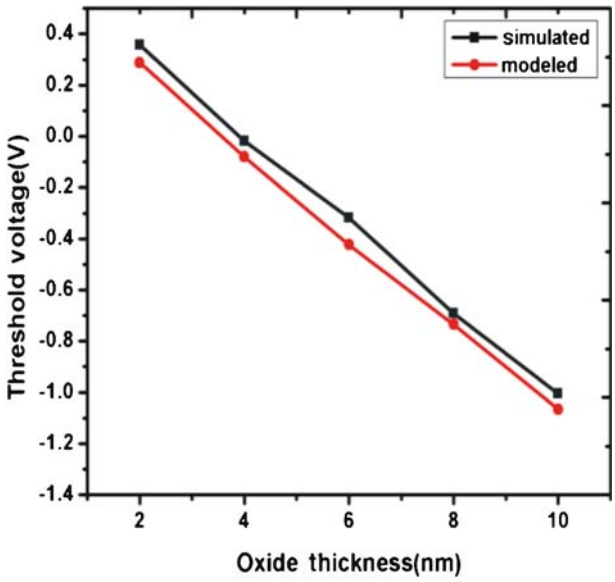

Figure 6. Plot showing threshold voltage (V_T) vs. oxide thickness for AlInN/GaN MOSHEMT.

capacitance on oxide thickness. It is observed from figure 7 that with the increase in oxide thickness the gate capacitance decreases which is validated by TCAD simulation results.

Tables 1 and 2 show the simulation results of gate capacitance for AlInN/GaN MOSHEMT and AlGaN/GaN MOSHEMT at a constant drain voltage of 1 V.

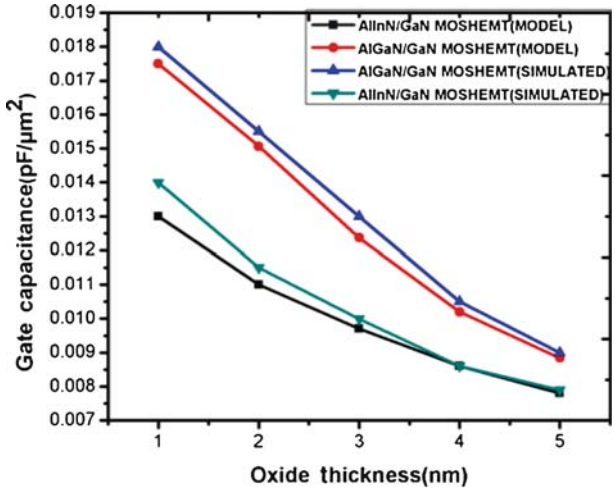

Figure 7. Plot showing gate capacitance (C_G) vs. oxide thickness for AlInN/GaN and AlGaN/GaN MOSHEMTs.

Table 1. Gate capacitance vs. gate voltage at different barrier thicknesses for AlInN/GaN MOSHEMT.

AlInN/GaN MOSHEMT					
	Gate capacitance (pF/μm^2)				
Voltage (V)	$T_{ox} = 1$ nm	$T_{ox} = 2$ nm	$T_{ox} = 3$ nm	$T_{ox} = 4$ nm	$T_{ox} = 5$ nm
−1	5.71E–03	5.58E–03	5.58E–03	5.52E–03	5.43E–03
−0.7	5.71E–03	5.59E–03	5.58E–03	5.54E–03	5.43E–03
−0.4	5.72E–03	5.57E–03	5.57E–03	5.54E–03	5.42E–03
−0.1	5.66E–03	5.58E–03	5.57E–03	5.44E–03	5.42E–03
0.2	5.92E–03	5.46E–03	5.45E–03	5.43E–03	5.40E–03
0.5	8.80E–03	7.99E–03	6.76E–03	6.05E–03	6.05E–03
0.8	1.30E–02	1.12E–02	1.09E–02	8.00E–03	7.51E–03
1.1	1.36E–02	1.13E–02	1.16E–02	8.29E–03	7.60E–03
1.4	1.38E–02	1.14E–02	1.16E–02	8.32E–03	7.62E–03
1.7	1.39E–02	1.15E–02	1.17E–02	8.37E–03	7.65E–03
2	1.39E–02	1.15E–02	1.17E–02	8.40E–03	7.70E–03
2.3	1.39E–02	1.15E–02	1.18E–02	8.49E–03	7.72E–03
2.6	1.40E–02	1.15E–02	1.19E–02	8.53E–03	7.81E–03
3	1.40E–02	1.16E–02	1.19E–02	8.60E–03	7.90E–03

It can be observed from tables 1 and 2 that as the oxide thickness increases from 1 to 5 nm, the gate capacitance decreases significantly with the increase in gate voltage.

The C–V characteristics of AlInN/GaN and AlGaN/GaN MOSHEMTs are plotted in figures 8 and 9, respectively. These plots show that at a very low gate voltage such as

Table 2. Gate capacitance vs. gate voltage at different barrier thicknesses for AlGaN/GaN MOSHEMT.

AlGaN/GaN MOSHEMT					
	Gate capacitance (pF/μm^2)				
Voltage (V)	$T_{ox} = 1$ nm	$T_{ox} = 2$ nm	$T_{ox} = 3$ nm	$T_{ox} = 4$ nm	$T_{ox} = 5$ nm
−1.0	4.50E–04	4.00E–04	4.20E–04	5.50E–04	5.50E–04
−0.7	4.60E–04	4.20E–04	4.30E–04	5.50E–04	5.50E–04
−0.4	4.70E–04	5.00E–04	5.50E–04	5.50E–04	5.60E–04
−0.1	4.70E–04	5.10E–04	5.60E–04	5.60E–04	5.60E–04
0.2	4.80E–04	5.40E–04	5.70E–04	5.60E–04	5.60E–04
0.5	5.60E–04	5.60E–04	5.70E–04	5.60E–04	5.60E–04
0.8	5.80E–04	5.70E–04	5.80E–04	5.80E–04	5.70E–04
1.1	4.13E–03	5.90E–03	4.75E–03	4.05E–03	4.54E–03
1.4	1.67E–02	1.54E–02	1.05E–02	7.94E–03	7.40E–03
1.7	1.76E–02	1.54E–02	1.29E–02	9.62E–03	8.69E–03
2.0	1.84E–02	1.54E–02	1.31E–02	9.94E–03	8.95E–03
2.3	1.85E–02	1.55E–02	1.34E–02	1.00E–02	9.01E–03
2.6	1.86E–02	1.55E–02	1.34E–02	1.01E–02	9.05E–03
3.0	1.86E–02	1.56E–02	1.35E–02	1.05E–02	9.10E–03

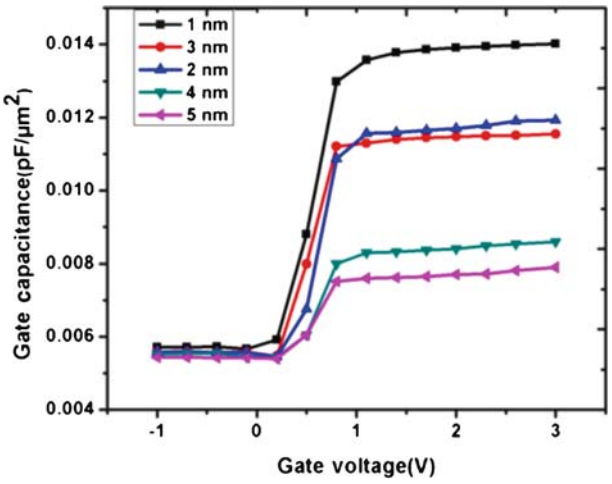

Figure 8. Plot showing gate capacitance vs. gate voltage for different oxide thicknesses of AlInN/GaN MOSHEMT.

at −0.8 and −1 V the value of gate capacitance is constant and almost the same for all oxide thicknesses as the device has not yet reached its threshold voltage level. As the gate voltage increases from 0 to 1 V there is a transition of gate capacitance from low to high but with further increase in gate voltage it remains constant.

In figure 10, the gate capacitance C_G for different oxide thicknesses at a gate voltage of 2 V is shown. It can be observed that at a particular oxide thickness, the gate capacitance is lesser for AlInN/GaN than for AlGaN/GaN MOSHEMT. It can be explained that in AlInN/GaN MOSHEMT, 83% Al content leads to more polarizations and more charge carrier confinement resulting in less density of states near the quantum well, leading to less quantum capacitance, whereas in AlGaN/GaN MOSHEMT, as there is comparatively

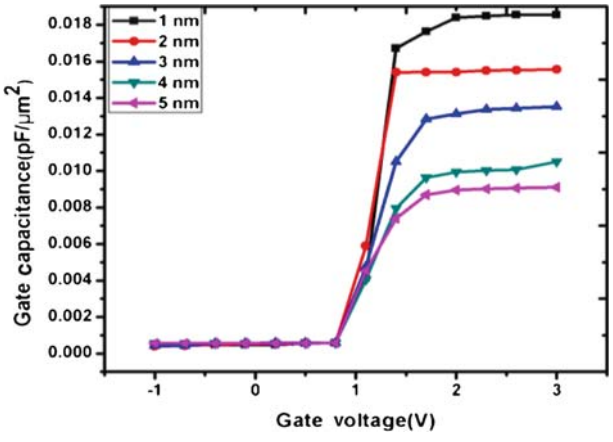

Figure 9. Plot showing gate capacitance vs. gate voltage for different oxide thicknesses in AlGaN/GaN MOSHEMT.

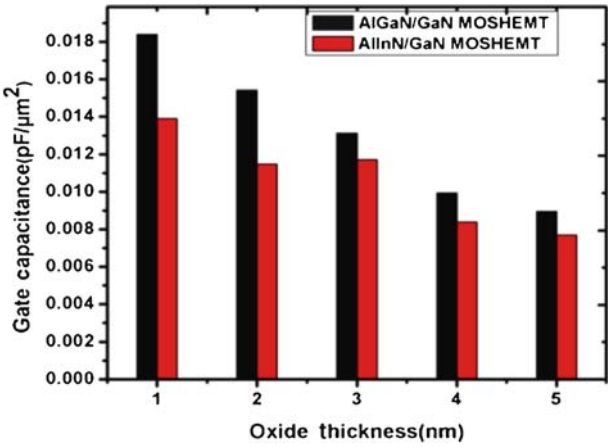

Figure 10. Plot showing gate capacitance vs. oxide thickness at a gate voltage of 2 V.

low polarization effect, resulting in less carrier confinement in the 2DEG, leading to more quantum capacitance and hence more gate capacitance C_G. However, more gate capacitance is not preferable for RF applications because of its propagation delay and speed limitation.

6. Conclusion

In this study, a mathematical model is developed to predict the behaviour of threshold voltage and gate capacitance with nanoscale variation of oxide thickness in AlInN/GaN and AlGaN/GaN MOSHEMTs. It is seen that the threshold voltage decreases from 0.3 to -1.1 V with the variation of oxide thickness from 2 to 10 nm, respectively. It is also observed that AlInN/GaN MOSHEMT has an advantage of significant decrease in gate capacitance up to 0.0079 pF/μm^2 with the increase in oxide thickness up to 5 nm as compared to the conventional AlGaN/GaN MOSHEMT. It is concluded that in nanoscale regime, AlInN/GaN MOSHEMT shows better performance than the conventional AlGaN/GaN MOSHEMT due to less gate capacitance which leads to reduced propagation delay and improved RF performance.

Acknowledgement

The authors acknowledge the Microelectronics Computational Laboratory under the Department of ECE at the National Institute of Technology, Silchar, India for providing all necessary facilities to carry out the research work.

References

[1] S Takagi and A Toriumi, *IEEE Trans. Electron. Devices* **42**, 2125 (1995)

[2] S Pal, K D Cantely, S S Ahmed and M S Lundstrom, *IEEE Trans. Electron. Devices* **55**(**3**), 904 (2008)
[3] F M Yigletu, S Khandelwal, T A Fjeldly and B Iniguez, *IEEE Trans. Electron. Devices* **60**(**11**), 3746 (2013)
[4] T R Lenka and A K Panda, *Indian J. Pure Appl. Phys.* **49**(**6**), 416 (2011)
[5] M Higashiwaki, T Matsui and T Mimura, *IEEE Electron. Device Lett.* **27**(**1**), 16 (2008)
[6] F Nakamura, S Hashimoto, M Hara, S Imanaga, M Ikeda and H Kawai, *J. Crystal Growth* **195**(**4**), 280 (1998)
[7] D Pandey and T R Lenka, *J. Semiconductors* **35**(**10**) (2014)
[8] S K Sinha and S Chaudhury, *IEEE Trans. Nanotechnol.* **12**(**6**), 958 (2013)
[9] S Luryi, *Appl. Phys. Lett.* **52**(**6**), 501 (1988)
[10] O Ambacher, J Smart, J R Shealy, N G Weimann, K Chu, M Murphy, W J Schaff, L F Eastman, R Dimitrov, L Wittmer, M Stutzmann, W Rieger and J Hilsenbeck, *Appl. Phys. Lett.* **85**(**6**), 3222 (1999)
[11] M Li and Y Wang, *IEEE Trans. Electron. Devices* **55**(**1**), 261 (2008)
[12] X Cheng, M Li and Y Wang, *IEEE Trans. Electron. Devices* **56**(**12**), 2881 (2009)
[13] S Kola, J M Golio and G N Maracas, *IEEE Electron. Device Lett.* **9**(**3**), 136 (1988)
[14] User Guide Manual, ATLAS, Version 5.12.0.R. USA, Silvaco Inc., 2010
[15] M K Bera, Y Liu, L M Kyaw, Y J Ngoo, S P Singh and E F Chor, *ECS J. Solid State Sci. Technol.* **3**(**6**), 120 (2014)