PRAMANA
— journal of
physics

Vol. 76, No. 4
April 2011
pp. 657–666

Mismatch of dielectric constants at the interface of nanometer metal-oxide-semiconductor devices with high-*K* gate dielectric impacts on the inversion charge density

LING-FENG MAO
School of Urban Rail Transportation, 178 Gan-jiang East Road, Soochow University, Suzhou 215006, People's Republic of China
E-mail: mail_lingfeng@yahoo.com.cn

Abstract. The comparison of the inversion electron density between a nanometer metal-oxide-semiconductor (MOS) device with high-K gate dielectric and a SiO_2 MOS device with the same equivalent oxide thickness has been discussed. A fully self-consistent solution of the coupled Schrödinger–Poisson equations demonstrates that a larger dielectric-constant mismatch between the gate dielectric and silicon substrate can reduce electron density in the channel of a MOS device under inversion bias. Such a reduction in inversion electron density of the channel will increase with increase in gate voltage. A reduction in the charge density implies a reduction in the inversion electron density in the channel of a MOS device. It also implies that a larger dielectric constant of the gate dielectric might result in a reduction in the source–drain current and the gate leakage current.

Keywords. Dielectric film; metal-oxide-semiconductor field transistors; quantization.

PACS Nos 85.30.Tv; 85.35.-p

1. Introduction

In recent years, a major thrust of the development in the semiconductor industry is the search for new materials that could replace SiO_2 as the gate dielectric in complementary MOS technology. This is because SiO_2 film, which is the most commonly used gate dielectric, will most probably fail to meet the industry requirement as an insulating barrier due to the defect-assisted leakage current and the quantum-mechanical tunnelling current. Therefore, there is a need for high-permittivity (high-K) gate insulators with greater physical thickness (a factor of $K_{\text{high-K}}/K_{SiO_2}$) to prevent direct gate tunnelling. A suitable replacement gate dielectric with a high-K material must exhibit low leakage current, should have the ability to be integrated into an MOS process flow, and should exhibit at least the same equivalent capacitance, performance, and reliability as that of SiO_2. The high-K materials that can potentially replace SiO_2 are Ta_2O_5, TiO_2, Y_2O_3, CeO_2, $SrTiO_3$, Zr–Sn–Ti–O, Al_2O_3, La_2O_3, and silicates and oxides of hafnium and zirconium.

Researches related to high-K dielectrics are increasing rapidly because of their potential for substituting silicon dioxide in microelectronic devices [1–8]. Among the high-K alternatives, hafnium oxide is very promising. Hafnium oxide is a hard material with a relatively high dielectric constant and wide bandgap. Hafnium oxide-related researches are increasing rapidly because it can be used to substitute silicon dioxide in its role as the gate dielectric in microelectronic devices ([9–21] and references therein). According to ref. [1], the relative dielectric constant of HfO_2 ranges from 16 to 30, whereas the relative dielectric constant of ZrO_2 ranges from 12 to 16; the conduction band offset of HfO_2 is 1.5 eV and the band gap of HfO_2 ranges from 4.5 to 6.0 eV, whereas the conduction band offset of ZrO_2 ranges from 1.4 to 1.5 eV and the band gap of ZrO_2 ranges from 5.7 to 5.8 eV. Additionally, the relative dielectric constant of $ZrSiO_4$ ranges from 10 to 12, the conduction band offset is 1.5 eV, and the band gap of $ZrSiO_4$ is $\sim$6.0 eV. It can be noted that in [2], $0.20m_0$ has been used as the effective electron mass for both HfO_2 and ZrO_2. Thus it is possible to fabricate high-K gate oxide with different dielectric constants in an MOS device, and the effective electron mass and the barrier height are almost constant for such an MOS device with high-K gate oxide.

One of the most important developments in semiconductors, both from the viewpoint of physics and for the purpose of device developments, has been the structure in which the electronic behaviour is essentially two-dimensional (2D). Major systems where such 2D behaviour has been studied are MOS structures, quantum wells and superlattices. With the decreasing oxide thickness and the increasing substrate doping level, a very large electric field at the Si/SiO_2 interface is produced. Such a large electric field can give rise to a significant quantization in the inversion layer, which results in the redistribution of carriers. Many physical properties of carriers (both electrons and holes) depend strongly on such spatial confinements [22].

In our previous work [23], the effects of in-plane momentum of the electrons in the inversion layer of an MOS device on the quantization due to the effective electron mass mismatch between silicon and silicon dioxide was reported. Quantum mechanical modelling of an MOS device with high-K gate dielectrics has also been reported in [8]. To understand the scaling limits and to ensure that the selected high-K materials are highly scalable and usable for many future generations of technology, it is necessary to discuss how the mismatch of dielectric constant between silicon and gate dielectric impacts the quantization in the inversion layer of an MOS device. Moreover, it is well known that the quantization in the inversion layer will result in a change in the charge density and thus affect both source–drain current and the gate leakage current. Therefore, it is interesting to discuss the relation between the inversion electron density and the dielectric constant mismatch for a nanometer MOS device. In this work, the difference between the dielectric constant of silicon and gate dielectric impacts on the quantization in the inversion layer of an MOS device with p-type silicon substrate has been theoretically investigated through the self-consistent solution to the coupled Schrödinger–Poisson equations.

2. Methods

The effective mass theory is a powerful theoretical method for investigating the quantum feature of electrons in semiconductor heterostructures. Applying the parabolic band in the

effective mass theory, the one-dimensional Schrödinger equation for an MOS structure can be written as

$$\left(\frac{1}{2m_z(z)}\hat{p}_z^2 + \phi(z)\right)\psi = E\psi, \tag{1}$$

where z is the direction perpendicular to the Si/SiO_2 interface, $\phi(z)$ represents the potential energy along the z-direction, m_z and p_z, respectively denote the mass and momentum operators perpendicular to the Si/SiO_2 interface plane, and E is the electron energy.

An accurate description of electron in the inversion layer of an MOS device required a self-consistent solution of the Poisson and Schrödinger equations. In general, the 1D Poisson equation along the z-direction can be written as

$$\frac{\partial}{\partial z}\left[\varepsilon(z)\frac{\partial \varphi}{\partial z}\right] = -e\left[N_{\mathrm{D}}^{+}(z) - N_{\mathrm{A}}^{-}(z) + p(z) - n(z)\right], \tag{2}$$

where $\varphi(z)$ is the electrostatic potential, $\varepsilon(z)$ is the spatially-dependent dielectric constant, $N_{\mathrm{D}}^{+}(z)$ and $N_{\mathrm{A}}^{-}(z)$ are the ionized donor and acceptor concentrations, respectively, and $n(z)$ and $p(z)$ are the electron and hole densities, respectively. In this paper, the 1D Poisson (eq. (2)) and 1D Schrödinger equations (eq. (1)) are self-consistently solved using the finite-difference method [24,25] to study the effects of dielectric constant mismatch between silicon and gate dielectric on the quantization of nanometer MOS devices.

The iteration procedure to obtain self-consistent solutions for eqs (1) and (2) used in this paper can be described as follows. Starting with a trial potential, the wave functions and the corresponding eigenenergies can be calculated. The eigenenergies can be used to calculate the electron density distribution in the silicon substrate. The calculated inversion electron density distribution and a given acceptor–donor concentration can be used to calculate potential using eq. (2). Subsequent iteration can result in the final self-consistent solution. The maximum allowed correction to the band diagram for the converged structure in this work is 1×10^{-10} eV. The coupled Schrödinger–Poisson equations are self-consistently solved in the region from the metal/gate dielectric interface to the position in the silicon substrate that is 100 Å away. There are two boundaries in the solution to the one-dimensional Schrödinger equation: one is metal/gate dielectric interface, the other is in the silicon substrate that is 100 Å away from silicon/gate dielectric interfaces. Both wave functions of the carrier at two boundaries have been set as 0.

A field effect transistor is a capacitance-operated device, where the source–drain current of the field effect transistor depends on the gate capacitance. For the electrical design of an MOS device, it is convenient to define the 'electrical thickness' of the high-K gate dielectric in terms of its equivalent silicon dioxide thickness or 'equivalent oxide thickness' (EOT) as

$$t_{\mathrm{ox}} = \mathrm{EOT} = \left(\frac{\varepsilon_{\mathrm{SiO_2}}}{K}\right) t_{\mathrm{hik}} + t_{\mathrm{SiO_2}}, \tag{3}$$

where $\varepsilon_{\mathrm{SiO_2}}$ is the static dielectric constant of SiO_2 (usually it is 3.9), $t_{\mathrm{SiO_2}}$ is the thickness of the SiO_2 layer, K and t_{hik} are the relative permittivity and the thickness of high-K layer, respectively.

3. Results and discussion

In this work, for SiO_2, an effective electron mass of $0.5m_0$, a band gap of 9.0 eV, and a conduction band offset of 3.15 eV between silicon and SiO_2 were chosen according to ref. [1]. An average effective electron mass of $0.26m_0$ of Si was used in all calculations. Here we considered an MOS device (metal gate/high-K dielectric/p-substrate with $N_A = 1.0 \times 10^{17} cm^{-3}$) with the equivalent oxide thickness of 1 nm. For high-K dielectric, an effective electron mass of $0.2m_0$, a band gap of 5.8 eV and a conduction band offset of 1.5 eV were chosen in all the calculations. In this work, for simplicity, we did not consider image charge effects on the quantum confinement properties.

First of all, we shall discuss how the dielectric constant mismatch between silicon and gate dielectric affects the quantization in the inversion layer of an MOS device. Figure 1a shows the comparison of the quantized energy levels in the inversion layer between SiO_2 gate dielectric and high-K gate dielectric when 1 V is applied to the gate and the dielectric constant of gate dielectric is 3.9, 16, 23, and 30, respectively. It is clearly seen in figure 1a

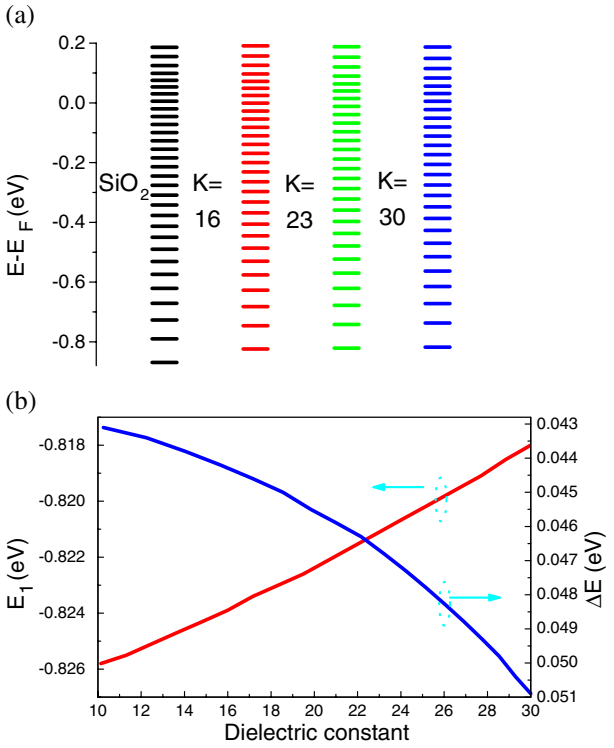

Figure 1. (**a**) The quantized energy levels (relative to the Fermi level in the p-type silicon substrate) in the inversion layer when the dielectric constant is 3.9, 16, 23, and 30, respectively. (**b**) The first quantized energy level in the inversion layer and its shift as a function of the dielectric constant of the gate dielectric. An equivalent oxide thickness of 1 nm and a gate voltage of 1 V were used in the calculations.

that the change in the dielectric constant of the gate dielectric will result in a positive shift in the quantized energy level. Figure 1b shows the first quantized energy level and its relative change compared to that in SiO_2 layer as a function of the dielectric constant of the gate dielectric. Here and in the following, E_1 and $E_1(0)$ respectively denote the first quantized energy level in the inversion layer of an MOS device with high-K gate dielectric and SiO_2 gate dielectric when the equivalent oxide thickness is 1 nm. Hence $\Delta E = E_1 - E_1(0)$. Figure 1b clearly illustrates that the first quantized energy level increases with the increase of the dielectric constant of the gate dielectric. All these imply that larger dielectric constant mismatch has a larger effect on the quantization level in the inversion layer of an MOS device. Basically, that the shift in the quantization level origins from that the dielectric function mismatch between silicon and gate dielectric can also affect the phase shift of the electron waves in the inversion layer of an MOS device through the change in the barrier height when a gate voltage is applied to the MOS device. Thus the phase shift of the electron waves will lead to a shift in the quantized energy level [26]. Note that the wave function $\psi(z)$ and the electron density $n(z)$ are related by [27]

$$n(z) = \frac{k_B T}{\pi \hbar^2} \sum_i g_i m_{di}^* \sum_j \ln\left(1 + \exp\left(\frac{E_F - E_{i,j}}{k_B T}\right)\right) \psi_{i,j}^2(z), \tag{4}$$

where m_{di}^* is the effective mass of the ith valley, k_B is the Boltzmann constant, $\hbar$ is the reduced Planck constant, T is the temperature, E_F is the Fermi level and $E_{i,j}$ is the quantization level. According to eq. (4), the shift in quantization level will lead to a change in the inversion electron density. As we know, the drive current for electron or source–drain current can be written as

$$J_n = q\mu_n\left(nF + \frac{k_B T}{q}\frac{\partial n}{\partial x}\right), \tag{5}$$

where q is the electron charge, μ_n is the electron mobility, F is the electric field, and x is the direction of electron flow. Equations (4) and (5) clearly illustrate that the shift in the quantization level should lead to a change in the drift current or source–drain current. Here also, the shift in the quantization level should lead to a change in the gate leakage current.

Figure 2a shows how the dielectric constant mismatch between silicon and gate dielectric affects the electron distribution in the inversion layer of an MOS device along the z-direction when 1 V is applied to the gate. Figure 2b shows the relative change of the concentration of electrons in the channel from 0 (the Si/gate dielectric interface) to 100 Å along the z-direction in the inversion layer compared to that for SiO_2 gate dielectric and peak values of the inversion electron density as a function of the dielectric constant of gate dielectric. Figure 2b clearly illustrates that the relative change in the peak value of electron density in the channel of an MOS device under inversion bias and the sheet concentration of electrons in the channel compared to that in SiO_2 gate dielectric decreases with the increasing dielectric constant of the gate dielectric. This is because higher dielectric constant of the gate dielectric can result in a phase shift of the electron waves in the inversion layer of an MOS device due to the difference between the dielectric constant of silicon and high-K gate dielectric. This implies that both the quantized energy level

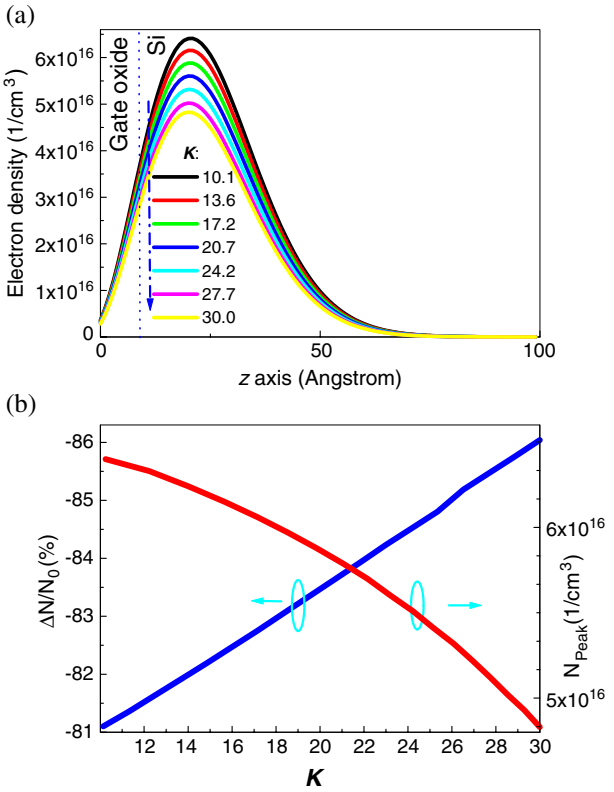

Figure 2. (**a**) The electron density in the channel that locates from 0 (the Si/gate dielectric interface) to 100 Å along the z-direction in the inversion layer with the equivalent oxide thickness of 1 nm and the gate voltage of 1 V. (**b**) The relative change in the peak value of electron density in the channel from 0 (the Si/gate dielectric interface) to 100 Å along the z-direction in the inversion layer compared to that for SiO_2 gate dielectric and peak values of inversion electron density as a function of the dielectric constant of gate dielectric.

and electron density profile will be affected by the dielectric constant mismatch between silicon and gate dielectric [26]. As we know, the main reason for replacing SiO_2 with high-K materials is to reduce leakage. The reducing charge density in the inversion layer of an MOS device represents the reducing gate leakage current. But it should be noted that the reducing charge density in the inversion layer of an MOS device also means reducing the drive current. It can be clearly concluded from figure 2b that a larger dielectric constant of gate dielectric might result in a reduction in the concentration of tunnelling electrons.

In the following section, we shall discuss how the impact of the dielectric constant mismatch between silicon and gate dielectric on the quantization in the inversion layer of an MOS device changes as a function of the gate voltage. Figure 3a shows the comparison of the quantized energy levels in the inversion layer between SiO_2 gate dielectric and high-K

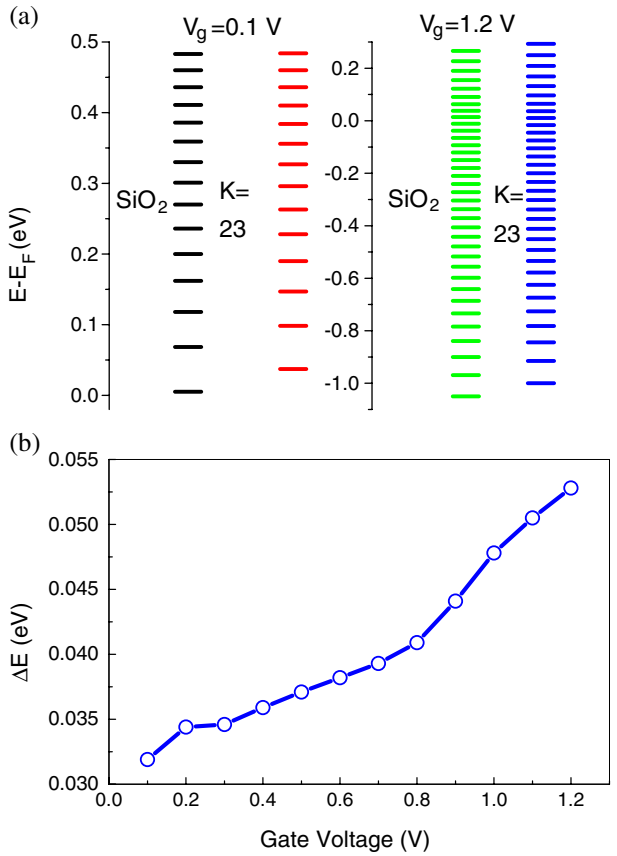

Figure 3. (**a**) The quantized energy levels (relative to the Fermi level in the *p*-type silicon substrate) in the inversion layer of SiO_2 gate dielectric MOS device and a high-*K* gate dielectric MOS device when the gate voltage is 0.1 and 1.2 V, respectively with the same equivalent dielectric thickness. (**b**) The shift in the first energy level in the inversion layer of a high-*K* MOS device compared to that for SiO_2 as a function of the gate voltage. An equivalent oxide thickness of 1 nm and a dielectric constant of 23 were used in the calculations.

gate dielectric. It can be clearly seen in figure 3a that the change in the dielectric constant of the gate dielectric will result in a positive shift in the quantized energy level for different gate voltages. Figure 3b illustrates how the shift in the first quantized energy level in the inversion layer of a high-*K* dielectric MOS device compared to that in SiO_2 gate dielectric changes with the gate voltage when the equivalent oxide thickness is 1 nm and the dielectric constant is 23. This figure clearly shows that first quantized energy level in the inversion layer of an MOS device will shift to higher energy levels when the gate voltage increases.

Figure 4 gives the relative change of the sheet concentration of channel electrons of an MOS device under inversion bias along the z-direction compared to that in SiO_2 gate

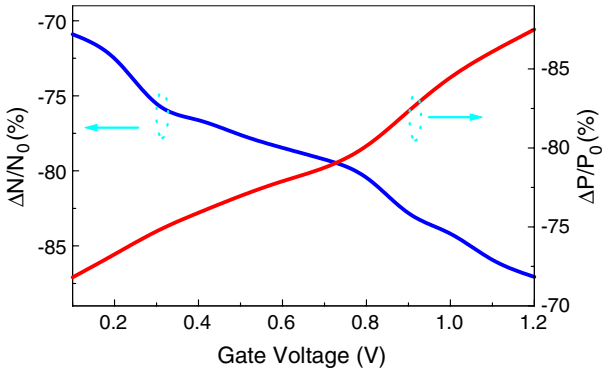

Figure 4. The relative change of the sheet concentration of electrons in the channel from 0 (the Si/gate dielectric interface) to 100 Å along the z-direction and the relative change of the peak value of electron density compared to that of SiO_2 gate dielectric as a function of gate voltage with an equivalent oxide thickness of 1 nm and a dielectric constant of 23.

dielectric change with the gate voltage. Equivalent oxide thickness of 1 nm and dielectric constant of 23 were used in the calculations. The figure clearly illustrates that the relative change of both the sheet concentration of electrons in the channel and the peak value of electron density linearly decrease with the increase of dielectric constant of gate dielectric. It is well known that a reduction in the inversion electron density in the channel might result in a reduction in the source–drain current and the gate leakage current. Thus it can be concluded from this figure that both the source–drain current and the gate leakage current compared to that of SiO_2 might be reduced when a larger voltage has been applied to the voltage.

Mismatch of dielectric constant at the interface of nanometer MOS devices with high-K gate dielectric impacts on the inversion charge density has been discussed. Note that the quantization in the inversion layer was determined by the electric field in the silicon substrate at the silicon/gate dielectric interface. The abrupt change in the dielectric constant can lead to an abrupt change in the electric field. But for continuous variable dielectric constant, a voltage drop will be applied to the transition region, which lead to an unchanged electric field in the silicon substrate at the silicon/gate dielectric interface. Therefore, there is no effect on the quantization of the inversion layer.

4. Conclusions

To conclude, the effects of the dielectric constant mismatch between silicon and gate dielectric on the quantization in the inversion layer was theoretically investigated through the self-consistent solution to the coupled Schrödinger–Poisson equations under the effective mass theory. Numerical calculations demonstrated that a larger dielectric constant mismatch between silicon and gate dielectric could lead to a reduction in the channel electron density of an MOS device under inversion bias. Larger dielectric constant mismatch was

found to largely affect the quantization in the inversion layer of the MOS devices. Understanding the impact of larger dielectric constant mismatch on the quantization throws light on future device processing, which needs a device to change the dielectric constant difference between the silicon and gate dielectric by properly selecting the gate dielectric or growth technology. Generally speaking, the electron density in the inversion layer of an MOS device decreases with the increase of dielectric constant mismatch. In other words, a larger dielectric constant mismatch between silicon and gate dielectric can result in a larger reduction in the inversion electron density in the channel. Thus, it can result in a reduction in the source–drain current and the gate leakage current.

Acknowledgement

The author acknowledges financial support from the National Natural Science Foundation of China (NSFC) Grant No. 61076102.

References

[1] C M Osburn, I Kim, S K Han, I De, K F Yee, S Gannavaram, S J Lee, C-H Lee, Z J Luo, W Zhu, J R Hauser, D-L Kwong, G Lucovsky, T P Ma and M C Öztürk, *IBM J. Res. Dev.* **46**, 299 (2002)
[2] B Govoreanu, P Blomme, K Henson, J Van Houdt and K De Meyer, *International Conference on Simulation of Semiconductor Processes and Devices* (Boston, USA, 2003) pp. 287–290
[3] Y-C Yeo, T-J King and C Hu, *IEEE Trans. Electron. Devices* **50**, 1027 (2003)
[4] R K Sharma, A Kumar and J M Anthony, *J. Metals* **53**, 53 (2001)
[5] S K Ray, R Mahapatra and S Maikap, *J. Mater. Sci.: Mater. Electron.* **17**, 689 (2006)
[6] J-P Locquet, C Marchiori, M Sousa, J Fompeyrine and J W Seo, *J. Appl. Phys.* **100**, 051610 (2006)
[7] V Fomenko, E P Gusev and E Borguet, *J. Appl. Phys.* **97**, 08371 (2005)
[8] H Wu, Y Zhao and M H White, *Solid-State Electron.* **50**, 1164 (2006)
[9] H Kim, P McIntyre and K C Saraswat, *Appl. Phys. Lett.* **82**, 106 (2003)
[10] M-H Cho, Y S Roh, C N Whang, K Jeong, S W Nahm, D-H Ko, J H Lee, N I Lee and K Fujihara, *Appl. Phys. Lett.* **81**, 472 (2003)
[11] R Puthenkovilakam and J P Chang, *J. Appl. Phys.* **96**, 2701 (2004)
[12] J C Garcia, A T Lino, L M R Scolfaro, J R Leite, V N Freire, G A Farias and E F da Silva Jr, *AIP Conf. Proc.* **772**, 189 (2005)
[13] X Zhao and D Vanderbilt, *Phys. Rev.* **B65**, 233106 (2002)
[14] O Maida, K Fukayama, M Takahashi, H Kobayashi, Y Kim, H Kim and D Choi, *Appl. Phys. Lett.* **89**, 122112 (2006)
[15] S Ferrari, S Spiga, C Wiemer, M Fanciulli and A Dimoulas, *Appl. Phys. Lett.* **89**, 122906 (2006)
[16] N Ikarashi, K Watanabe, K Masuzaki, T Nakagawa and M Miyamura, *J. Appl. Phys.* **100**, 063507 (2006)
[17] N Miyata, *Appl. Phys. Lett.* **89**, 102903 (2006)
[18] J J Gavartin, D Muñoz Ramo, A L Shluger, G Bersuker and B H Lee, *Appl. Phys. Lett.* **89**, 082908 (2006)
[19] M H Hakala, A S Foster, J L Gavartin, P Havu, M J Puska and R M Nieminen, *J. Appl. Phys.* **100**, 043708 (2006)

[20] H Takahashi, J Okabayashi, S Toyoda, H Kumigashira, M Oshima, K Ikeda, G L Liu, Z Liu and K Usuda, *Appl. Phys. Lett.* **89**, 012102 (2006)
[21] M-H Cho, K B Chung, C N Whang, D-H Ko, J H Lee and N I Lee, *Appl. Phys. Lett.* **88**, 202902 (2006)
[22] F Pregaldiny, C Lallement, R van Langevelde and D Mathiot, *Solid-State Electron.* **48**, 427 (2004)
[23] L F Mao, *Appl. Phys. Lett.* **91**, 123519 (2007)
[24] G L Snider, I-H Tan and E L Hu, *J. Appl. Phys.* **68**, 2849 (1990)
[25] I-H Tan, G L Snider and E L Hu, *J. Appl. Phys.* **68**, 4071 (1990)
[26] L F Mao and Z O Wang, *Superlattices and Microstructures* **43**, 168 (2008)
[27] S-H Lo, D A Buchanan and Y Taur, *IBM J. Res. Dev.* **43**, 327 (1999)