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Electrical characteristics of top contact pentacene organic thin film transistors with SiO_2 and poly(methyl methacrylate) as gate dielectrics

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Abstract. Organic thin film transistors (OTFTs) were fabricated using pentacene as the active layer with two different gate dielectrics, namely SiO_2 and poly(methyl methacrylate) (PMMA), in top contact geometry for comparative studies. OTFTs with SiO_2 as dielectric and gold deposited on the rough side of highly doped silicon (n^+-Si) as gate electrode exhibited reasonable field effect mobilities. To deal with poor stability and large leakage currents between source/drain and gate electrodes in these devices, isolated OTFTs with reduced source/drain contact area were fabricated by selective deposition of pentacene on SiO_2/PMMA through shadow mask. This led to almost negligible leakage currents and no degradation in electrical performance even after 14 days of storage under ambient conditions. But, the field effect mobilities obtained were lower than 10^{-3} cm^2 V^{-1} s^{-1}, whereas by using PMMA as gate dielectric with chromium deposited on the polished side of n^+-Si as gate electrode, improved field effect mobilities (>0.02 cm^2 V^{-1} s^{-1}) were obtained. PMMA-based OTFTs also exhibited lower leakage currents and reproducible output characteristics even after 30 days of storage under ambient conditions.

Keywords. Pentacene; organic thin-film transistors; poly(methyl methacrylate).

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1. Introduction

Organic thin film transistors have gained immense importance in recent years in the field of low cost, flat, and flexible large area coverage electronic applications such as flat panel displays, large area sensors and low cost RFID tags.

Several conjugated polymers and small molecules are widely studied for organic semiconducting active layer in OTFTs. Among organic semiconductors, pentacene has been the leading material for electronic applications with field effect mobilities

and threshold voltages comparable to those obtained with hydrogenated amorphous silicon [1,2]. This high performance of pentacene-based OTFTs is attributed to better intermolecular charge conduction due to high density and crystallinity of thermally deposited pentacene films and thus becomes one of the best candidates for future electronic applications.

To address the issue of large area coverage at low cost and low temperature, solution processable organic dielectrics are preferred over thermally grown SiO_2. In this direction, solution processed benzocyclobutene, polyvinyl alcohol, and other organic layers are studied as gate dielectrics in OTFT structures [3]. Field effect mobilities more than 1 $cm^2\ V^{-1}\ s^{-1}$ in pentacene-based OTFTs have been reported by the insertion of PVP buffer layer over inorganic dielectrics [4].

However, performance of OTFTs is affected significantly in air [5]. Recent studies on the environmental stability of OTFTs indicate that some specific gases such as H_2O and O_2 affect the TFT performance significantly [6–8]. For example, H_2O remarkably affects the performance of the OTFT with no encapsulation in ambient air. H_2O can diffuse into the grain boundaries and crystal lattice, and capture charges generated in the channel because of its polar nature [6,7,9]. This leads to the decrease in the on-current and field-effect mobility.

Oxygen diffused to the grain boundaries does not contribute to the accumulation of holes due to its electronegativity as suggested by Jurchescu *et al* [9], but changes pentacene into pentacene quinone by oxidation [10] leading to both chemical and electrical degradation of pentacene.

Apart from environmental stability, leakage current in organic semiconductor-based electronic devices is a key issue. The positive current at $V_{ds} = 0$ that increases with V_G is due to leakage between source/drain and gate electrodes through the gate insulating layer [11]. Incorporation of an additional low dielectric polymeric insulating layer in OTFTs is suggested by Yuan *et al* [11] to reduce leakage currents and parasitic capacitances derived from gate/source and gate/drain overlap.

In this work, we are comparing the electrical performance of top contact pentacene-based OTFTs fabricated using two different gate dielectrics, namely, SiO_2 (inorganic) and PMMA (polymeric). To deal with the leakage currents and bad electrical performance of pentacene TFTs having SiO_2 as dielectric layer and gold deposited on the rough side of n^+-Si as gate electrode (as shown in figure 1a), the fabrication of isolated devices with smaller contact areas (as shown in figure 1b) is suggested by us. The performance of these devices in terms of field effect mobility, leakage currents and environmental stability is compared with the OTFTs fabricated using spin-coated polymeric layer instead of the thermally grown SiO_2 as gate dielectric. The PMMA is opted for gate dielectric because of its easy processability, high resistivity ($>2 \times 10^{15}\ \Omega$ cm) and dielectric constant similar to that of SiO_2 ($\varepsilon = 2.6$ at 1 MHz, $\varepsilon = 3.9$ at 60 Hz). PMMA layer, inserted between the gate electrode and the active layer, has acted as both gate dielectric and an organic buffer layer to improve the film crystallinity of pentacene layer. In order to reduce the leakage current and improve the field effect mobility, we have fabricated these OTFTs with smaller source and drain contact areas and much lower W/L ratio [12].

It has been found that devices with PMMA as gate dielectric and chromium deposited on the polished side of highly doped Si as gate electrode for better ohmic

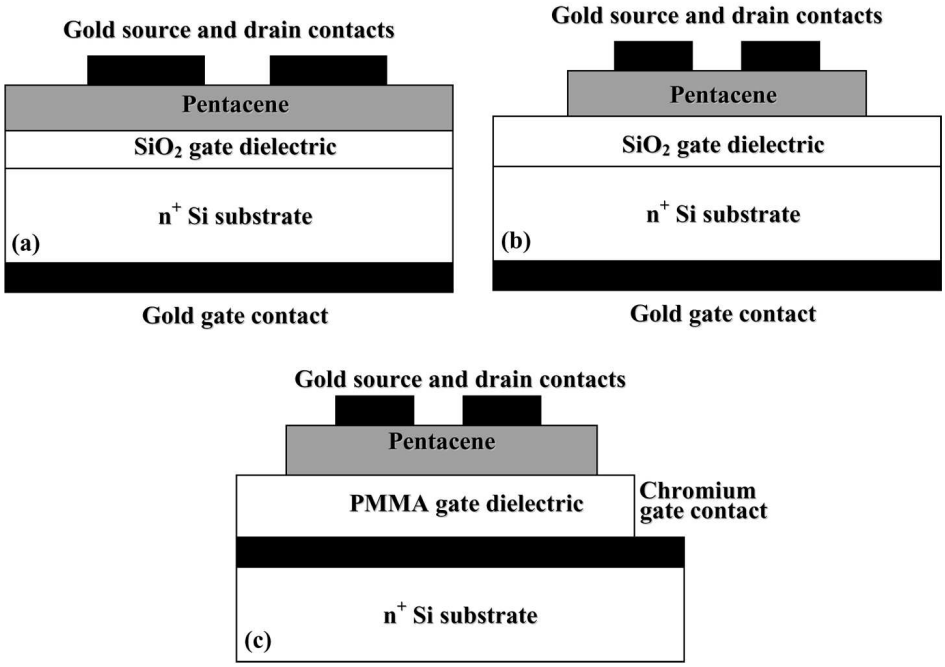

Figure 1. Schematic structures of OTFT: (**a**) non-isolated devices having SiO_2 dielectric and large contact area, (**b**) isolated devices having SiO_2 dielectric and small contact area, and (**c**) devices with PMMA gate dielectric and small contact area.

contact (shown in figure 1c), exhibit an improvement of one order in field effect mobilities along with better device performance and much lower leakage currents.

2. Experimental

Over highly doped n-type Si(1 0 0) wafer, a 100 nm thick SiO_2 layer was grown thermally. The wafer so prepared was subjected to standard RCA I & II cleaning procedures without any HF dip and then dried thoroughly under dry nitrogen. On the back, rough side of the Si–SiO_2 wafer, gate contact was fabricated by thermal evaporation of gold under vacuum ($<10^{-5}$ mbar). Then, pentacene (Aldrich, 97%), without further purification, was deposited over SiO_2 by thermal evaporation in a high vacuum system with a base pressure of the order of 10^{-6} mbar with deposition rate <1 Å/s. The thickness of the pentacene layer was about 200 nm as determined by surface profilometer. Finally, gold contacts were thermally evaporated through a shadow mask to form the drain and source electrodes. These devices had a channel length of 70 μm and a width of 5000 μm ($W/L = 71.43$). The contact area of single contact pad was $\sim$0.25 cm^2.

In order to reduce leakage currents, a second set of OTFTs was fabricated with smaller device and contact areas under similar conditions. To define and isolate

the devices, pentacene was evaporated through a metallic shadow mask in small pockets. Finally, gold contacts were thermally evaporated through an overlapping shadow mask to form the drain and source electrodes. These devices had a channel length of 70 μm and a width of 4000 μm ($W/L = 57.14$). The contact area of single contact pad was $\sim$0.05 cm^2.

For PMMA-based OTFTs, highly doped n-type Si wafer was cleaned by RCA I & II and finally subjected to HF dip in a diluted HF solution (H_2O : HF as 30 : 1) for 10 s. Subsequently, this wafer was cleaned with lots of DI water and dried properly under nitrogen. Immediately, it was loaded for chromium deposition on the polished side of Si wafer in vacuum coating unit. A 100 nm thick chromium layer was thermally evaporated to form the gate electrode. Then, as-purchased PMMA with a molecular weight of 950 K diluted in chlorobenzene (5%) was spin coated at 5000 rpm for 60 s. Baking at 165°C in a conventional oven was done for 30 min. The PMMA thickness was 300 nm as determined by reflectometer. Over this dielectric, pentacene was deposited as described above. And finally, source and drain contacts were fabricated by thermal evaporation of gold using a shadow mask. These devices had a channel length of 100 μm and a width of 2000 μm ($W/L = 20$). The contact area of single contact pad was $\sim$0.05 cm^2.

Neither surface modification nor encapsulation of OTFTs was attempted. Once the fabrication steps were over, the devices were characterized and kept at room temperature under ordinary environmental conditions (T = 298 K & RH = 55). No precautions were taken to prevent the degradation of pentacene films.

3. Results

Figures 2a and 2b show output and transfer characteristics of OTFT device fabricated over Si–SiO_2 wafer with large contact area and W/L ratio. From the curve of square root of drain current vs. gate voltage at constant -25 V drain–source voltage, carrier mobility is estimated to be 0.01 cm^2 V^{-1} s^{-1} at room temperature with a threshold voltage of about –10 V. The field-effect mobility is estimated in the saturation regime using eq. (1), where C_i is the capacitance of dielectric layer per unit area (F cm^{-2}):

$$I_{\mathrm{D}} = W/2L\mu_{\mathrm{EF}}C_i(V_{\mathrm{G}} - V_{\mathrm{T}})^2. \tag{1}$$

Figures 3a and 3b show output and transfer characteristics of an isolated OTFT device on Si–SiO_2 with smaller contact area. These devices were isolated from one another by depositing pentacene films selectively through a shadow mask. From the curve of square root of drain current vs. gate voltage at constant -25 V drain–source voltage, carrier mobility is estimated to be $<$0.001 cm^2 V^{-1} s^{-1}. Threshold voltage is about -5 V.

OTFTs fabricated by selective deposition of pentacene showed reproducible output characteristics even after 14 days of storage under ordinary environmental conditions, whereas the output characteristics of non-isolated devices got degraded with 45% reduction in output saturation current at $V_{\mathrm{G}} = -25$ V within 24 h in ambient conditions as shown in the inset of figure 2a.

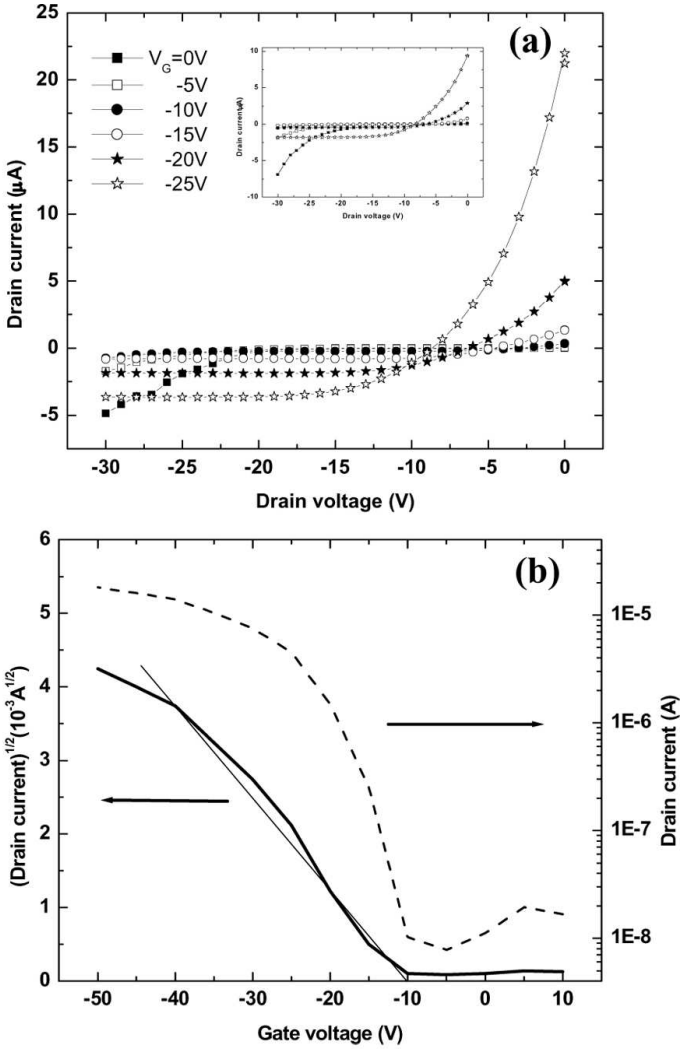

Figure 2. Output and transfer characteristics of non-isolated OTFT device fabricated over Si–SiO_2 with large contact area: (**a**) I_D vs. V_D for a series of gate voltages and (inset) output characteristics after 24 h and (**b**) I_D and $I_D^{1/2}$ vs. V_G for a fixed drain–source voltage of −25 V.

Figures 4a and 4b show output and transfer characteristics of an OTFT device with PMMA as gate dielectric. From the curve of the square root of the drain current vs. gate voltage at $V_G = -35$ V drain–source voltage, carrier mobility is estimated to be >0.02 cm^2 V^{-1} s^{-1}, which is more than the field effect mobility obtained in OTFTs fabricated using SiO_2 as gate dielectric. Threshold voltage is −20 V. Leakage currents between source/drain and gate electrodes through the gate-insulating layer are also reduced significantly (from 21 μA to 40 nA, at

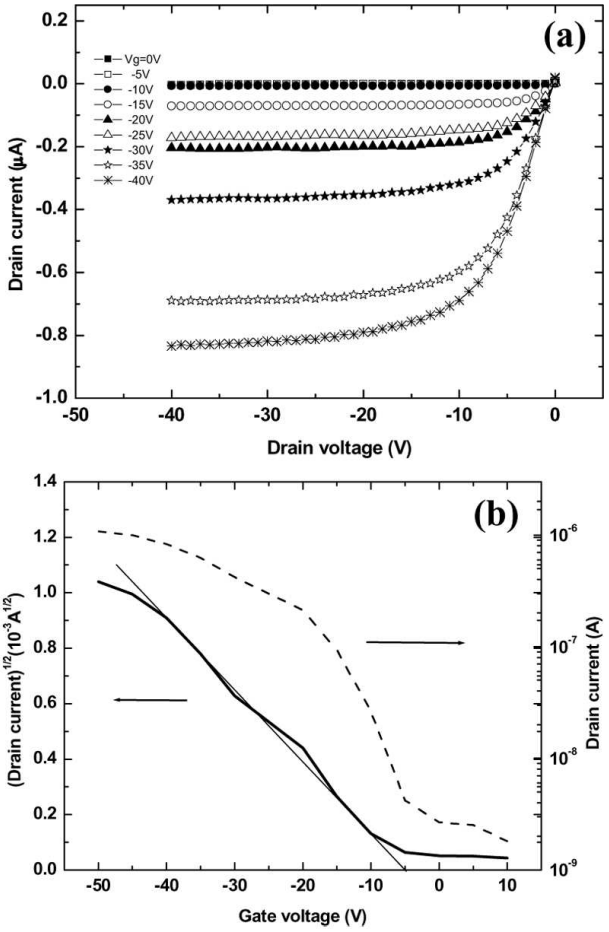

Figure 3. Output and transfer characteristics of isolated OTFT device fabricated over Si–SiO_2 with smaller contact area and W/L: (**a**) I_D vs. V_D for a series of gate voltages and (**b**) I_D and $I_D^{1/2}$ vs. V_G for a fixed drain–source voltage of −25 V.

$V_G = -25$ V). These results were reproducible even after 30 days of storage under ambient conditions.

4. Discussions

In the case of OTFTs having SiO_2 as gate dielectric, the positive current near $V_{DS} = 0$, appearing in output characteristics of non-isolated devices with larger contact area (0.25 cm^2, $W/L = 71.43$), is due to leakage of charge between source/drain and gate electrodes through the gate insulating layer. Due to this large leakage current, the value of the estimated field effect mobility is not reliable and may be

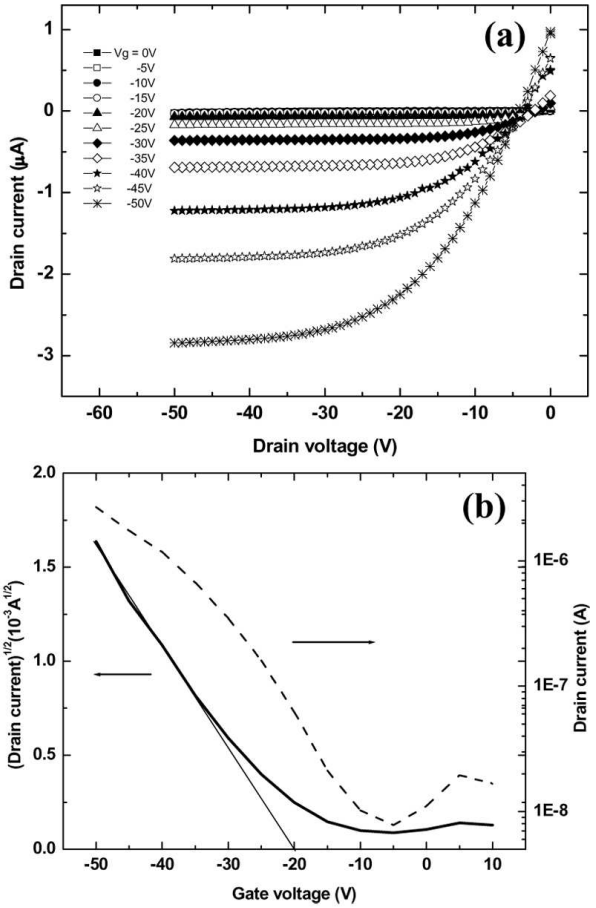

Figure 4. Output and transfer characteristics of device with PMMA gate dielectric: (**a**) I_{D} vs. V_{D} for a series of gate voltages and (**b**) I_{D} and $I_{\mathrm{D}}^{1/2}$ vs. V_{G} for a fixed drain–source voltage of −35 V.

overestimated. This leakage current increases with increasing V_{GS}. It is the direct outcome of overlap of source/drain electrode with the gate electrode.

In order to reduce this overlap, OTFTs are fabricated with shorter source/drain electrode area (0.05 cm^2, $W/L = 57.14$). Pinholes in the dielectric layer and cross-talk among devices fabricated over a common spread of pentacene layer also contribute to the leakage current. To omit the chances of leakage of current from pinholes and already short devices through pentacene, OTFTs are isolated by selective deposition of pentacene through shadow mask. This effort has resulted in better device performance. The threshold voltage got reduced to −5 V in isolated devices as compared to −10 V in non-isolated devices. A remarkable reduction in leakage currents (from 21 μA to 1 nA, at $V_{\mathrm{G}} = -25$ V) is also obtained. The estimated field effect mobility in these isolated devices is of the order of 10^{-3} cm^2 V^{-1} s^{-1}.

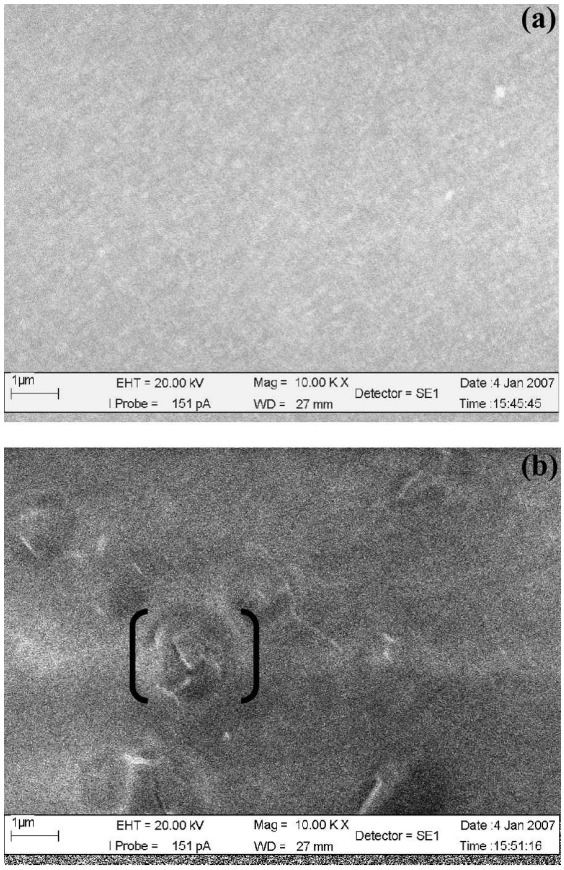

Figure 5. SEM pictures of 200 nm thick pentacene layer grown on: (**a**) SiO_2 and (**b**) PMMA (magnification = 10.00 KX and scale = 1 μm).

Moreover, the isolated devices with lower contact area exhibited reproducible output characteristics for a period of 14 days under ambient conditions. Longer stability of isolated devices is the direct outcome of lower effective area of pentacene exposed to light and air in the case of small pocket growth by selective deposition, as compared to the case of growth of pentacene all over the substrate. Hence, the propensity of light-catalysed aerial oxidation, leading to chemical and electronic degradation, gets appreciably reduced.

In order to study the variation of leakage current with source/drain electrode area, isolated devices were fabricated over SiO_2 dielectric layer with contact areas of 0.5 cm^2, 0.1 cm^2, 0.06 cm^2, and 0.05 cm^2. The leakage current in these devices progressively decreased as the contact area got reduced and found to be 0.12 μA, 83 nA, 40 nA, and 0.98 nA, respectively.

In the case of PMMA gate dielectric, along with higher field effect mobility >0.02 cm^2 V^{-1} s^{-1}, much lower leakage current (40 nA at $V_G = -25$ V) and reproducibility of output characteristics for longer period (30 days) have been obtained

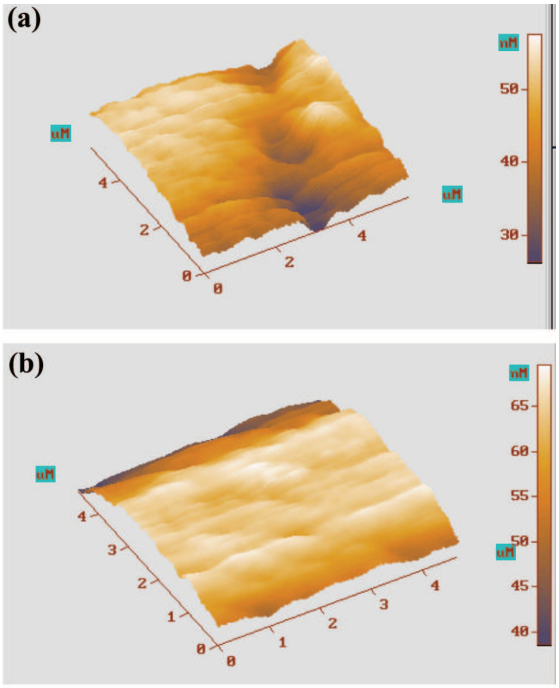

Figure 6. AFM images of pentacene layer (200 nm) grown on (**a**) SiO_2 and (**b**) PMMA.

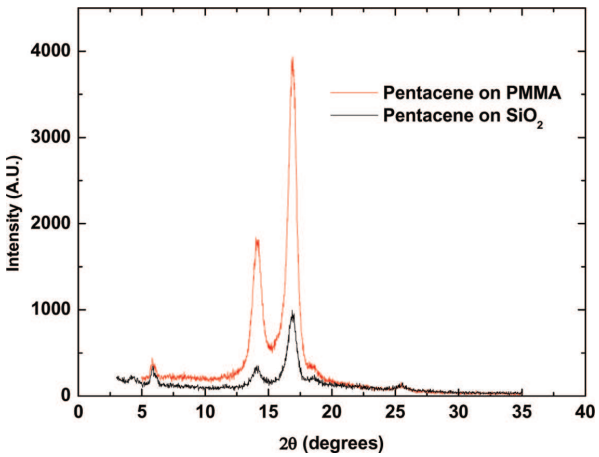

Figure 7. XRD plots of pentacene grown over SiO_2 and PMMA.

in OTFTs. Higher threshold voltage (−20 V) obtained in these devices is attributed to thicker PMMA gate dielectric (300 nm). Significant reduction in leakage current is the direct outcome of smaller source/drain contact area (0.05 cm^2, $W/L = 20$) as previously discussed.

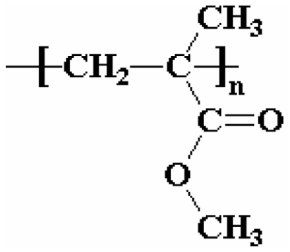

Figure 8. Poly(methyl methacrylate) (PMMA).

It is known that carrier mobility within a crystal grain is high. In polycrystalline structures grain boundaries scatter the carriers, resulting in lower mobilities. Since pentacene film grown on PMMA layer has bigger crystalline grains [13] than the one grown on SiO_2 as also shown in figures 5a and 5b, this consequently has led to improved field effect mobilities in PMMA-based devices. The formation of better pentacene films over PMMA is also evident in AFM images (figures 6a and 6b). The XRD plot of pentacene over PMMA exhibits more sharper and intense peaks as compared to the XRD plot of pentacene over SiO_2 (shown in figure 7).

The $-CH_3$ and $-OCH_3$ groups of PMMA polymer chains (figure 8) on the surface of the PMMA layer facilitate the oriented growth of pentacene through hydrophobic interactions and also lead to better adhesion of pentacene over PMMA. As a result of improved interfacial properties and crystalline nature of the pentacene film over PMMA, better device characteristics in terms of mobility, leakage current and stability and reproducibility of output characteristics for longer duration have been obtained. Moreover, lower contact resistance resulting from better adhesion of chromium on the polished side of Si wafer having lower surface roughness has led to better transistor action in these devices at gate voltage as high as -50 V.

OTFT having PMMA as gate dielectric layer showed reproducible output characteristics even after 30 days of storage under ordinary environmental conditions. This is again correlated to bigger grain size of pentacene film on PMMA that limits the diffusion of reactive gases, such as H_2O and O_2, making it less vulnerable to aerial oxidation thus imparting greater stability.

5. Conclusion

The result presented in this work shows that the reduction in the source/drain contact area and isolation of the devices not only result in better transistor action in terms of lower leakage current and reduced threshold voltage but also lead to better stability of the OTFT devices having SiO_2 as gate dielectric in terms of reproducible output characteristics. The issue of lower mobility in isolated devices has been taken care of by replacing SiO_2 with PMMA gate dielectric for better crystallinity of the pentacene films. PMMA is also a low cost and low temperature processed substitute for thermally grown SiO_2. Pentacene films over PMMA dielectric show better electrical performance, in terms of field effect mobility, along with longer stability.

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References

[1] D J Gundlach, Y Y Lin and T N Jackson, *IEEE Electron Dev. Lett.* **18**, 87 (1997)
[2] D Knipp, R A Street, A Völkel and J Ho, *J. Appl. Phys.* **93**, 347 (2003)
[3] D Knipp, R A Street, B Krusor, R Apte and J Ho, *J. Non-Cryst. Solids* **299–302**, 1042 (2002)
[4] C S Kim, S J Jo, S W Lee, W J Kim, H K Baik, S J Lee, D K Hwang and S Im, *Semicond. Sci. Technol.* **21**, 1022 (2006)
[5] S H Han, J H Kim, J Janga, S M Cho, M H Oh, S H Lee and D J Choo, *Appl. Phys. Lett.* **88**, 073519 (2006)
[6] D Li, E J Borkent, R Nortrup, H S Moon, H Katz and Z Bao, *Appl. Phys. Lett.* **86**, 042105 (2005)
[7] Y Qiu, Y Hu, G Dong, L Wang, J Xie and Y Ma, *Appl. Phys. Lett.* **83**, 1644 (2003)
[8] R Ye, M Baba, K Suzuki, Y Ohishi and K Mori, *Thin Solid Films* **464**, 437 (2004)
[9] O D Jurchescu, J Baas and T T M Palstra, *Appl. Phys. Lett.* **87**, 052102 (2005)
[10] O D Jurchescu, J Baas and T T M Palstra, *Appl. Phys. Lett.* **84**, 3061 (2004)
[11] J Yuan, J Zhang, J Wang, X Yan, D Yana and W Xu, *Appl. Phys. Lett.* **82**, 3967 (2003)
[12] C D Dimitrakopoulos and D J Mascaro, *IBM J. Res. Dev.* **45**, 11 (2001)
[13] J Puigdollers, C Voz, A Orpella, R Quidant, I Martin, M Vetter and R Alcubilla, *Organic Electronics* **5**, 67 (2004)