New developments of the R&D silicon tracking for linear collider on silicon trackers

A SAVOY-NAVARRO, on behalf of the SiLC R&D Collaboration
LPNHE Universités Paris 6 et 7, and CNRS-IN2P3, 4 Place Jussieu, 75252 Paris Cedex 05, France
E-mail: aurore@lpnhep.in2p3.fr

Abstract. The status of the R&D activity achieved so far within the SiLC (silicon tracking for the linear collider) collaboration is reported here. It includes the following items: present status of the collaboration, new developments on sensors, on mechanics (new directions for module construction, large support structure, cooling, and alignment and integration issues), new lab test bench results on electronics and sensors. The perspectives over a period of four years are presented with a detailed test beam schedule and the roadmap including the construction of new mechanical prototypes equipped with front end and readout chips in deep sub-micron CMOS technology are discussed. Combined tests with other sub-detectors are finally addressed. This test beam program is inserted in the framework of the EUDET European project.

Keywords. New generation of silicon tracking; new sensors; large area tracking systems for international linear collider; deep sub-micron electronics.

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1. Introduction

The SiLC R&D collaboration (The SiLC Collaboration includes: University of Michigan, Ann Arbor (USA), IMB-CNM/CSIC, Barcelona (Spain), HIP, University of Helsinki (Finland), IEKP, University of Karlsruhe (Germany), University of Liverpool (UK), Moscow State University (Russia), Obninsk State University (Russia), LPNHE-Université Pierre et Marie Curie/CNRS-IN2P3 (France), Charles University in Prague (Czech Republic), IFCA, University of Cantabria/CSIC (Spain), SCIPP and UCSC Santa Cruz (USA), IFIC-CSIC, Valencia (Spain), IHEP, Academy of Sciences, Vienna, (Austria), Kyungpook, University of Taegu, Yonsei University, Seoul, Korea University, Seoul, Seoul National University, SungKyunKwan University in Seoul (Korea), Tokyo University (Japan) and Hamamatsu Co. (Japan). There are also close collaboration contacts with CERN, FNAL and SLAC.) gathers a number of Asian, European and US institutes and research laboratories. It is a generic R&D collaboration aiming to develop the next generation of large area silicon trackers for the future linear collider (ILC) as well as for the upgrades of the LHC (SLHC) [1]. Indeed this R&D applies to three detector concepts.
for the ILC, i.e. LDC and GLD both include a TPC chamber as central tracker and SiD which has an all silicon tracking system. In fact, the main difference between these detector concepts is the tracking system. SiLC R&D offers a unique framework to compare their tracking performances. It is important to stress the synergy with the present LHC construction and its future upgrades and the fact that the development of collaborative contacts with industrial firms is underway.

2. R&D activities: Summary of present achievements

2.1 The sensors

This R&D is aiming for new breakthroughs in the silicon sensor technology. The silicon strips remain the baseline but the goal is to have larger wader (8" or more), thinner, both single and double sided (for some applications). Furthermore, for some region in the tracking system or some specific applications, the novel pixel technologies (new hybrid pixels, DEPFET, MAPS, SOI or 3D pixels) are under consideration.

2.1.1. Strategy for developing a new generation of silicon sensors. In order to achieve these goals, a new strategy is developed within SiLC. The first step consists of the development of close collaboration between institutes in SiLC and some industrial firms in order to study novel ideas on sensors. These firms will be able to provide the fabrication lines for producing a small number of new sensor prototypes. Once these new ideas are developed and tested, the technology can be further pursued by these firms or else transferred to larger firms for a large production line with insurance on high quality and reliability. The idea is to avoid the monopoly of a single firm and thus to create alternatives.

Most of the research laboratories interested in this R&D objective are equipped with the needed test bench framework, i.e. test bench with laser diode and radioactive sources to perform the characterization and accurate measurement of the signal/noise ratio delivered by each sensor prototype, but also some of these laboratories have developed, for the construction of the LHC silicon tracking systems, test set-ups that allow a very detailed characterization of the silicon sensors as produced by the industrial firm. This is the case of Karlsruhe and Vienna laboratories which have built test quality control of fabrication lines for CMS and developed a test procedure with detailed test structures added on the wafers that allow a full characterization and quality test of the production line. Because of this expertise, SiLC has established IEKP Karlsruhe as the head node that will coordinate and centralize the information and results coming from the different labs and firms which are developing new sensors. IEKP will collaborate with IHEP, Vienna to successfully lead this coordination task.

2.1.2. Signal over noise as a function of the strip lengths: New results. An interesting result has been achieved by the Paris and Prague teams in measuring the signal/noise (S/N) ratio vs. the length of the strips (figure 1), in a length ranging from 28 cm to 224 cm. The curve shows the results of this study pursued on the Paris test bench with a radioactive source. It shows that the S/N ratio varies from
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Figure 1. Signal/noise as a function of the strip length.

45 (mean calculated) or 30 (maximum probable value, MPV estimate) for about 30 cm length strips down to 8 (mean) or 5 (MPV) for 224 cm length. It stays above 15 (mean) or 10 (MPV) for a length up to 100 cm. The noise scales with strip length; the ENC is of the order of 20 electrons per cm. It must be noted that these results are obtained with a VA64-hdr readout circuit from IDEAS [2]. This device has a shaping time adequate for strip length up to 100 cm or so, but it is a bit too short for longer strips thus slightly deteriorating the signal from these longer strips [3].

2.1.3. Position using timing measurement. An interesting preliminary result was achieved by the Paris team on the attempt to measure the position using timing with silicon strips. The study was tackled in various ways. A simulation study was based on a detector linear model with SPICE that simulated the strip as a set of 1 cm long strip cells. The strip is characterized as a delay line element and thus the pulse velocity ($V$) is evaluated as in a simple LC line by $V = 1/\sqrt{LC}$. Using $L = 50 \text{nH}$, $C(\text{interstrip}) = 1 \text{pF/cm}$ and $C(\text{substrate}) = 100 \text{fF}$, and a resistive strip with $R = 5.6 \Omega/cm$, gives a line propagation at 8 cm/ns velocity (figure 2).

Another way to address the feasibility study was based on attempting to perform this measurement with a detector prototype at the Paris Lab test bench, moving the laser diode, set at its maximum available strength, along 28 cm length strips by steps of 2 cm. At each step, the strip response to the laser signal was recorded by a fast digital oscilloscope, after preamplification of gain 20 with a voltage preamplifier also used as impedance adapter. The measured velocity was indeed found to be 8 cm/ns, after applying a constant fraction threshold and filtering the pulse (figure 3).

Moreover, an estimate was made of the possible electronics timing resolution. A multiple sampling was simulated assuming a 180 nm CMOS technology front end chip; this allowed to take the noise value measured on the first prototype, i.e. 375 + 10.5 e/pF. A S/N ratio of 25 for 30 pF detector capacitance was assumed. The calculation was done with a n-points pulse sampling over two shaping time and least squares minimization time estimation [4]. Using $S/N = 25$, 8 samples and
50 ns shaping time for this measurement, 1.8 ns time resolution was obtained. This can still be improved by about a factor 2.

This work is still in progress but the first results are quite promising and the design of a front end electronics adapted to this measurement is underway. It is characterized by the use of SiGe technology (for optimizing the noise performances), a large gain preamplification stage and a fast shaping [5].

2.2 The mechanical issues

The mechanical aspects of this R&D are mainly dedicated in reducing, by all possible means, the overall material budget of such a tracking system. The activity is focusing on the following topics:

- Developing a new approach to build the elementary modules
- CAD design studies of the various components (light and large mechanical structure)
- Prototype design and construction
- Cooling thermomechanical studies
- Related positioning, alignment
- Integration issues with other sub-detectors.

2.2.1. New approach to build elementary modules. The elementary module is like the tile of the overall architecture of this tracking device. The main goals are to make it with novel sensors (see §2.1), they are made of one or a few such sensors assembled with very light and robust mechanical structure (investigating on new materials). The module includes the front end and readout chip(s) made in very deep sub-micron (VDSM) CMOS technology and wired directly onto the detector. This is to avoid extra room on the module for the electronics, pitch adapter and wiring and cabling and also to reduce the material budget. Largely multiplexed readout chips will sit on detector using in a first conservative approach flip chip bump bonding. Newer technology such as 3D integration technology is under consideration. Serial
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Figure 3. Attempt to measure the timing along silicon strips, by moving a laser diode by steps of 2 cm.

Figure 4. Two possible XUV designs of the end cap silicon tracking layers at large radius.

links will be used wherever possible to avoid multiple wire connection improving transparency and reliability, and the first description of the overall wiring and cabling for such detectors is elsewhere in these Proceedings [6].

This study addresses also the automation of the construction of such devices in large quantity and the possible industry transfer. The LHC silicon tracking system is based on sensors of various dimensions and shapes. This makes more difficult the construction of these devices. The goal is now to have tracking systems based on a single sensor type, i.e., unique in size and shape. This is reflected in the CAD designs of different components as briefly described in the next subsection.

2.2.2. CAD design of different silicon tracking components. Progress has been made towards designing large surface detector components both of the central barrel and the end caps using the same sensor unit. Figure 4 shows the design of the layers of an end cap silicon tracker using a XUV geometry instead of a projective design as done in the present silicon end cap trackers for LHC experiments.
Other components of special interest are the inner layers of both the barrel and the forward tracking. A number of questions must be addressed in this tricky region, one of them is about the best sensor technology(ies) to be used in these areas. In the current design, double-sided microstrips are the baseline for the central inner layers. But there is an increased interest in extending the pixel technologies to this region. One interesting possibility is the hybrid pixels as developed for BTeV experiment. Similar to the first forward disks near the vertex detector, pixels are to be used. But again what is the best technology? There is also an interesting development of the LHCb VELO device that could be considered for the forward disks [7].

2.2.3. **Thermomechanical studies.** Cooling is a crucial parameter in the increase of the material budget of any detector. Diminishing it by all means is one of the main goals of this R&D. The FE and readout electronics present in the detector is one the major cause of power dissipation. The designed electronics ensures that the complete electronics chain installed on the detector per channel will dissipate less than 1 mW/channel. The detailed CAD designs of the elementary modules and of the various components have allowed evaluating the thermal map of these devices already quite accurately. Realistic mechanical prototypes have been realized and detailed thermomechanical studies have been performed for each case. The main conclusion is that the power dissipated by the electronics on the detector can be easily handled by air cooling [8]. But the main concern is the heat possibly dissipated by the environment. This fact, in addition to the need for electromagnetic compatibility leads to the need of an insulating envelop to isolate the detector from any external disturbance such as noise or heat. Such envelopes are built for the actual LHC detectors using a light and very thin material based on rohacell foam.

2.2.4. **Alignment.** The silicon tracking devices are able to provide very high position resolutions, namely of a few microns even over large surfaces. This intrinsic property should not be deteriorated by the design of the detector itself. Aligning the silicon detectors and strips as accurately as possible is thus mandatory.

The IFCA team is proposing to address this issue by using collimated laser beams (IR spectrum), going through the silicon detector modules. The laser beams would be detected directly in the silicon modules. This is based on the previous experience of the AMS1 experiment [9] and extrapolating from their achieved results, a few microns (less than 2 microns) resolution could be achieved.

The main advantages of this approach are that particle tracks and laser beam share the same sensors, removing the need of any mechanical transfer and ensuring a minimum interference with silicon support structures.

2.3 **The R&D on the front end and the readout electronics**

This is another crucial topic of this R&D. Major advance was achieved in this front with the development of prototypes in deep sub-micron electronics. After the design and production of the first prototype achieved in 180 nm UMC technology, a lot of work was dedicated to the test of these first chips that proved to be quite successful. In parallel, the design of a second prototype with a full readout chain
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including, a sparsifier, an analogue pipeline and a Wilkinson A/D converter was undertaken in UMC 130 nm technology and sent to foundry by mid-April 2006. This is reported in more details in another contribution to these Proceedings [10].

3. Perspectives for the next four years: The EUDET program

Some of the collaborators of the SiLC collaboration are also part of the EUDET, FP6 E.U. Program on Infrastructures. This E.U. program aims to develop infrastructures for test beams for the major sub-detectors R&D projects for ILC. The deliverables for EUDET to be provided by the SiLC collaboration are:

- Front end readout chips to equip the silicon tracking prototypes that will be included in the beam tests. Two sets of foundries are foreseen in VDSM technology. One will be in 130 nm CMOS technology with readout chip including a A/D multiplexing on 128 channels. The other one will be in 90 nm CMOS technology and a multiplexing of at least 512 channels.
- Detector prototypes experiencing new large and light mechanical supports with new modules. These prototypes will be made of various new sensors that are starting to be developed.
- An alignment prototype, based on the design briefly described in 2.2.4.
- A cooling system prototype based on a design minimizing the material budget.

Several sequences of tests are scheduled. The first one will occur on fall 2006, on a 5 GeV electron beam in DESY, with newly designed elementary modules equipped first with the 180 nm prototype and possibly by the end of the year with the new 130 nm prototypes. These new FE readout chips will be first tested at the Paris test bench on a detector prototype and a radioactive source. Comparison with a VA1 FE chip from IDEAS will be performed. The performances in noise and S/N measurements will be the main parameters to evaluate these chips. The following years, larger detector prototypes with a few tens of thousands readout channels to be equipped with newly developed chips will be submitted to beam tests at high energy proton beams at CERN and/or FNAL. Also combined tests with other sub-detectors, namely, vertex devices, TPC and calorimeters and with magnetic field will be achieved.

This represents an ambitious program of work over the 4 next years. EUDET is a fantastic asset to achieve the R&D objectives of the SiLC collaboration and vice versa. All the SiLC partners including the non-E.U. ones will be contributing to EUDET and in return will have access to the EUDET facilities.

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