An electromagnetic calorimeter for the silicon detector concept

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Abstract. A silicon–tungsten calorimeter for silicon detector (SiD) at the International
Linear Collider is under development. Recent progress is summarized.

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1. Introduction

To complement LHC capabilities, ILC detectors must reconstruct hadronic final
states, including reasonable separability of $W \rightarrow$ jets from $Z \rightarrow$ jets. The LDC and
SiD full detector concept designs include silicon–tungsten (Si–W) electromagnetic
calorimeters (ECal) for particle flow reconstruction of jets at the ILC. With high
density and segmentation, they are critical to the physics goal jet energy resolution
of $\approx 30\%/\sqrt{E_{\mathrm{jet}}}$.

The few mm segmentation possible with a Si–W ECal provides outstanding re-
construction and isolation of individual photons. At the same time, good elec-
tromagnetic energy resolution is achievable — $\approx 15\%/\sqrt{E}$. Also, excellent lepton
reconstruction results from this 'imaging' calorimeter, crucial for many new physics
signatures. For more on the advantages of the Si–W approach, see refs [1–5].

An outstanding technical issue is integration of silicon detectors with readout
electronics. With about 50 million detector pixels, a solution to the integration issue
and the cost of the silicon detectors will likely determine viability. We proposed [6,7]
a possible integration solution which naturally allows high transverse segmentation
(currently 3.5 mm) and a small readout gap (currently 1 mm), maintaining a small

Moliere radius. In the SiD application, this design includes thirty longitudinal sampling layers – twenty of thickness $5/7X_0$, followed by ten of thickness $10/7X_0$.

The silicon detectors dominate the cost of our design, so we use simple sensor designs to control cost. The small Moliere radius allows better separability effectively at a reduced ECal radius, also reducing costs, since other elements of the overall detector are then smaller.

During the past year we have made important progress. The readout chip (KPiX) design was completed and sent to industry, for three prototype cycles. The prototype functions, albeit with some issues. We have made progress characterizing prototype silicon detectors and developing a novel readout cable concept for the thin gap. The critical bump bonding is being planned for prototypes. This progress gives us confidence in the design and we plan to demonstrate the detector concept with prototypes in an electron test beam, and develop a full-depth ECal module, incorporating features needed for a realistic ILC detector. This module could be part of an international test beam study. While we focus on an implementation of our approach for the SiD design, the ideas and R&D are applicable to other Si–W ECal designs, notably LDC.

2. Overview of gap design

The thrust of our project is to integrate pixels on a large, commercially feasible silicon wafer, with the readout electronics, including digitization, contained in a single chip, bump bonded to the wafer. Pixel size of 12 mm^2 (motivated by PFA requirements for photon isolation) gives $N \approx 10^3$ pixels per 6-inch wafer. The beam-crossing duty cycle ($\sim 10^{-3}$) permits heat reduction with power cycling. Our design has several important features: (i) electronics channel count effectively reduced by a factor $N = 1024$, (ii) transverse segmentation down to a few mm naturally accommodated, (iii) cost, to first order, independent of the transverse segmentation, and (iv) small readout gaps ($\sim$1 mm, figure 1), maintaining a small Moliere radius. The first property is necessary for a realistic highly-segmented ECal. The electronics is then a relatively small fraction of the ECal cost. The third creates flexibility to optimize for physics goals. The fourth optimizes the physics capability and reduces cost.

3. KPiX readout chip

The most significant development for our project has been completion of the design of the KPiX readout chip and the fabrication of the first rounds of prototype chips. A recent discussion of the KPiX functionality can be found in ref. [8].

4. Silicon sensor properties

In the past year we continued measurements on 6-inch Hamamatsu prototypes with an emphasis on parameters relevant to use of the sensors with electronics design.
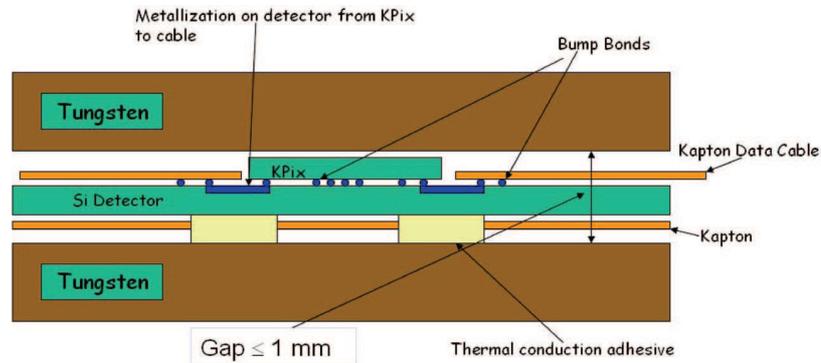
Figure 1. Schematic of the readout gap. With power cycling of the readout chip, the heat load of the KPiX readout chip can be handled by passive conduction through the tungsten.

The most important measurements in this regard are stray capacitance and leakage current. We have also investigated the use of a radioactive source for an absolute calibration. The results here are an update of our presentation [9] at LCWS05.

4.1 *Pixel capacitance and trace resistance*

In most cases the noise of a pixel charge measurement is directly proportional to the total capacitance input to the amplifier, dominated by the stray capacitance of traces connecting pixels to the bump-bonding array. Our Hamamatsu detectors have oxide metal layers about $0.9\,\mu$m thick, and $6\,\mu$m thick traces, giving a theoretical capacitance of approximately $3.1\,$pF/cm. The total stray capacitance of a given pixel has two contributions, one from the capacitance of the traces connecting the pixel to the bump-bonding array, and a second due to traces from other pixels which cross the given pixel. These are compensating effects, leading to very similar values for the stray capacitances.

A small fraction of the pixels have a very large number of crossing traces, resulting in capacitances of little more than 100 pF. In a future version of the sensors we plan to reduce the larger stray capacitances by narrowing the traces in the vicinity of the bump-bonding array. In figure 2, the measured capacitances are shown for a large number of pixels in one quadrant for the Hamamatsu detector, as well as the expected capacitance for a future version of the detector with 1024 pixels and slightly smaller pixels.

Another important property of the detectors is trace series resistance (R_s), with a noise contribution proportional to $C_\mathrm{tot}\sqrt{R_\mathrm{s}}$, where C_tot is the total input capacitance. It is desirable to keep this noise term comparable to the input FET noise, or $R_\mathrm{s} \sim 300\Omega$. We measure a trace resistance of $57 \pm 2\Omega$/cm. For the longest traces ($\sim 10\,$cm) the measured value implies a maximum resistance of $\sim 600\Omega$.
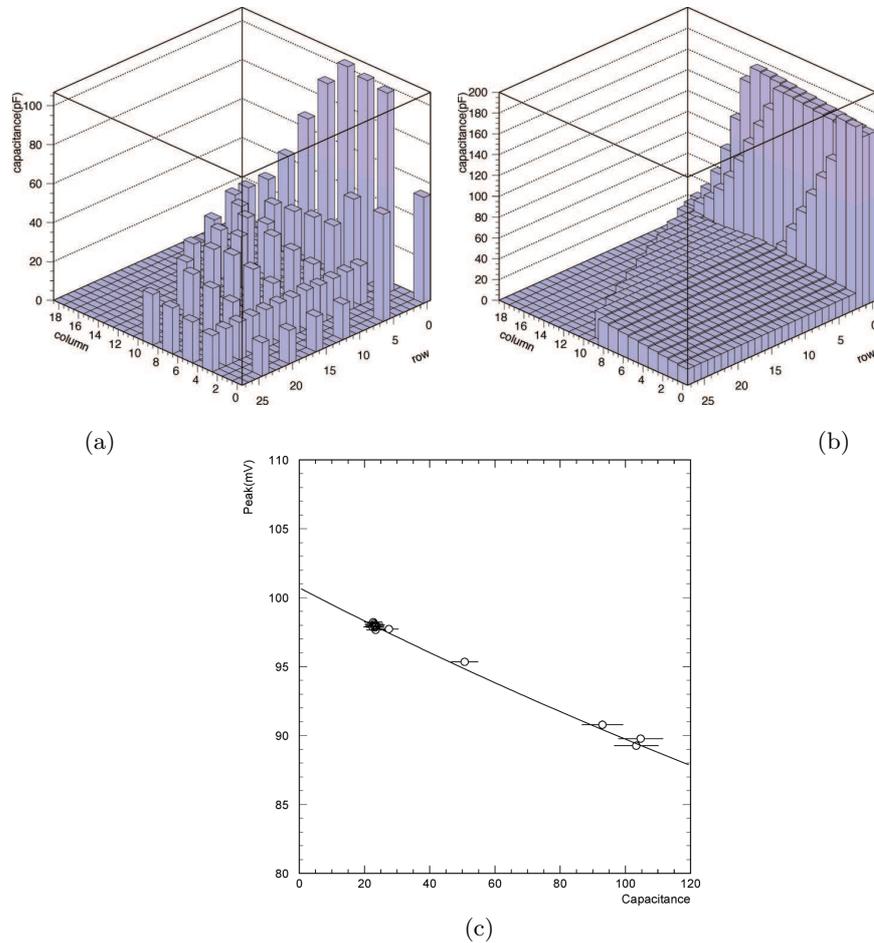
(a)

(b)

(c)

Figure 2. Summary of capacitance measurements as a function of pixel position on the detector. Figure 2a shows current measurements, where the high capacitance of pixels at small row number is due to large number of traces in that region. Figure 2b shows the expected capacitance in a 1024 pixel version of the sensor. Figure 2c shows the measured position of ^{241}Am peak signal versus total pixel capacitance.

4.2 *Leakage current*

Leakage current (typically a few nA/cm^2) can add an additional term to the electronic noise that grows with shaping time. Leakage current was measured to be $<2\,nA/pixel$ for the interior of the detector. The neighboring pixels and the guard ring were left 'floating'. For pixels on the edge of the detector, with the guard ring floating, the leakage current was less than $10\,nA/pixel$. We expect the noise contribution for leakage current to be minimal, ~250 electrons.

4.3 *Calibration*

Silicon calorimeters are quite stable. Since the largest change in response is due to the electronics, it is designed with an internal calibration system. This internal calibration should limit the spread within a chip to $\sim 1\%$. Chip-to-chip variations could be larger. Each sensor might be calibrated after the readout chip has been bump bonded with 60 keV photons from ^{241}Am. Fully contained deposition gives a signal of approximately 16,000 electrons, somewhat less than the MIP signal, but well above our noise. The calibration must be done before the detector assemblies are placed between the tungsten sheets.

To demonstrate this technique we show the measurements of the ^{241}Am photon peak versus pixel capacitance in the right plot of figure 2. The peak shifts lower at larger capacitance because of the finite input capacitance of laboratory electronics. The signal-to-noise for the ^{241}Am peak will be about 8 in the final system, which will broaden the peak considerably. The charge measurement will be relative to an external bunch clock rather than to the time of arrival of the photon in the laboratory. This adds an additional smearing of the observed spectrum of less than 5%. Thus we expect a total width for the ^{241}Am 60 keV signal of approximately 15%.

Since the readout ADC will have a least significant bit approximately equal to the expected noise it should be possible to calibrate each pixel to 1% with approximately 250 detected photons. Relating the charge scale at 8 ADC counts to that at full scale readout, will require care in the design. Somewhat easier, but still difficult, will be a wafer-to-wafer calibration at the sub-per cent level, averaging over 1024 pixels/wafer.

4.4 *Cross talk*

The cross talk introduced capacitive couplings between the channels has been found to be at or below the 1% level. The cross talk is a function of both the capacitive coupling and the properties of the readout electronics. While we have a qualitative understanding of the cross talk, we are continuing to work on a quantitative model and on incorporating the properties of the KPiX electronics into the model.

Acknowledgments

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