PRAMANA
— journal of
physics

Vol. 69, No. 6
December 2007
pp. 977–980

Preliminary thoughts on the data acquisition for the next generation of silicon tracking systems

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Abstract. Preliminary thoughts about the data acquisition system to be developed for the next generation of large area silicon tracker are presented in this paper. This paper describes the set of data delivered by these tracking systems, and the various stages of processing and data flow transmission from the front-end chip sitting on the detector to the latest stage in the data processing. How to best profit from the status of the art technologies is a major goal.

Keywords. New generation of silicon tracking; large area tracking systems for international linear collider; deep sub-micron electronics; new packaging technologies; data acquisition.

PACS No. 29.40.Gx

1. Introduction

The SiLC R&D collaboration is a generic R&D aiming to develop the next generation of large area silicon trackers for the future linear collider (ILC) as well as for the upgrades of the LHC (SLHC) [1]. One major issue is the readout and data acquisition system (DAQ) attached to these detectors. From the front-end chip to the fully processed detector information, there is a long path with different crucial steps. High technology breakthroughs are of high importance to design these sophisticated systems at each of these steps. The information delivered by the detectors are first discussed. The various stages in the processing of this information and the data flow transmission are then presented with an emphasis on the technological challenges and preliminary ideas of how to tackle them best.

2. The information extracted from the detector

The front-end and readout system associated to this detector is described elsewhere in these Proceedings [2]. This readout chain delivers two types of information, namely:

- The pulse height signal from the detector is processed by the front-end and readout electronics in order to provide the position along the track with a very high precision. The sparsification will be included in the readout chain on the detector. The analog signal from the detector will be converted into a digital information by a 10-bit A/D converter. In order to achieve a precision of a few μms in the 2D space, a real time computation of the cluster centroid will be included.
- The timing information is provided in two ways. One is a coarse 150–300 ns bunch crossing (BCO) timing information in order to provide the BCO tagging. The other timing information consists of a fine nanosecond timing for evaluating the position coordinate along the strip. To do so, a fine BCO tagging is required [1,2]. This will be included in one or a few layers, only in certain region of the detector if proven to be useful.

3. Challenges of the on-detector data processing

The data processing is achieved by the front-end and readout chip that sits onto the detector and possibly additional processing profiting from the digitization applied on-detector plus the relatively long time in between bunch trains (of the order of 100–200 ms in the ILC case). The on-detector front-end chip processes the data in the following way [2]: 5–10 samples of the pulse are stored over two different shaping times (if the timing is included, or only one for the pulse height). It is followed by a multi-event buffering in a 8-deep 2D analog buffer, i.e. 8 times 5 to 10 sample cells per channel. After the end of the train, an analog-to-digital conversion is performed in parallel for all channels by a Wilkinson A/D converter. This type of conversion is optimum with respect to silicon area, power, and speed. Sparsification using threshold detection on analog sums will be included, as well as a complete on-chip calibration scheme. The digital processing on detector will comprise the amplitude and time estimation and the charge cluster characterization algorithms.

The time stamping resolution is expected to be of the order of 30–50 ns, tagging the sparsifier output at four times the BCO clock, i.e. 12 MHz. The fine time measurement resolution is expected to be of the order of 1–3 ns, with 32 times BCO on-chip interpolated clock sampling (PLL at 96 MHz). It will use digital processing over 5–10 digitized samples.

The total data per hit channel is given by: Address (32 bits) + time (BCO, 16 bits) + data (10) bits. The main challenges of the overall DAQ system sitting on the detector are to have a highly performing readout and real time processing system with the lowest possible material budget. They have to be taken into account in the design of the overall DAQ architecture scheme, the electronics components, the packaging and the cabling as well as the calibration and the cooling systems.

4. Transmission of the data flow

We briefly give some indication about the cabling scheme to transmit the data flow from the detector to the outside world. This topic will be particularly dependent on the technology developments which, in this field, are expected to be very important. Presently it is foreseen to use micro-coaxial cables of typically one millimeter diameter, 0.4 g/m weight. Kapton cables are also under consideration. At a later stage in the cabling scheme, i.e. to transmit the information from the edge of the detector to the outside, 6 GHz SCM fiber optic links are presently considered, but the micro-coaxial could also be used. Of course all this is under serious investigations taking into account what the prospects are in the related industrial domain. Three main issues are:

- Cables versus/and/or fibers. Micro-coaxial cables are making a comeback and seem to gain some favour with respect to fibers. This issue has to be followed closely with the corresponding developments in the industry. Micro-coaxials have typical bandwidths from 50 to 150 GHz against 6 GHz of the present fiber technology. Moreover, the propagation velocity is of the order of $c/2$ using fibers against $c/1.2$ in cables, and there is no power wasted to produce IR light in the driver.
- High multiplexing rate versus redundancy. The present goal is to apply large multiplexing factors to reduce the number of channels and the overall cabling as much as possible, thereby decreasing the material budget. A large multiplexing factor of at least 512/1 or even 1024/1 is under study at the A/D converter level. Then other multiplexing factors will be applied on the cabling path. Of course this has to be balanced with respect to redundancy (safety issue) in order to avoid loosing a large fraction of the detector information if any problem occurs in the readout and data processing/transmission chain. It should be mentioned that this increase in multiplexing factors should result in a decrease in the overall cost.
- Power switching. The total power to be sent is of the order of 1.5 kW during data taking, 10 W in average with power cycling. Switchings will imply current spikes of the order of 500 A, if all channels are set at the same time.

  A round robin scheme ramping one of the sixteen detector sections every millisecond, for instance, would average the currents and avoid huge local power spikes.

5. Application to a component of the silicon tracking system

The present DAQ scheme of the external silicon component in the LDC concept is briefly summarized here, as an example of what is currently under study. A silicon external tracking component (SET) sitting between the TPC and the electromagnetic calorimeter in the central barrel, has been proposed in the LDC concept [3]. In the current design it is made of 60 cm long strips and it follows the octogonal design of the electromagnetic calorimeter. The overall device is divided into two parts that are assembled jointly at 90° with respect to the beam axis. Each half

is made of eight rectangular planes of 2.4 m length by 1.2 m width. Each of these rectangular planes is made of modules composed of three single sided sensors of 20 by 20 cm^2 bonded to each other to form the 60 cm long strips. The SET component is a false double sided layer, false meaning that this layer is indeed made of two single sided layers. This device will cover a total area of the order of 80 m^2 and corresponds in the present design to roughly 1.6 million of channels to be read out.

The daisy chaining the front-end chips of four adjacent modules on the same half plane with micro-coaxial cabling, results in a total of six micro-coaxial cables for each half plane. The resulting signal would then be transmitted from the edge of each half plane to the outside world by fibers. A total of eight fibers for each side would thus transmit the overall detector information. For safety, each fiber would be doubled by another fiber in case there is a problem. Thus 16 fibers on each side would be needed to transmit the overall processed information.

Taking a 1% occupancy for this external silicon component, 3000 bunch trains per crossing and of the order of 100.000 channels sent by fiber, this gives 3.2 Mwords per bunch and per fiber and between 19 and 32 Mbytes depending upon the on-detector processing, as a total. It corresponds to 3.2 or 5.3 ms total transfer duration for 6 Gb/s fibers. This gives the current status of thinking on the total amount of information to be transmitted by these very large area tracking components, a tentative way to reduce the needed number of on-detector chips, on-detector cabling and transmission to the outside world.

People have been so far mostly focused on developing the front-end readout chips but they are starting now to develop the design and the needed R&D on the following components of the DAQ. This includes the packaging, the cabling and the repartition of the processing on or out of the detector. A very active R&D and development of close collaborations with industry are starting on these crucial issues.

References

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[2] J F Genat *et al*, *Status on the development of front-end and readout electronics for large silicon trackers*, These proceedings, and references therein

[3] The chapter on *Supplementary tracking* in the DOD document for the LDC detector concept, and references therein