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A PSD-based electronic system for AC response studies of superionic conductors

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Abstract. An electronic system based on quadrature oscillator, current-to-voltage converter and phase sensitive detector (PSD) has been designed and constructed for measurement of AC electrical conductivity and complex impedance/admittance on ionic and superionic conductors at several frequencies upto 60 kHz. The design incorporates a CMOS FET switch controlled by two anti-square reference signals for rectification and a differential amplifier for summation and impedance matching. The performance of the system has been demonstrated and the measurement possibilities discussed.

Keywords. Current-to-voltage converter; phase sensitive detector; AC response; impedance/admittance; superionic conductors.

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1. Introduction

The electrolytic conduction in ionic/superionic solids is mainly due to the movement of charged ions under the influence of an applied electric field. When a constant DC potential is applied to an electrolyte kept between two different electrodes as shown below

–	nonblocking electrode	A^+B^-	blocking electrode	+

the cation starts moving towards the negative electrode. As a result, the right end of the electrolyte suffers a depletion of cations as no more ions are supplied at the positive electrode. As soon as the circuit is switched on the instantaneous current and voltages give a measure of total conductivity (ionic plus electronic). The current decays slowly with the lapse of time yielding a stabilized final value. This is a measure of the electronic conductivity.

These polarization effects (Wagner 1976) are troublesome in a DC measurement unless nonpolarizing electrodes capable of supplying mobile ions at the anode-electrolyte interface are used. Then the electrode configuration becomes

–	nonblocking electrode	A^+B^-	nonblocking electrode	+

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where the electrode materials are the same as that of mobile species. This avoids the problem of polarization, but the utility of such electrodes is limited by the following facts (Chandra 1981).

(a) the extent of electronic conductivity cannot be evaluated for the transport number measurement (b) the type of mobile ions have to be known before hand. Further, if more than one type of charge carrier is present, it is difficult to find a material which can act as a reversible electrode for various types of mobile ions. (c) it is not always easy to handle the mobile species electrodes. For example in fluorine ion conductors like PbF_2, having a fluorine electrode is tricky.

The problems associated with the choice and use of an appropriate non-blocking electrode can be overcome by employing blocking electrodes and measuring as a function of frequency.

Apart from the undesirable polarization effects, when the DC measurements are performed on ionic conductors, over a wide range of temperatures, another unavoidable difficulty arises owing to the presence of interfering voltages due to the Thomson and Seebeck effects. These interfering voltages make the measurement more difficult because of its random variations with changes of room temperature. To avoid these heating effects and the difficulty due to polarization, an AC method employing synchronous rectification is devised for the measurement of electrical conductivity.

The AC measurements are also significant because in addition to bulk conductivity, many other electrochemical parameters are also sampled as a function of applied frequency. The resultant alternating current is out of phase with the applied AC voltage and perturbs the various processes within the measuring cell (such as surface, interfacial, grain boundary ionic transport and double-layer formation at electrode/electrolyte interface) in different ways.

In superionic conductors, particularly in sintered polycrystalline and ill-quenched glassy forms the grain boundary contribution becomes significant. The extraction of true intrinsic conductivity therefore must involve measurement such as an impedance/admittance technique which would enable clear separation of the observed response into intrinsic and grain boundary contribution. In such cases a simple DC measurement would be vitiated by the presence of significant polarization and grain boundary effect, thus making an AC measurement mandatory.

Our design of this electronic instrument is a considerably modified version of Nelson who used a full-wave rectifier (Nelson 1980) for detection instead of phase sensitive detection (PSD) employed in the present case. One of the main advantages of PSD over precision rectifier is the total rejection of discrete frequency noise such as AC mains pick up and unwanted signals due to DC offset, $1/f$ noise and various thermal effects.

2. Description of the circuit

The instrumental set up is shown in figure 1.

2.1 *Quadrature oscillator and buffer*

Figure 2 shows the quadrature oscillator (Jones 1985). This is a low-distortion ($\leqslant 0{\cdot}1$) two-phase sine-wave oscillator, which provides three stable outputs at 0° (sine), 90°

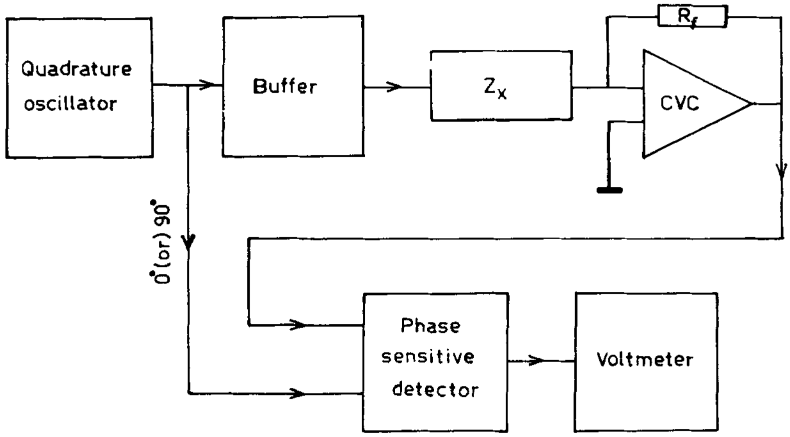

Figure 1. Block diagram of the electronic system showing various modules (CVC = current-to-voltage converter).

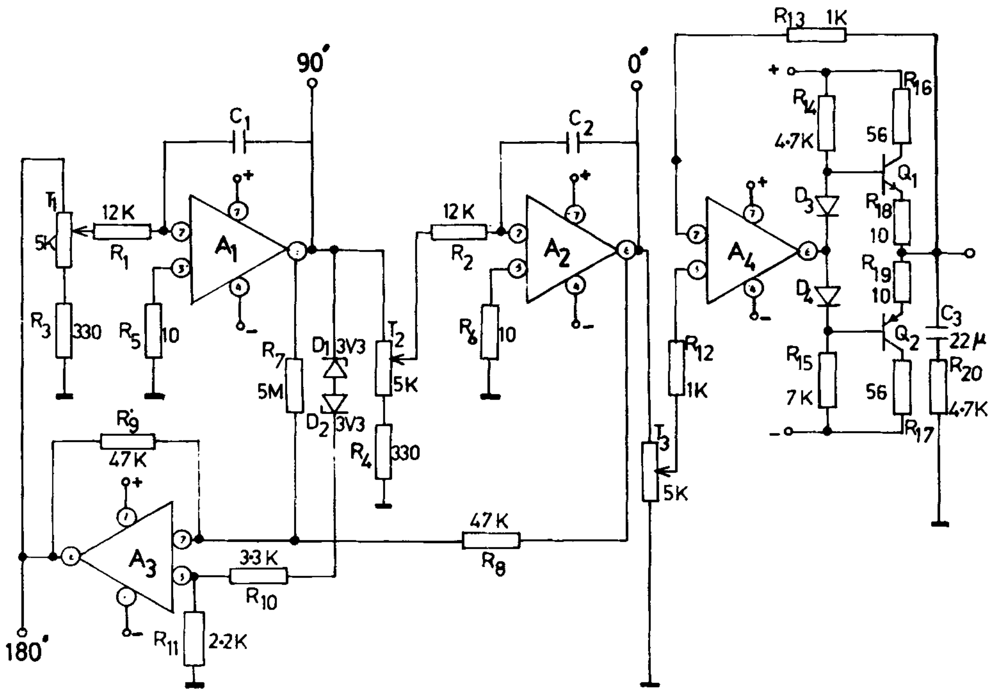

Figure 2. Quadrature oscillator and buffer, amplifier (A_1 to A_4) are 741 type. Transistors Q_1 = SL 100 and Q_2 = SK 100.

(cosine) and 180° (−sine) phases. Basically it is two integrators connected with feedback via a unity gain inverter. Oscillations will occur at a frequency where each integrator has unity gain i.e., where $1/\omega RC = 1$ (where $R_1 = R_2 = R$ and $C_1 = C_2 = C$). For different frequency ranges different matched pairs of capacitors can be selected using band switch arrangement. The resistors R_7 applies a small amount of 'negative damping' to ensure that oscillator starts as soon as the circuit is switched on. The amplitude is limited by using zener diodes D_1 and D_2. The module consisting of operational amplifiers A_1, A_2 and A_3 now develops a total phase shift of 360° and constitute a positive feedback loop with unity gain which will stimulate and sustain stable oscillations.

Measurements on superionic conductors have shown that the sample resistance often becomes a few ohms at temperatures $T \geqslant T_t$, where T_t is the insulator to electrolyte transition temperature. As the operational amplifiers are limited by its maximum output current, the oscillator output has to be boosted before it is allowed to excite the sample. This may however be accomplished by adding power transistors Q_1 and Q_2 which provide sufficient current to drive the sample. The use of such a pair of NPN and PNP transistors in the output stage is also referred to as complementary symmetry. The input stage of the buffer also includes a trimpot for adjusting the voltage level required to excite the sample.

2.2 *Current-to-voltage converter*

Figure 3 shows the current-to-voltage converter (CVC). This operates on the principle that the current through the input impedance (Z_x) and the feedback resistors (R_f) will always be equal in order to maintain zero voltage difference between the two inputs. The unknown impedance (Z_x) may then be calculated using the Kirchoff law as

$$Z_x = (v_i R_f)/v_z.$$

If Z_x is a purely resistive element, then there will only be a change in the amplitude of the exciting signal (v_i) with no change in the phase. But if Z_x is purely capacitive, then there will not only be a phase difference between the output and input signals but also a change in their amplitudes. Generally if Z_x is a complex impedance which involves both resistive and capacitive reactances in parallel or in series, the output signal undergoes both amplitude and phase modulations.

The real and imaginary parts of Z_x are derived using lock-in technique with the

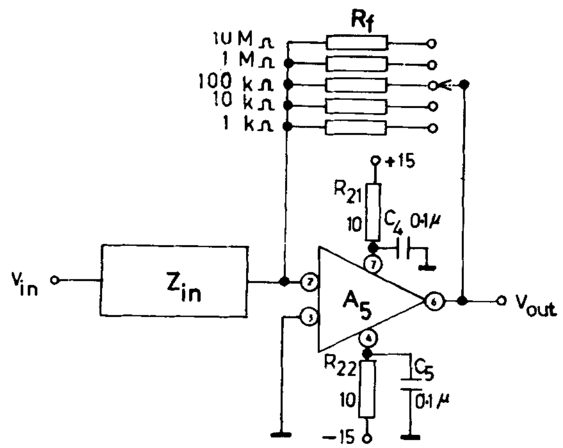

Figure 3. Current-to-voltage converter. A_5 = NF 357. The feedback resistors are 0·1% tolerance metal film resistors with virtually zero stray reactance.

help of phase sensitive detector and represented as $Z \cos\theta$ versus $Z \sin\theta$ along the x-axis and y-axis of a complex-Z plane, in the so called impedance plot (one could also present these results in the form of an admittance plot or modulus plot). The various forms of impedance/admittance spectra provide detailed and separate information about all possible combinations of R_x and C_x. This is done by comparing these experimental plots with those that could be generated by equivalent circuit models (Macdonald 1976; Bauerle 1969).

As mentioned by Nelson, selection of the operational amplifier for use as a CVC is a crucial aspect of its design; one should select an operational amplifier with a high input impedance and wide unity gain bandwidth product. NF 357 having an input impedance of 10^{13} ohms in parallel with less than 3 pf and 20 MHz unity gain bandwidth product is used as a CVC in our experiment.

Another important aspect of design is the selection of reference resistors. One should use perfectly non-reactive resistors as standards. For this purpose one could either prefer 0·1% metal film resistors or 0·1% wire wound resistors whose reactive components are nullified by symmetrical opposite windings. These non-reactive resistors are checked thoroughly before their use as standard resistors. 0·1% metal oxide resistors were found unsuitable as references, as they exhibit considerable reactive components.

2.3 *Phase sensitive detector*

During conductivity measurements the signals of interest are always accompanied by high levels of noise and interference due to $1/f$ noise, AC pick ups and thermoelectric voltages. The main purpose of using phase sensitive detectors (PSD) is to reject totally all these unwanted signals. This is achieved by limiting the bandwidth of detection to that just necessary to include the range of frequencies occurring in the signal. Signals at other frequencies are averaged to zero and thus a greatly improved signal-to-noise ratio is achieved.

Several phase sensitive detectors have been described in the literature with electronic switching for rectification (Williams 1970; Blair and Sydenham 1975; Sthanapathi *et al* 1977), with different circuit configurations. We opted for a different technique for the demodulation. Two square waves 180° out of phase to each other are used to control two pairs of switches. The outputs from this switching network pass through the low-pass filter and a differential amplifier. Because of its high input impedance the differential amplifier isolates the output circuit from the PSD circuit and provides a low output impedance suitable for connecting it to even an ordinary multimeter.

$$\text{If } v_i[V_i \sin\omega t],\quad v_z[V_z \sin(\omega t+\phi)] \quad\text{and}\quad v_r[V_r \sin(\omega t+\theta)]$$

are the excitation, CVC output and reference signals respectively with ϕ-the phase difference introduced by the reactive component of Z_x and θ-the angle of reference signal set with respect to excitation signal, then the multiplier output is

$$\begin{aligned} v_z v_r &= \tfrac{1}{2} V_z V_r[\sin(\omega t+\phi)\sin(\omega t+\theta)] \\ &= \tfrac{1}{2} V_z V_r[\cos(\theta-\phi)-\cos(2\omega t+\theta-\phi)] \end{aligned}$$

the second component of which is completely rejected by the low-pass filter. The alternate positive and negative DC components corresponding to the alternate half cycles of modulated AC signal (V_z) are added using a differential amplifier whose output is given by

$$V_0 = \tfrac{1}{2} V_z V_r \cos(\theta - \phi).$$

If the chosen impedance is purely resistive (i.e., $\phi = 0°$) then the output of the detector is

$$V_0 = \tfrac{1}{2} V_z V_r \cos\theta,$$

whose real and imaginary parts can be separated by properly choosing the inphase ($\theta = 0°$) and quadrature phase ($\theta = 90°$) signals as reference. The corresponding output of the detector will be

$$V_0 \text{ (with } \theta = 0°) = \tfrac{1}{2} V_z V_r,$$

$$V_0 \text{ (with } \theta = 90°) = 0.$$

If the chosen impedance also includes some reactive components the quadrature output will always be non-zero. Correspondingly the inphase output will be less than the maximum output $\frac{1}{2} V_z V_r$.

In the present design the PSD consists of a phase shifter, a zero-crossing detector, an inverter, a switching network, a low-pass filter and a differential amplifier.

The reference signals (0° and 90° phases) are derived from the same quadrature oscillator. These signals are sent through the phase shifter to adjust the phase accurately, so that the reference (v_r) can be precisely set in phase or 90° out of phase with the excitation signal (v_i) applied to the sample. Part (a) of figure 4 shows the phase shifter. This has a gain of unity and enables continuous phase adjustment from 0° to 180°.

The reference signal from phase shifter is sent to the zero crossing detector (ZCD) which is a high speed voltage comparator (response time ~ 200 ns). Basically this ZCD-acts as a high gain amplifier which can change its state each time the input signal changes direction. Thus the circuit part (b) of figure 4, squares the input signals into a series of rectangular output pulses with rising and falling slopes corresponding to the input zero crossing.

Two square waves differing by 180° are generated using the CMOS 4049 (Fairchild 1977a) inverting buffers and are used as control signals for the switching action which is the heart of PSD.

The switching is done by CMOS FET 4066 (Fairchild 1977b) which possesses four independent bilateral analog switches. Two switches are controlled by one square wave (reference 1) and the other two by the other inverted square wave (reference 2). Only those input signals that are in synchronization with the carrier frequency are extracted. The switching action may be clearly understood by looking at figure 5.

The output of the switches are then applied to the low-pass filter which is an RC network in our case. This smoothes out the ripple components of the signals coming from FET switches and supplies positive DC voltage and ground to the non-inverting and inverting inputs of differential amplifer, during positive half cycles of reference 1. During the negative half cycles of reference 1, the switching occurs such that the low-pass filter delivers negative DC voltage and ground to the inverting and non-inverting inputs. Being a differential amplifier this last stage simply adds the

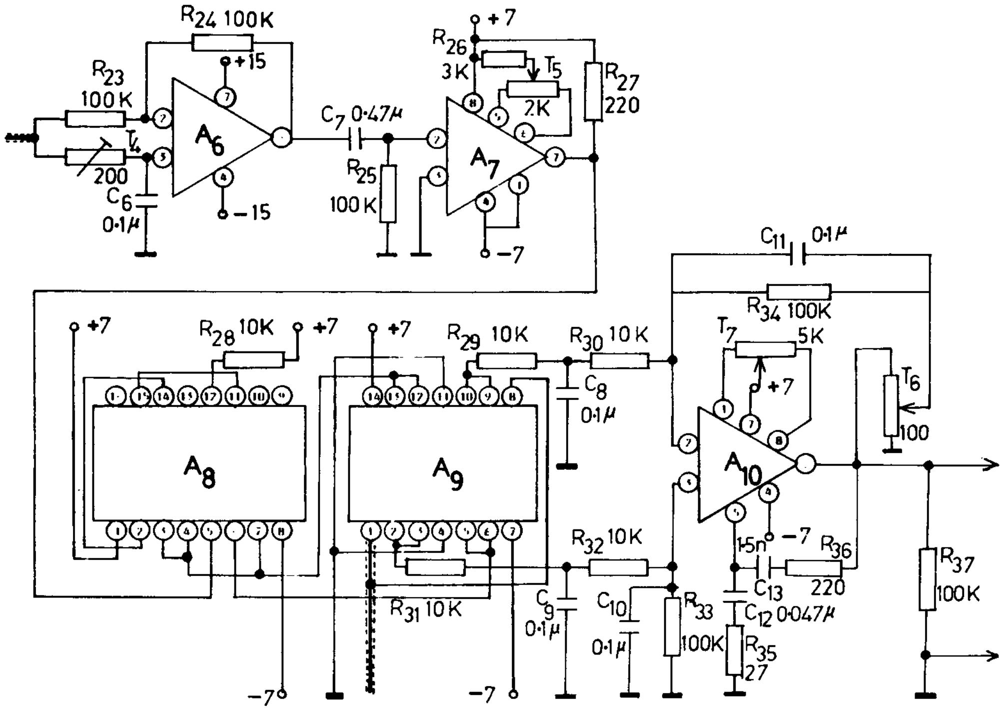

Figure 4. Phase sensitive detector. A_6 = NF 356; A_7 = LM 311; A_8 = CMOS 4049; A_9 = CMOS 4066; A_{10} = 725; The frequency compensation for A_{10} is done externally as shown.

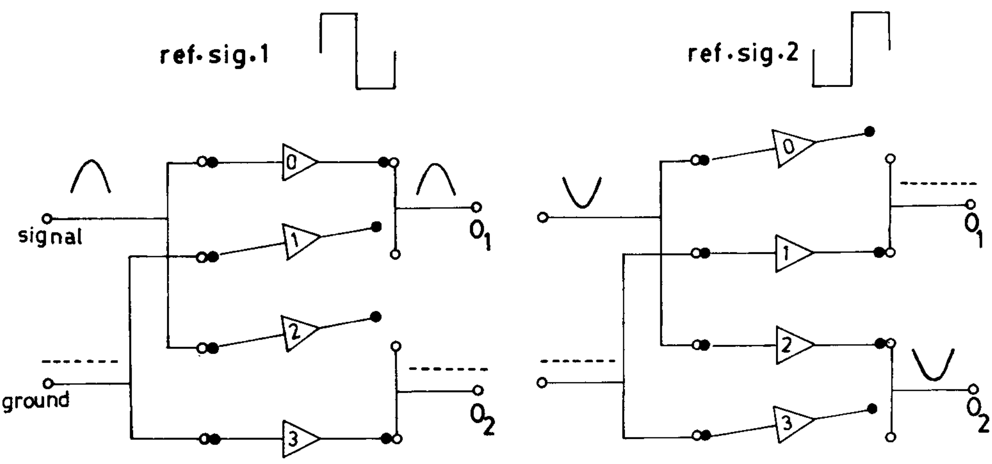

Figure 5. Switching action of A_9 (of figure 4). FETs 0 and 3 are controlled by reference signal 1, while 1 and 2 are controlled by reference signal 2. Outputs O_1 and O_2 are sent to the non-inverting and inverting inputs of differential amplifier.

inputs and delivers a positive DC voltage. Proper care was taken using offset trimpot and appropriate resistors to eleminate the offset voltages due to FET switches and differential amplifier.

3. Experimental procedure

The Au/electrolyte/Au configuration mounted in an electrically shielded conductivity cell is connected to the inverting input of the CVC. Perfect shielding is mandatory to avoid the AC pick ups from the furnace particularly at high temperature ranges. We employed a furnace giving very low inductive noise to avoid this difficulty to a considerable extent. In addition, a thick stainless steel sheet (connected to main ground) was inserted in between the conductivity set up and the furnace. The furnace body input and output terminals of the sample are also shielded perfectly.

The 0° phase output of the oscillator is boosted using the buffer stage and its output is adjusted to ~ 100 mV peak to peak. As the voltage levels at different frequencies seem to show slight variations, the constancy of the input signal to the sample is checked at several selected frequencies using the detecting stage. The output of the synchronous detector is made zero by adjusting the signal (v_i) and the reference (v_r) into quadrature at the multiplier using the phase shifter. The detector output with reference (v_r) and exciting signal (v_i) in-phase at the multiplier now measures the voltage level to be used as input. This signal is allowed to excite the sample at the input of CVC, and appears as the measurand signal (both amplitude and phase modulated) at the output of CVC. This measurand signal (v_z) is now sent to the detecting part for further analysis with 0° and 90° phases as reference signals to extract the corresponding real and imaginary parts of impedance Z_x.

4. Performance achieved

The working of the instrument has been tested by performing complex admittance/impedance and AC conductivity measurements on (a) sintered polycrystalline pellet

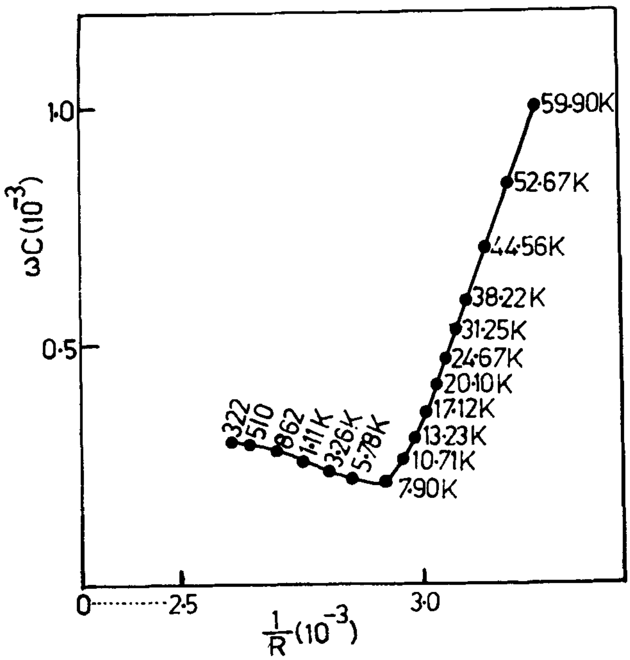

Figure 6. A typical complex-admittance plot of the 40% Li_4SiO_4–60% Li_3VO_4 sintered pellet at 468 K.

of 40% Li_4SiO_4–60%Li_3VO_4 in the temperature range 100–350°C and (b) 30% Li_2O–70% TeO_2-glass in the temperature range 70–200°C at various frequencies upto 60 kHz using two probe method. The CVC also allows us to prefer the three probe measurement.

The data collected in the present cases are analysed in the form of admittance/impedance plots. A typical admittance plot is shown in figure 6 for 40 %Li_4SiO_4–60% Li_3VO_4 sintered pellet. This profile very closely resembles one of the theoretical admittance plot of Bauerle (1969) for a model circuit comprising a resistance and a series capacitance in parallel with another capacitance. The abrupt rise in the admittance, suggests that the sample is becoming more and more capacitive. The bulk DC conductivity of polycrystalline lithium silicate-lithium vanadate and glassy lithium oxide-tellurium oxide systems are separated from the grain boundary contributions by the analyses of all admittance/impedance plots and presented as a

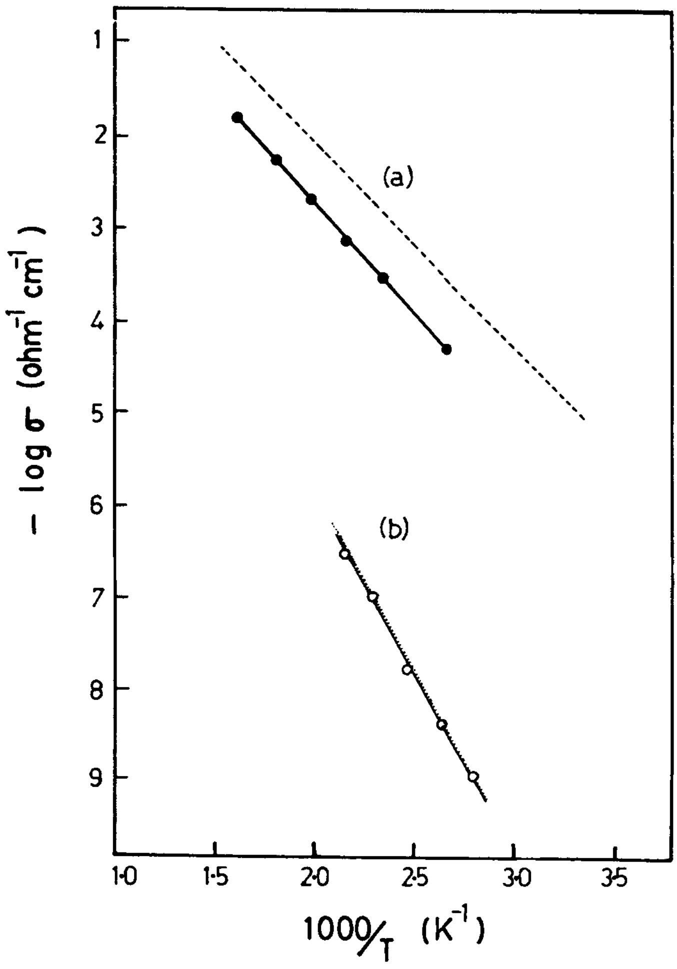

Figure 7. Temperature dependence of the conductivity of (a) polycrystalline 40% Li_4SiO_4–60%Li_3VO_4 and (b) 30% Li_2O–70% TeO_2 glass, extracted from admittance/impedance plots at different temperatures, shown as Arrhenius ($\log \sigma$ vs. $10^3/T$) plot. Dashed line: data of West (1984). The difference is due to the ageing effect on polycrystalline sample stored for about 3 years. Dotted line: data of Tanaka *et al* (1988).

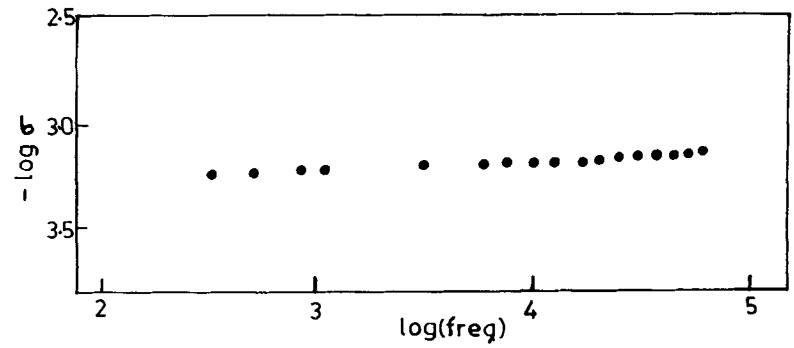

Figure 8. Frequency dependence of total AC conductivity of 40% Li_4SiO_4–60% Li_3VO_4 at 468 K shown as $\log\sigma$ vs. $\log f$ plot.

$\log\sigma$ vs. $10^3/T$ plot shown in figure 7. The activation energies deduced from these DC plots are 0·49 eV and 0·79 eV for the polycrystalline and the glassy systems.

After applying the exciting signal (v_i) at a particular frequency to the sample, the inphase reference is slowly adjusted using phase shifter to give a maximum voltage at the output. This voltage is used for the calculation of total AC conductivity at that frequency. Figure 8 shows log (total AC conductivity) vs frequencies at 468 K of 40% Li_4SiO_4–60% Li_3VO_4.

5. Other possible applications

The real (ε') and imaginary (ε'') components of the complex dielectric constant ε^* of ionic and electronic materials may also be determined from the same results obtained with non-reactive resistors as feedback elements using the relations

$$\varepsilon' = (\sigma''(\omega))/\omega,$$

and

$$\varepsilon'' = (\sigma'(\omega))/\omega.$$

One drawback of this direct calculation from conductivity results is that the measurement sensitivity falls with decreasing frequency. One could possibly overcome this problem by using standard capacitors with negligible stray conductance as feedback elements instead of resistors. The results obtained with 0° and 90° phases as reference signals can now be directly used for the calculation of ε' and ε'' along the x and y-axes of the complex plane. Use of capacitors as feedback element (instead of resistors) is more advantageous because, suitable capacitors with virtually zero stray conductance (normally $C_f = 10$–100 pf) are more easily obtained than resistors of 10^1–$10^7\,\Omega$ with negligible stray reactances. Using this set up AC measurements on high T_c superconductors are being done, the results of which will be reported later.

6. Conclusions

An electronic system was specially designed and fabricated for the measurement of total AC conductivity and complex admittance/impedance. This system gives reliable and accurate data at various frequencies upto 60 kHz. Though the CVC technique was used by Nelson for the total AC conductivity measurement, the separation of real and imaginary parts of complex admittance/impedance from the distorted signal coming out of CVC, by a phase sensitive detector is new as far as our knowledge goes. The CVC technique for the AC conductivity is also not well known in the field of superionic conductors. As these materials are very well known to have resistances (of the order of 10^6–$10^8\,\Omega$), at ambient temperatures, the conventional technique of connecting a standard resistor in series with the sample and measuring the AC voltage drop across the sample, using Lock-in amplifier or frequency response analyser always introduces impedance mismatching problem, whereas CVC, which does not introduce any such problem would conveniently measure up 200 MΩ (with $R_f = 10\,M\Omega$) at the lowest frequency possible. Application of this technique to a Li_2O–TeO_2 glass composition and Li_4SiO_4–Li_3VO_4 sintered polycrystalline pellet has helped isolate the grain boundary contribution to conductivity and deduce activation energies for Li^+ ion conduction. The PSD described here has definite advantages in terms of effective noise rejection, simplicity and low cost. These features permit construction of this instrument very easily even in small research laboratories.

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