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Effect of $CuIn_{1-x}Al_xSe_2$ (CIAS) thin film thickness and diode annealing temperature on Al/p-CIAS Schottky diode

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Abstract. Al/p-CIAS Schottky diodes were fabricated by depositing aluminium (Al) on different flash evaporated copper–indium–aluminium–diselenide (CIAS) films of varying thickness. Further, all diodes were annealed at 573 K for an hour. The influence of p-CIAS film thickness and the thermal annealing of Al/p-CIAS Schottky diode were investigated by observing current–voltage (*I–V*) and capacitance–voltage (*C–V*) characteristics at room temperature. Various diode parameters, such as ideality factor (η), barrier height (ϕ_{bo}) and series resistance (R_s) were calculated using Cheung's and Norde methods. ϕ_{bo} found to increase with annealing as well as with increase in the film thickness. However, the value of η and R_s decreases with annealing and CIAS thickness. The effective density of states (N_v), acceptor density of states (N_A) and barrier height have been calculated from *C–V* measurements. Values obtained from CV analysis were well matched with *I–V* results. The value of N_v decreases and the value of N_A increases with the increase in the film thickness. Using *I–V* and *C–V* parameters, energy band gap for the prepared Al/p-CIAS diodes has been reconstructed.

Keywords. Thin film Schottky diode; current–voltage (*I–V*) measurement; capacitance–voltage (*C–V*) measurement; energy band diagram.

1. Introduction

In the recent years, many optoelectronic devices which have properties of barrier height enhancement and good thermal stability are getting more attention. Such devices are organic field effect transistors, photovoltaic cells, Schottky diodes, negative-resistance devices, switching and memory systems, thermistors, etc. [1–4]. In the category of photovoltaic cell and Schottky solar cell, $CuIn_{1-x}Al_xSe_2$ (CIAS) is a promising p-type direct band gap absorber layer, because the band gap of it can vary from 1.0 to 2.7 eV simply by varying Al/In ratio [5]. These affect electrical properties too. Many researchers focus on one or both properties of CIAS thin films.

In 1990, Gebicki *et al* [5] produced bulk semiconductor CIAS with x in the range between 0 and 1. The pure elements were supplied using a chemical transport method in which iodine was the transport agent [5]. The variations in lattice constants a and c with the composition were recorded. They were found to obey Vegard's law in both cases. In 1998, Itoh *et al* [6] reported the preparation of CIAS by depositing a stack of In(Al)/Cu/Se/Cu/Al(In) using vacuum evaporation and then heating the whole stack in vacuum. The results show that the resistivity and energy band gap of the CIAS thin films were found to increase with Al content. In addition, non-linear changes in lattice constants a and c were reported with increased Al content. US researchers from the IEC at Delaware, produced single phase CIAS thin films using multisource elemental evaporation in which the elements Cu, In, Al and Se were co-evaporated onto soda-lime glass (SLG) or Mo-coated SLG substrate [7]. They reported that energy band gap was varied over the range of 1.0–1.74 eV with an increase in Al content. In addition to that for the first time, they have reported that the solar devices produced using CIAS absorber films; an efficiency of 11% was obtained for $x = 0.26$. Two years later, same group reported a device efficiency of 16.9% for a CIAS solar cell with absorber of thickness 2.0–2.5 μm and a band gap of 1.16 eV [8]. The increase in device performance was achieved due to significant improvements in the device fabrication process, such as the addition of thin Ga layer (5 μm) by sputtering onto the Mo-coated SLG substrate, which improvises the adhesion of the absorber film to the Mo back contact for temperatures >500°C. Reddy and Raja [9] reported the production of $CuIn_{1-x}Al_xSe_2$ thin films (with $x = 0.7$) by a four-source co-evaporation method with an aim of using such layers in tandem solar cell structure. Those films were single phase, stoichiometric and p-type in conductivity ($\rho = 140\ \Omega$ cm). Takao Hayashi *et al* [10] deposited CIAS thin films by molecular beam epitaxy on a

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Mo/SLG substrates by the three source evaporation process. Recently Kim *et al* [11] reported RF-sputtered 3-layer structure of CIAS thin film; they observed a low resistivity of the order of 10^{-2} Ω cm was obtained in the $CuIn_{1-x}Al_xSe_2$ thin films with $x = 0.74$.

Very few reports on Schottky devices based on quaternary semiconductor thin films have been reported. The metal semiconductor (MS) interface plays a major role in the functioning of any electronic and optoelectronic devices. Hence, major focus is on the electronic transport through the Schottky barrier height (SBH). New heterojunction thin film-based solar material is known for the low-cost high efficient devices, having a better control in the grain and the charge distribution. This envisioned the utilization of CIAS thin films for preparing and for feasibility study of Schottky diode. Considering the relevant and recent report i.e., Touati *et al* [12] reported Schottky device having 400-nm thick thermally evaporated CZTS thin film. They observed that the Schottky barrier height was 0.807 eV. The other Schottky parameters, such as series resistance and ideality factor were estimated by Cheung and Cheung method [13]. In the present work, we followed the same method for estimating the Schottky parameters. In addition, we have estimated the barrier height inhomogeneity at interface by Norde method [14]. Our earlier study focussed on the barrier height inhomogeneity of MS interface at different device temperatures [15] and the present study focusses on the influence of film thickness and the annealing temperature on the Al/CIAS Schottky devices. The structural, optical, morphological and electrical properties of CIAS were already reported in the previous work [16].

2. Experimental

Al/p-CIAS Schottky diodes were made by depositing $CuIn_{1-x}Al_xSe_2$ ($x = 0.19$) thin film on to the 500 nm thick silver (Ag), ohmic contact, coated glass substrate using flash evaporation method. The preparation method for $CuIn_{1-x}Al_xSe_2$ ($x = 0.19$) compound, used for evaporation, was well described in our earlier work [16]. In addition, we had deposited and optimized CIAS thin film according to the optimized deposition and annealing parameters as per the previous work done [16], viz. deposition temperature was 273 K, deposition rate was 0.3–0.4 nm s^{-1}, annealing temperature was 573 K, time duration of annealing was 1 h and the base pressure for annealing was 10^{-3} mbar. The thickness of the film was measured using quartz crystal thickness monitor (Hindhivac make). The Schottky contact, i.e., aluminium (Al) was deposited onto the glass/Ag (+ve ohmic contact)/CIAS structure using a stainless steel mask (diameter of 0.1 mm), at room temperature by thermal evaporation (technique) having a deposition rate of 0.5–0.6 nm s^{-1}. The thickness of CIAS and Al thin films was measured by quartz crystal thickness monitor. All evaporation processes were carried out in a vacuum coating unit at about 10^{-6} mbar. In this work, we had prepared Schottky diodes by varying the thickness of the CIAS films viz. 200, 500 and 700 nm, and examined the influence of CIAS thin films thickness and thermal annealing on the Schottky diode parameters. The schematic diagram of CIAS Schottky diode and its measurement setup is shown in figure 1.

The fabricated CIAS Schottky diodes (glass/Ag/CIAS/Al) were tested by current–voltage (*I–V*) as well as capacitance–voltage (*C–V*) behaviours using computer interfaced *I–V*/*C–V* setup comprising of a programmable source meter (Keithley make, model 2400), precision programmable LCR meter (Agilent make, model 4284A), cryogenic setup (Janis make, model Cryodyne 22CP CTI) equipped with compressor (model 8200 CTI) and temperature controller (Lake Shore make, model 321). The interfacing of these instruments was established by using LabVIEW software by National Instruments, USA.

3. Results and discussion

3.1 *Current–voltage (I–V) characterization*

The semi-logarithmic current–voltage (*I–V*) characteristics, both forward and reverse biases of Al/CIAS Schottky diodes having a different thicknesses of CIAS thin film as well as annealed are shown in figure 2. *I–V* characteristics revealed that the diode current increases as the thickness is increased in forward bias. However, the same has been found to decrease with increase in thickness under reverse bias condition.

Improvement in the diode current for thicker and annealed Schottky diodes can be explained by the increase in grain size, reducing the grain boundaries and better enforcement of crystal growth [17]. To find the diode parameters from the *I–V* plot, one can notice from the non-linear region of the semi-logarithmic forward *I–V* curves caused by the presence of the effect of R_s, apart from that a complex facet arises due to a number of non-interacting parallel diodes with grain boundaries of barrier heights act simultaneously. This causes misplay in the extraction of diode parameters [18].

Similarly, semi-logarithmic reverse characteristics of the diode demonstrate non-saturating response can be explained on the basis of the spatial inhomogeneity of barrier heights [13], majorly due to the current flow through the low barrier heights patches. Again, there is a possibility to acquire faulty diode parameters. With the objective of accurately determining the ideality factor, barrier height and series resistance of the Al/CIAS Schottky contacts, Cheung's [13] method was employed. According to Cheung's functions, the relation between applied voltage and current can be written as:

$$\frac{d(V)}{d(\ln I)} = R_s I + \left(\frac{\eta kT}{q}\right). \quad (1)$$

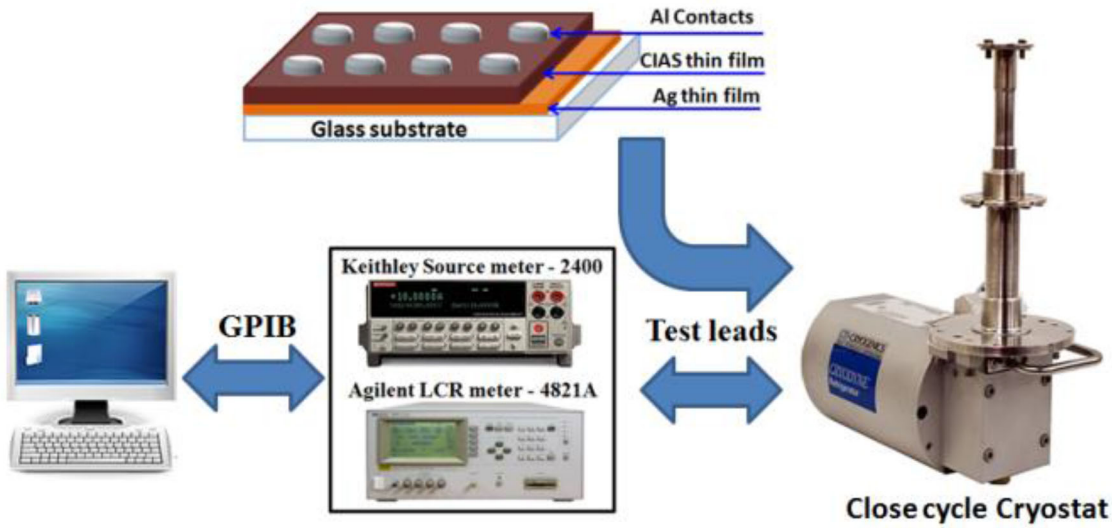

Figure 1. Schematic of CIAS Schottky diodes and its measurement setup.

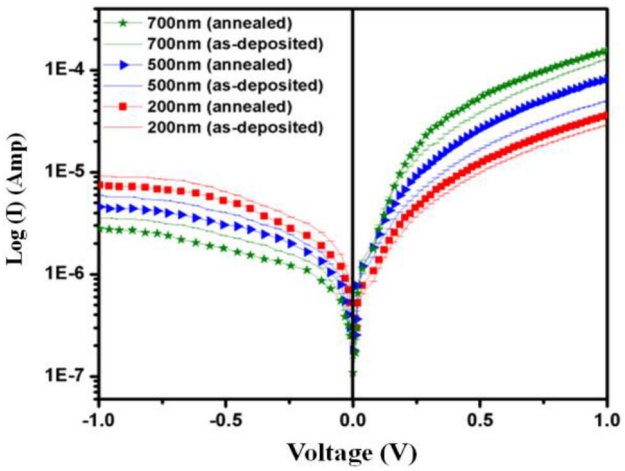

Figure 2. Log (*I*)–*V* characteristics of as-deposited and annealed Al/p-CIAS Schottky diodes.

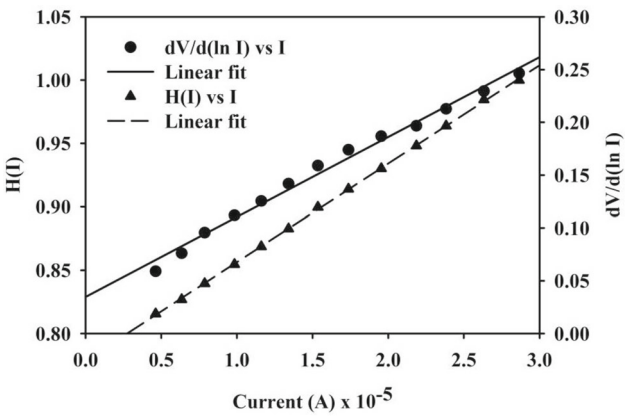

Figure 3. $d(V)/d(\ln I)$ and $H(I)$ variations with respect to observed Schottky diode current.

Thus, a plot of $d(V)/d(\ln I)$ *vs. I* (shown in figure 3) will give the value of R_s and η. To evaluate ϕ_{bo}, we can define a function $H(I)$ given as:

$$H(I) = V - \left(\frac{\eta kT}{q}\right)\ln\left(\frac{I}{AA^{**}T^2}\right). \tag{2}$$

For equation (2), we can deduce:

$$H(I) = R_s I + \eta\phi_{bo}. \tag{3}$$

From the plot of $H(I)$ *vs. I* (shown in figure 3), we can determine the value ϕ_{bo} and R_s, which can be used to check the consistency in the values calculated from equation (1).

Thus, the calculated values of R_s, ϕ_{bo} and η of Al/CIAS diodes having different thicknesses, as deposited and annealed, are tabulated in table 1, and the variation is shown graphically in figure 4.

Looking at the ideality factor values of the diodes from table 1, one can reveal that there is an obvious improvement observed as the thickness of CIAS increases and on annealing. The best observed value of diode factor is 1.62 for 573 K annealed and 700 nm thick CIAS Schottky diode. Similarly, for the same fabrication condition of Schottky diode, we observed the minimum series resistance viz. 6.8 kΩ. Very negligible overall improvement in the barrier height, i.e., 0.57–60 eV can be observed.

According to equation (3), we can say that the high values of series resistance hinder precise evolution of barrier height. Norde [14] employed a method that evaluates barrier height from the standard *I*–*V* plot. The modified Norde function can be defined as:

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\left(\frac{I(V)}{AA^{**}T^2}\right), \tag{4}$$

where γ is the first integer $>\eta$. Here, γ has been taken as 2, A the diode area = 9×10^{-2} mm^2, A^{**} effective Richardson

Table 1. Experimental values of barrier height (ϕ_{bo}) and ideality factor (η) are calculated using Cheung's function for Al/p-CIAS Schottky diodes with and without annealing.

CIAS thickness (nm)	Annealing temperature, T_a (K)	Barrier height, ϕ_{bo} (eV)	Ideality factor, η	Series resistance, R_s (kΩ)
200	Unannealed	0.57	2.06	13.7
	573	0.58	2.01	11.9
500	Unannealed	0.58	1.90	10.6
	573	0.59	1.83	9.3
700	Unannealed	0.59	1.76	8.1
	573	0.60	1.62	6.8

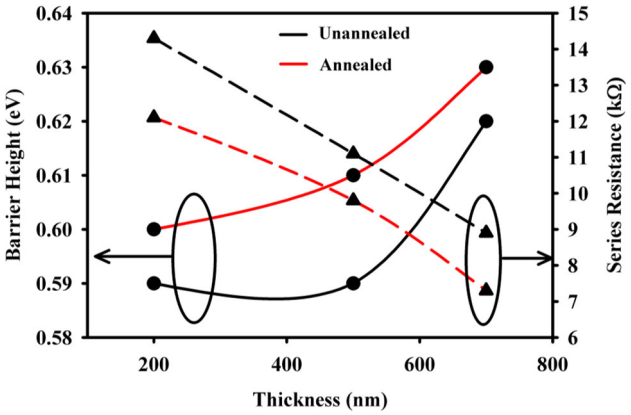

Figure 4. Variations in barrier height and series resistance as a function of CIAS film thickness, calculated using Cheung's function.

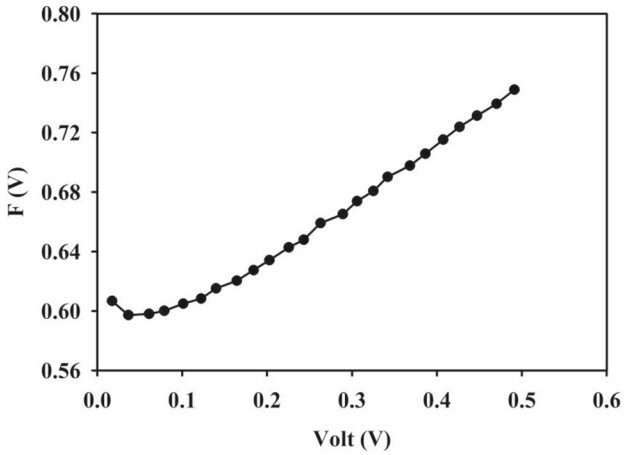

Figure 5. Norde's $F(V)$ variation with respect to applied voltage (V) for the Schottky diodes.

constant = 30 A cm^{-2} K^{-2} and the barrier height of device can be obtained by using:

$$\phi_{bo} = F(V_0) + \frac{V_0}{\gamma} - \frac{kT}{q}, \tag{5}$$

where $F(V_0)$ is the minimum value of $F(V)$ *vs.* V graph (shown in figure 5) and V_0 is the corresponding voltage.

The series resistance using Norde's method has been calculated through the relation:

$$R_s = \frac{kT(\gamma - \eta)}{qI}. \tag{6}$$

The values of barrier height and series resistance are tabulated in table 2. Very minute changes in the values of barrier height and series resistance were observed in comparison with Cheung's method (table 1). The ideality factor improves (decreases) and barrier height increases as thickness as well as annealing temperature increase. Improvement in the ideality factor implies that the current flows through the grains and its boundaries rather to the patches, that ultimately responsible to obtain the increasing behaviour of the barrier height with thickness and that of annealing temperature. Biber *et al* [19] also observed linear relationship between experimental effective barrier heights and ideality factors of Schottky contacts.

3.2 *Capacitance–voltage (C–V) characterization*

The basic C–V relationship for MS Schottky barriers was discussed in the earlier work [15,20]. $1/C^2$–V characteristics for as-deposited as well as annealed Al/p-$CuIn_{0.81}Al_{0.19}Se_2$ Schottky diodes have been presented in figure 6 (range is 0 to −2 V). The annealed samples provided lower value of capacitance as compared to corresponding as-deposited diodes, which caused increase in their barrier height values, since the lower capacitance values suggest a higher built-in voltage and consequently, a higher barrier height. The Schottky diode parameters extracted from $1/C^2$–V measurements have been illustrated in table 3.

The value of acceptor density of states (N_A) as calculated from the slope of reverse bias C^{-2}–V characteristics is found to be in the order of 10^{19} cm^{-3} and is in close agreement with that obtained from electrical analysis [15]. We have taken the dielectric constant of the film as 13.6 and the effective mass of hole is 0.71 for the calculation of C–V parameters. Table 3 suggests that as the thickness and annealing temperature increase, the values of N_A increase. The conclusions drawn from these parameters suggest that annealing the diodes leads to an increase in the barrier height and an improvement (decrease) in the ideality factor.

Table 2. Experimental values of barrier height (ϕ_{bo}) and series resistance (R_s) are calculated using the Norde's method for Al/p-CIAS Schottky diodes with and without annealing.

CIAS thickness (nm)	Annealing temperature, T_a (K)	Barrier height, ϕ_{bo} (eV)	Series resistance, R_s (kΩ)
200	Unannealed	0.59	14.3
	573	0.60	12.1
500	Unannealed	0.59	11.1
	573	0.61	9.8
700	Unannealed	0.62	8.9
	573	0.63	7.3

Table 3. Various electrical parameters deduced by the $1/C^2$–V measurement.

CIAS thickness (nm)	Annealing temperature, T_a (K)	Effective donor density of states × 10^{18} N_v (cm^{-3})	Effective acceptor density of states × 10^{19} N_A (cm^{-3})	Barrier height ϕ_{cv} (eV) (±0.01)
200	Unannealed	1.15 ± 0.02	1.08 ± 0.02	0.74
	573	1.20 ± 0.03	1.12 ± 0.03	0.75
500	Unannealed	1.26 ± 0.03	1.11 ± 0.03	0.76
	573	1.31 ± 0.04	1.16 ± 0.01	0.77
700	Unannealed	1.38 ± 0.03	1.15 ± 0.02	0.77
	573	1.44 ± 0.02	1.21 ± 0.03	0.78

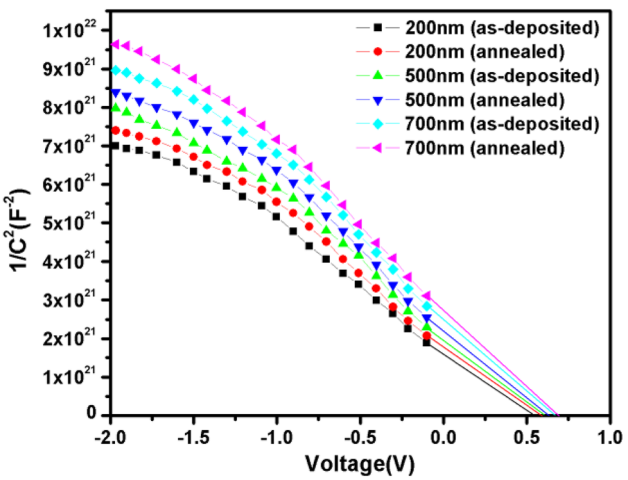

Figure 6. $1/C^2$–V characteristics of as-deposited and annealed Al/p-CIAS Schottky diodes.

3.3 *Energy band diagram of Al/p-CIAS Schottky diode*

Interfacial layer between the metal/semiconductor and the interface states plays a vital role in the determination of the Schottky barrier parameters. For the determination of electron affinity (χ) of the semiconductor, it has relation with the barrier height (ϕ_{bo}) and work function of the metal (ϕ_m), as follows:

$$q\phi_{bo} = E_g - q(\phi_m - \chi), \tag{7}$$

where ϕ_{bo} is the barrier height of Al/p-$CuIn_{0.81}Al_{0.19}Se_2$ Schottky diodes (0.78 eV) and E_g the band gap of the p-type semiconductor i.e., E_g = 1.24 eV [16].

The electron affinity (χ) of $CuIn_{0.81}Al_{0.19}Se_2$ has been calculated as 3.82 V. Further, the work function semiconductor (ϕ_s) has a relation with work function of the metal (ϕ_m) and built in potential (V_{bi}) as:

$$q\phi_s = q(\phi_m + V_{bi}). \tag{8}$$

The value of work function for p-$CuIn_{0.81}Al_{0.19}Se_2$ is equal to 4.98 eV. Using the above values of various parameters, equilibrium energy band diagram for the p-$CuIn_{0.81}Al_{0.19}Se_2$/Al Schottky diode has been plotted and presented in figure 7.

In the present case, the value of the metal work function is low compared to that of semiconductor (i.e., $\phi_m < \phi_s$), electrons will move from metal to semiconductor. Each electron flowing into the semiconductor removes a hole from the valence band, leaving neutralized charge of ionized acceptor in the semiconductor and thus, forming a potential barrier at the metal–semiconductor interface region [21]. Since the current in a p-type semiconductor is carried mainly by holes, the contact behaviour seems to be a Schottky with a barrier height of ∼0.78eV.

Alike with CIAS Schottky diode, rectifying characteristics of Pt/$Al_{0.08}In_{0.08}Ga_{0.84}N$ Schottky diode show the barrier height and ideality factor as 0.76 eV and 1.03, respectively, by optimizing annealing temperature of the device [22]. Atasoy *et al* [23] reported the fabrication of

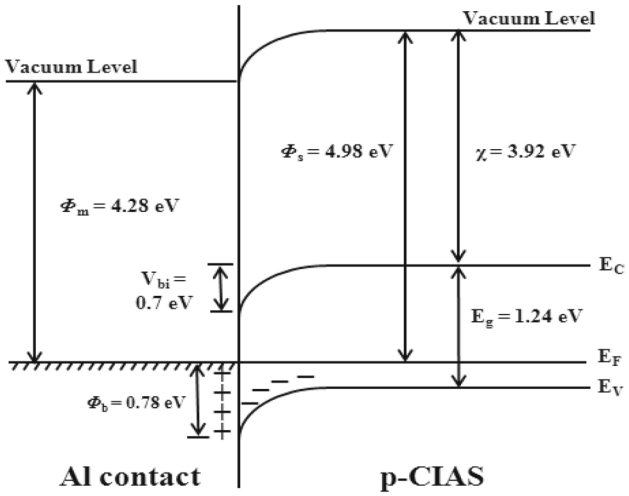

Figure 7. Energy band diagram of Al/p-CIAS Schottky diode.

Schottky diode based on Cu_2ZnSnS_4 (CZTS) films. They adopted the device structure as Mo/CZTS/Al, and observed the values of n and ϕ_{bo} as 4.5 and 0.84 eV, respectively. Similarly, Touati *et al* [12] prepared the same structure (Mo/CZTS/Al), but they have observed better ideality factor i.e., 1.4 compared to Atasoy *et al* [23] work and the barrier height was about 0.807.

4. Conclusion

Al/p-$CuIn_{0.81}Al_{0.19}Se_2$ Schottky diodes were fabricated and the effect of semiconductor layer thickness and annealing over the characteristics of Al/p-$CuIn_{0.81}Al_{0.19}Se_2$ Schottky diode has been analysed on the basis of current–voltage (*I–V*) as well as capacitance–voltage (*C–V*) measurements. The results showed obtrusive influence of thermal annealing on Al/p-$CuIn_{0.81}Al_{0.19}Se_2$ Schottky diode, which improved their quality by reducing the values of series resistance, ideality factor as well as reverse leakage current and increasing the barrier height. Thus, depicting reasonably good quality Schottky diodes formed with 700 nm annealed CIAS layer.

References

[1] Lloyd G, Raja M, Sellers I, Sedghi N, Di Lucrezia R, Higgins S *et al* 2001 *Microelectron. Eng.* **59** 323
[2] Zhu M, Cui T H and Varahramyan K 2004 *Microelectron. Eng.* **75** 269
[3] Moiz S A, Ahmed M M and Karimov K S 2005 *ETRI J.* **27** 319
[4] Aydin M E and Turut A 2007 *Microelectron. Eng.* **84** 2875
[5] Gebicki W, Igalson M, Zajac W and Trykozko R 1990 *J. Phys. D: Appl. Phys.* **23** 964
[6] Itoh F, Saitoh O, Kita M, Nagamori H and Oike H 1998 *Sol. Energy Mater. Sol. Cells* **50** 119
[7] Paulson P D, Haimbodi M W, Marsillac S, Birkmire R W and Shafarman W N 2002 *J. Appl. Phys.* **91** 10153
[8] Shafarman W N 2002 *Proc. 28th IEEE Photovoltaic Specialists Conference, USA*, p 519
[9] Reddy Y B K and Raja V S 2006 *Sol. Energy Mater. Sol. Cells* **90** 1656
[10] Takao Hayashi, Takashi Minemoto, Guillaume Zoppi, Ian Forbes, Kiyoteru Tanaka, Satoshi Yamada *et al* 2009 *Sol. Energy Mater. Sol. Cells* **93** 922
[11] Kim N-H, Jun Y-K and Lee W-S 2016 *J. Nanosci. Nanotechnol.* **16** 1583
[12] Touati R, Trabelsi I, Rabeh M B and Kanzari M 2017 *J. Mater. Sci.: Mater. Electron.* **28** 5315
[13] Cheung S K and Cheung W N 1986 *Appl. Phys. Lett.* **49** 85
[14] Norde H 1979 *J. Appl. Phys.* **50** 5052
[15] Parihar U, Ray J R, Panchal C J and Padha N 2016 *Appl. Phys. A* **122** 568
[16] Parihar U, Sreenivas K, Ray J R, Panchal C J, Padha N and Rehani B 2013 *Mater. Chem. Phys.* **139** 270
[17] Cova P and Singh A 1990 *Solid State Electron.* **33** 11
[18] Rau U, Taretto K and Siebentritt S 2009 *Appl. Phys. A* **96** 221
[19] Biber M, Gullu O, Forment S, Van Meirhaeghe R L and Turut A 2006 *Semicond. Sci. Technol.* **21** 1
[20] Kaufmann E N 2012 *Characterization of materials*, 2nd edn (New York: John Wiley & Sons)
[21] Sze S M 1981 *Physics of semiconductor devices* 2nd edn (New York: Wiley)
[22] Abd-Shukor R, Awang R, Deraman M, Kamisah M M and Shamsudin R 2012 *Adv. Mater. Res.* **501** 226
[23] Atasoy Y, Olgar M A and Bacaksiz E 2019 *J. Mater. Sci.: Mater. Electron.* **30** 10435