Hybrid bilayer gate dielectric-based organic thin film transistors

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Abstract. Organic thin film transistors (OTFTs) are key building blocks for flexible, low cost electronics systems. They provide a viable alternative for silicon-based electronics with added advantages of low cost and flexibility. However, few issues like high-operating voltage, low-switching speed, high-leakage current and reliability are still a challenge. The overall performance of an OTFT depends on organic semiconductors and gate dielectric interface. In this paper, we review the current status and trends in the choice of dielectric layer for OTFTs. As a starting point, the performance parameters of an OTFT and their dependence on the dielectric layer are briefly discussed. A variety of dielectric materials which includes high- k inorganic, organic, surface coated inorganics and nanocomposites are also presented. The advantages and drawbacks of each of these materials are discussed in detail. We reviewed the latest developments in the dielectric materials especially, self-assembled monolayers (SAMs), hybrid bilayers and nanocomposites. SAM-based OTFTs offer several advantages but shift in the threshold voltage remains a concern. Nanocomposites are a latest addition to the dielectric materials, which offer advantages like solution processing and improved dielectric constant but have a rough surface. A hybrid bilayer that incorporates the inorganic dielectric as a base layer and a thin polymer layer over it to improve the surface properties offers several desirable characteristics over the other choices. Hence, we propose that hybrid bilayer gate dielectrics shall play a pivotal role in improving the OTFT performance.

Keywords. Organic thin film transistor; gate dielectric; high- k inorganic; low- k organic; self-assembled monolayer; hybrid bilayer.

1. Introduction

Over the past two decades, there has been a remarkable progress in the development of thin film transistors (TFTs) based on organic semiconductors (OSCs). These organic TFTs (OTFTs) are commonly used for display drivers in the back planes of active matrix organic light emitting diodes (AMOLEDs) [1], radio frequency identification (RFID) tags [2], sensors for tactile sensing [3] and memory applications [4]. Use of OTFTs instead of oxide TFTs or polycrystalline silicon TFTs offers a special advantage of flexibility to devices, making them bendable, rollable and foldable. At present, the two major challenges faced by OTFT technology over the existing TFT technology are: low field effect mobility ($<1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$) and high-operating voltage ($>10 \text{ V}$) [5]. Low field effect mobility, however, is an intrinsic property of OSCs and is attributed to the lack of band-like transport in OSCs. OSCs are molecular solids and a band-like transport is observed only at low temperatures [6]. In a molecular solid, molecules are loosely packed due to weak intermolecular forces. As a result, the charge carrier transport in these devices takes place through the hopping mechanism and results in poor mobility [7]. Since, low field effect mobility is an intrinsic property, several new OSCs have been investigated for improving the mobility in OTFTs [8–13]. Mobility can be

increased in OTFTs by tailoring the side chains, backbone networks of the OSCs [14]. Apart from mobility, operating voltage also remains a serious concern in OTFTs. Low operating voltage is necessary for portable, mobile and other battery operated applications. Therefore, a good number of studies have focused on reducing the operating voltage [15–18]. In addition to the above two aspects, reliability issue of OTFTs is also a concern and has been investigated by several research groups [19–21]. OTFTs should have good stability, longer life-time and should operate reliably when operated under different environmental conditions. Reliability is determined by observing the I – V characteristics of an OTFT when subjected to prolonged electrical stress either through constant voltage or constant current and mechanical stress applied in the form of bending and compression. Stability of an OTFT is predicted by observing its performance, when subjected to illumination, atmosphere and elevated temperature.

An insight into structure and operation of OTFTs can lead to a better understanding of what can be done to improve the performance of an OTFT. The most commonly used configuration of an OTFT is bottom gate top contact (BGTC) structure which is shown in figure 1. Other configurations of an OTFT, like bottom gate bottom contact (BGBC), top gate bottom contact (TGBC) and top gate top contact (TGTC) also exist [22–25]. BGTC structures are easy to fabricate

Figure 1. Schematic view of a BGTC OTFT.

and offer superior performance over the other three configurations [25]. An OTFT is a multilayer structure in which, charge carrier conduction between the source and drain terminals is controlled by potential applied on the gate terminal. Charge carrier conduction between the source–drain terminals takes place through a very thin layer (channel) formed at the interface of an OSC and a gate dielectric. Henceforth, an OSC is also referred to as an active layer. Potential applied on the gate terminal modulates the conductivity of an active layer and hence controls charge flow. Therefore, performance of an OTFT depends on the layers and nature of interface between any two adjacent layers. Hence, it is very important to properly choose each layer and tailor its interface with the adjacent layer to improve the performance of OTFTs. A substrate provides mechanical support, and acts as a base for the rest of device. Substrate material needs to be uniform, smooth, continuous, free from contamination, mechanically tough, flexible, thermodynamically stable, chemically nonreactive with the layers above it and should show good etch resistance for etchants for the layers above it. In case if the substrate is a conductor it can also be used as a gate electrode. However, in most cases a gate electrode is formed through sputtering of metals like aluminium, copper, silver or chromium [26–29]. A gate electrode layer should have good conductivity, smooth surface, a well-defined work function suitable for tuning the threshold voltage and should be easy to deposit at lower temperatures. A thin layer of insulator separates the gate and active layer. This gate dielectric layer introduces an electrostatic capacitive coupling between the gate and active layer. The amount of charge accumulated in the active layer (Q_{ch}) is proportional to capacitance offered by the dielectric layer as shown in equation (1):

$$Q_{ch} = C_i V_{GS} \quad (1)$$

where V_{GS} is the gate–source potential difference and C_i is given by the equation

$$C_i = \frac{\epsilon_0 \epsilon_r}{t} \quad (2)$$

where ϵ_0 and ϵ_r denote the dielectric constant of free space and the relative dielectric constant of the dielectric layer and t is the thickness of the dielectric layer. The two electrodes, source and drain are deposited over the active layer. They should have good adhesion with the active layer, low-temperature processability and suitable work function so as to improve the carrier injection efficiency.

In this paper, we review recent progress in the design of OTFTs using hybrid bilayer gate dielectric and discuss key challenges and advantages, which these structures provide to improve the performance of OTFTs. In section 2 various performance indices and factors which influence them are presented.

2. Performance parameters of an OTFT

Three main parameters that characterize the performance of an OTFT are operating voltage, subthreshold swing (SS) and the current modulation ratio (I_{ON}/I_{OFF}). Operating voltage is dependent on threshold voltage (V_T) of the OTFT. Smaller the threshold voltage, lower is the operating voltage. The definition of threshold voltage is not so evident in the case of OTFTs, because, unlike inorganic metal–oxide–semiconductor field-effect transistors (MOSFETs) which operate in inversion mode, OTFTs operate in accumulation mode [30]. In the case of inorganic MOSFETs, the gate–source potential (V_{GS}) at which the channel enters strong inversion is defined as the threshold voltage of a device. An OTFT on the other hand is an accumulation mode device and never enters inversion. Therefore, it is inappropriate to define threshold voltage in the case of OTFTs on the lines of MOSFETs [31]. Quite often, another parameter called switch on voltage (V_{SO}), the voltage at which the flat band conditions are achieved, is used instead of threshold voltage [32]. SS is a measure of how fast an OTFT can turn on or turn off. It is expressed in V per decade and is measured from the slope of $\log(I_D)$ vs. V_{GS} . SS is an important parameter for determining the OTFT application in high frequency switching circuits. The current modulation ratio is the ratio of I_{ON} to I_{OFF} which is largely dependent on the off state current of the OTFT. All these parameters are dependent upon the gate dielectric material and can be improved significantly by choosing a proper dielectric layer. The following sub-sections explain in detail the impact of gate dielectric on each of these parameters.

2.1 Impact of gate dielectric on threshold voltage

Understanding the definition of threshold voltage can actually help to decipher the role of gate dielectric in improving it. An OTFT is a normally off device, which means that ideally, under no bias condition ($V_{GS} = 0$) no current flows through the device. If the conduction begins upon making V_{GS} more positive, then the device is called an n-type OTFT, while, if it conducts when V_{GS} becomes more negative it is called a p-type OTFT. Unlike the inorganic MOSFETs where the channel

region is doped, the active layer in the OTFT is un-doped. In an inorganic MOSFET, the gate–source potential for which the thin channel layer adjacent to the gate dielectric layer inverts its nature is referred to as threshold voltage. However, using the same definition for an OTFT similar to that of a MOSFET is not justifiable. OTFTs operate in accumulation mode and the threshold voltage should account for several physical phenomena occurring at the dielectric–semiconductor interface. One such expression is presented in equation (3). Extraction of V_T from I – V characteristics is another challenge. A usual approach reported in many research works is to extract threshold voltage from the plot of $\sqrt{I_D}$ vs. V_{GS} . The $\sqrt{I_D}$ curve is extrapolated till it cuts the voltage (V_{GS}) axis. The intercept on the voltage axis is treated as V_T . This method is a gross approximation and assumes constant mobility. While, field effect mobility is a function of V_{GS} [33]. Extraction of threshold voltage from the I_D – V_{GS} curves is a challenge, and is investigated by many research groups [31,34–36]. Threshold voltage of an OTFT is presented in equation (3):

$$V_T = \Phi_{MS} + \frac{Q_{ch}}{C_i} + \frac{Q_{it}}{C_i} \quad (3)$$

where Φ_{MS} is the work function difference between the gate metal and semiconductor, Q_{ch} is the areal charge density of the charge carriers in the channel region, Q_{it} is the interface trap density per unit area and C_i is the per unit area capacitance of gate dielectric. Threshold voltage must account for three components: first, work function difference between the gate electrode and semiconductor, second, charge accumulated at the dielectric–semiconductor interface and third, interface traps present in the dielectric layer. Work function difference is an intrinsic property of the work functions of the gate material and OSC. While, the remaining two terms are strongly dependent on C_i . Increasing C_i can significantly reduce the contribution of these terms. Interface trap density Q_{it} is a strong function of the dielectric–semiconductor interface. Hence, by choosing a proper dielectric material and tailoring its surface properties like surface roughness, surface energy and functional groups, interface trap density can be reduced considerably [37].

2.2 Impact of gate dielectric on SS

SS is a measure of how fast the OTFT can switch from the on state to off state, i.e., how fast the drain current decreases/increases with gate voltage. SS can be obtained from the slope of the $\log(I_D)$ – V_{GS} plot using the expression in equation (4):

$$SS = \left[\frac{\partial(\log I_D)}{\partial V_{GS}} \right]^{-1} \quad (4)$$

It also depends on various other parameters. This can also be expressed as below [38]:

$$SS = \frac{kT \ln 10}{e} \left[1 + \frac{e}{C_i} \left(\sqrt{\varepsilon_s N_{bulk}} + e N_{int} \right) \right] \quad (5)$$

where e is the charge of an electron, k the Boltzmann constant, T the absolute temperature, ε_s the dielectric constant of the OSC, C_i the capacitance per unit area of the gate dielectric, N_{bulk} the areal density of the bulk traps and N_{int} is the areal density of the interface traps.

Equation (5) can also be written as

$$SS = \frac{kT \ln 10}{e} \left[1 + \frac{e^2}{C_i} N^* \right], \quad (6)$$

where N^* denotes the contribution of both bulk traps and interface traps per unit area and per unit energy. From equation (6), it can be observed that increasing the value of C_i can reduce the value of SS. It is reported that SS of an OTFT can be improved significantly by tailoring the surface of gate dielectric, which reduces the trap states [16,39–42].

2.3 Impact of gate dielectric on the current modulation ratio

The ratio of I_{ON} to I_{OFF} in an OTFT is referred to as the current modulation ratio. It is a very critical performance parameter for low power circuit applications. A large current modulation ratio ($>10^6$) is desired. In general, a negligibly small current is expected from an OTFT in the off state while a large current is expected in the on state. Therefore, the current modulation ratio is expected to be as large as possible. Due to poor field effect mobility in OSCs, I_{ON} cannot increase significantly [43–45]. As a result, improvement in the current modulation ratio is often achieved by lowering I_{OFF} . An additional requirement which necessitates a low I_{OFF} is, to minimize standby power consumption and to increase charge retention time in organic memories [46]. I_{OFF} is a result of leakage current from all three terminals: drain, source and gate. The leakage current from these terminals can be due to several reasons like structural defects in the gate dielectric layer like pin holes, defect states and trapped charges in the gate dielectric layer, fringe field at the drain/source electrode overlap region and tunnelling of charge carriers through the gate dielectric [47–49]. Proper choice of the dielectric layer can improve the current modulation ratio too. A smooth, low-surface energy dielectric can increase I_{ON} . While, uniform, thick gate dielectric layer free from defects and structural inhomogeneity can reduce gate leakage current and hence, can improve the current modulation ratio.

2.4 Impact of gate dielectric on the reliability of OTFT

Reliability is by far the most challenging aspect of OTFTs. Hysteresis, V_T shift, temperature and bias stress effects

Figure 2. Hysteresis in OTFTs and measuring hysteresis width.

Table 1. Impact of gate dielectric on the performance parameters of OTFT.

Sl. no.	Performance parameter	Desired characteristics of gate dielectric to improve the performance parameter
1	Threshold voltage (V_T)	Large value of C_i , smooth gate dielectric surface
2	SS	Large value of C_i , less interface trap density
3	Current modulation ratio	Uniform thick gate dielectric layer, large energy band gap, smooth gate dielectric surface
4	Reliability	Non-polar gate dielectrics, uniform thick gate dielectric layer

(BSEs) remain as a hurdle for commercialization of OTFTs. Hysteresis refers to the shift in the I_D – V_{GS} curves when V_{GS} is swept in opposite directions as shown in figure 2.

Hysteresis is quantified in terms of hysteresis width, which refers to the difference in the V_{GS} for the same current, during forward and reverse V_{GS} sweeps. Ideally, hysteresis should be zero. Hysteresis is strongly dependent on the nature of gate dielectric [50–53]. Especially, properties like surface roughness, functional groups and thickness of dielectric layer play a crucial role in determining the hysteresis width. In the case of rough dielectrics, interface trap density increases. As a result, more charges get trapped resulting in a large hysteresis width [54]. Nature of functional groups can influence the hysteresis width in the case of polymer dielectrics [52,55,56]. Noh *et al* have reported that moisture is the root cause of hysteresis in polymer dielectric OTFTs and suggested that, by suitably drying the polymer dielectric layer before the deposition of OSCs can eliminate hysteresis [52]. Lee *et al* demonstrated the impact of hydroxyl groups on hysteresis and demonstrated that hysteresis can be eliminated by reducing the hydroxyl group concentration [56]. Thin dielectric films suffer from poor uniformity which creates non-uniform vertical

electric fields that lead to non-uniform carrier trapping and V_T shift.

Table 1 summarizes desirable characteristics of gate dielectric to improve the performance of OTFTs. One common conclusion that can be made by observation is: a high value of C_i is desirable. From equation (2), it is clear that the C_i value can be increased either by scaling down the thickness of an insulator layer or by increasing the dielectric constant. Scaling down the thickness of a dielectric layer is not preferred because, thin films suffer from poor uniformity, structural defects, early dielectric breakdown and thickness variation in the film from run to run.

To increase the value of C_i while avoiding the problems due to thin dielectric layers is a challenge. Various approaches to realize gate dielectric are available in the literature [57–59]. High- k inorganic materials, organic dielectric materials, surface modified high- k inorganic materials, bilayer dielectrics composed of low- k polymer on a high- k inorganic dielectric and nanocomposites are the various possible alternatives. Section 3 discusses these methods, their advantages and limitations in detail. Figure 3 shows the classification of gate dielectric materials used in OTFTs.

Figure 3. Classification of gate dielectric materials used in OTFTs.

3. Materials for gate dielectrics

3.1 High-*k* inorganic dielectric materials

Materials with dielectric constant greater than that of silicon nitride ($\epsilon_r \sim 7$) are referred to as high-*k* materials, while those with dielectric constant less than silicon dioxide ($\epsilon_r \sim 3.9$) are referred to as low-*k* dielectrics [60]. Use of high-*k* dielectric materials for performance improvement is inherited from complementary metal–oxide–semiconductor (CMOS) technology. In CMOS technology, high-*k* dielectrics are used to address the scaling issues, especially leakage current in short channel MOSFETs. Choosing a proper high-*k* dielectric with high energy-band gap (E_G) can reduce gate leakage current considerably. Use of high-*k* dielectrics for performance improvement is also observed in the case of oxide TFTs and poly-Si TFTs. The same idea can be extended for OTFTs too. A good number of research groups have explored the possibility of performance improvement in OTFTs through the use of high-*k* inorganic dielectrics like SiN_x [61,62], Al_2O_3 [63,64], HfO_2 [65], BaTiO_3 [66], ZrO_2 [67], Ta_2O_5 [68] and TiO_2 [69]. These dielectric materials are well studied and hence can be readily adapted for use in OTFTs. Through techniques like RF sputtering, anodization, atomic layer deposition (ALD) and pulsed laser deposition (PLD) they can be deposited with good control over thickness at room temperature and hence compliant with the low-temperature paradigm of OTFTs. However, these materials suffer from two major drawbacks. First, reduction in mobility with an increase in dielectric constant and second, high-surface energy, which reduce the mobility further. High-*k* inorganic dielectrics often induce broadening of density of states (DoS) near the Fermi level in OSCs [70]. This reduces hopping probability of the carriers and reduces the field effect mobility. It is also observed that the dielectric constant and mobility of charge carriers in OTFTs are inversely related. This can be due to a local polarization effect [71]. Veres *et al* proposed that in an OTFT, the presence of random dipole at the semiconductor–dielectric interface can actually increase the energy disorder and reduce the field effect mobility [72]. Another major challenge with inorganic dielectrics is their high-surface energy. Low-surface energy dielectrics are desirable for deposition of OSCs, because low-surface

energy allows an OSC material to spread along the surface of dielectric. This uniform distribution facilitates the growth of grains in lateral directions too, hence filling the vacant spaces between grains. This leads to tightly packed and well interconnected grains. Hence, mobility increases when an OSC is deposited on the low-surface energy dielectric [73].

3.2 Organic dielectric materials

Organic (polymer) dielectric materials have the potential to be a viable alternative for truly flexible applications. They offer several advantages over high-*k* inorganic dielectrics. Unlike inorganic dielectrics which need high vacuum and high-temperature processes for deposition, organic dielectrics can be deposited by solution processing techniques such as spin coating, dip coating and inkjet printing [74]. These processes are compatible with OSCs and can help in realizing top-gate structures [57]. Polymer dielectric is a well-researched and established area. The chemical and physical properties of polymer dielectrics are well studied and hence, they can be readily adapted for OTFTs. The properties of polymer dielectrics can be tuned by changing the monomer structures and polymerization conditions [59].

Organic dielectrics offer two major advantages over inorganic counterparts. They are characterized by a smooth surface and low-surface energy. Their surface roughness (RMS) is usually of a few nanometres [70,75–77]. Because of its smooth surface, an OSC layer deposited is free from discontinuities. In addition to low-surface roughness, organic dielectrics also have low-surface energy. A low-surface energy dielectric layer improves the microstructure and morphology of the OSC. As a result, improvement in mobility and reduction in operating voltages can be observed in polymer dielectric-based OTFTs. However, the phenomena causing a reduction in operating voltage are different from that of high-*k* inorganic materials. In high-*k* materials, reduction in operating voltage is achieved by increasing C_i . Increasing C_i can accumulate more charge carriers in the channel region even at small values of V_{GS} . These charge carriers fill the interface traps at lower values of V_{GS} and hence the threshold voltage and operating voltage are lowered. Polymer dielectrics have low-*k* and the operation voltage reduction is not obtained by increasing C_i but, by making a clean interface and reducing interface traps [72]. Even, I_{ON} obtained in low-*k* polymer-based OTFTs is comparable with high-*k* counterparts, because a linear decrement in the gate capacitance is compensated by exponential increment in mobility [72].

In spite of these advantages, organic dielectrics have some drawbacks. The dielectric constant is quite low and to obtain a large C_i , the gate dielectric layer needs to be thin. But, thin films suffer from poor uniformity, early dielectric breakdown and pinholes. In addition to this, hysteresis effects in I – V characteristics is also reported in polymer dielectric-based OTFTs [52,78]. Thus, polymer dielectrics also fail to fulfil all the characteristics required for an ideal dielectric in OTFTs.

Table 2. Comparison of inorganic and organic dielectrics.

Property	Inorganic dielectrics	Organic dielectrics	Desired aspect of a gate dielectric material
Dielectric constant	High- k (>7.2)	Low- k (<3.9)	Higher- k is desired
Deposition techniques	Vacuum deposition techniques	Solution processing	Solution processing
Temperature	Ranges from 200 to 500°C which is necessary for annealing	Ranges from 100 to 300°C, which is determined by curing temperature	Low temperature
Impact on threshold voltage	Clean interfaces, lower and stable V_T	Variable V_T due to interface states	Stable V_T
Impact on mobility	Surface energy mismatch between the dielectric material and OSC leads to poor mobility	Surface energy matching between the OSC and dielectric enhances the mobility	High mobility
Impact on current modulation ratio (I_{ON}/I_{OFF})	No structural defects and has good dielectric strength and hence large current modulation ratio	Structural defects are common in thin layers and tend to increase I_{OFF} thereby reducing current modulation ratio	Large current modulation ratio
Impact on reliability	Hysteresis is rarely observed	Hysteresis is common	No hysteresis

Table 2 summarizes the capabilities and limitations of inorganic and organic dielectrics. From the table, it can be clearly observed that it is almost impossible to find a single such dielectric material that satisfies all the criteria necessary to improve the performance of an OTFT. Therefore, an alternate approach which uses a combination of two or more materials is investigated and discussed below.

4. Self-assembled monolayer (SAM)-based OTFTs

Low voltage OTFTs are made possible by high capacitance and low leakage gate dielectrics. High- k inorganic dielectrics offer both these properties but their surface properties remain a concern. Therefore, one approach to improve performance of OTFTs using inorganic high- k dielectrics is by modifying surface properties of high- k material. This surface modification is attained by inserting a thin layer referred to as a SAM between the dielectric and semiconductor. A schematic of a SAM-based BGTC OTFT is shown in figure 4. SAMs are ultrathin, supramolecular layers which are formed by spontaneous adsorption of an active molecular precursor onto a solid surface [79]. A SAM can be deposited by solution processing techniques, hence suits the low temperature, low cost conditions demanded by organic electronics. In addition, the process of self-assembly favours large area coverage, substrate selectivity and produce densely packed layers [80].

In an OTFT, it is reported that, charge carrier conduction happens only in the first few monolayers of the active layer and is largely dependent on the nature of the dielectric–semiconductor interface [14]. The surfaces of inorganic high- k dielectrics have dangling bonds, which acts as trapping sites for charge carriers [57,81,82]. Charge carriers

Figure 4. SAM-based BGTC structure.

get trapped in these trap sites as they move along the channel from the source to drain. As a result, mobility reduces. In addition, the trapping and de-trapping of carriers introduces hysteresis in the I – V characteristics by causing a V_T shift [57]. Modification of the surface of the dielectric layer using a SAM results in a smooth surface with low-surface energy. Deposition of OSC on such smooth low-surface energy surfaces improves the morphology and microstructure of the semiconductor film which results in improved mobility. SAM, if deposited over a dielectric layer can also help to reduce the gate leakage current [83].

There are a wide variety of polymers available to form a SAM [79]. The choice of SAM material depends on the nature of the surface on which it is to be deposited. Organosilane-based SAMs such as hexamethyldisilazane (HMDS) [84] and octyltrichlorosilane (OTS) [85] are preferred because of their high stability and physical robustness [86]. Silane-based SAMs can be deposited easily on hydroxylated surfaces. Technologically relevant dielectrics such as SiO_2 , AlO_x , HfO_x etc. are rich in hydroxyl groups and provide an ideal surface for deposition of silane-based SAMs. However, silane-based

SAMs cannot be used on polymer gate dielectrics because they have comparatively less hydroxyl groups on its surface [86,87]. Another set of SAMs quite often used with metal oxide surfaces is *n*-alkanoic acids and phosphonic acid (PA) [79]. As reported by Acton *et al* [87], PA-based SAMs are thermally stable even at higher temperatures (400–450°C) and offer several advantages over silane-based SAMs like higher resistance to moisture, less probable homo-condensation and the deposition of PA on metal oxide is independent of surface hydroxyl concentration [88]. Table 3 summarizes the list of various SAM/dielectric material combinations and the performance parameters of OTFTs fabricated using them.

4.1 Threshold voltage shift

Threshold voltage shift in SAM-based OTFTs has been reported by many groups [85,89–91]. Pernstich *et al* [85] investigated the V_T shift in organosilane-based SAMs on SiO₂ gate dielectrics in both single crystal and polycrystalline OTFTs based on rubrene and pentacene, respectively. It was concluded that the V_T shift is a function of organosilane forming the SAM and is independent of the film morphology [85]. The study leads to a conclusion that the V_T shift is a result of electron acceptor tendency in the SAM. Electrons get attracted by the SAM, leaving behind mobile holes in the channel. This necessitates more positive gate voltage to turn off the device, which leads to a shift in V_T . The charge distribution in the SAM molecules is influenced by the electronegativity of its functional group. An electric dipole is created in the SAM as a result of the charge distribution. The dipole alters the surface potential near the channel region and hence the threshold voltage. The relation between the threshold voltage shift (ΔV_T) due to SAM is given as [89,92]

$$\Delta V_T(\text{SAM}) \approx \frac{Q_{\text{SAM}}}{C_i} = \frac{C_{\text{SAM}}}{C_i} V_{\text{SAM}} \quad (7)$$

$$C_i = \frac{C_{\text{ox}} C_{\text{SAM}}}{C_{\text{ox}} + C_{\text{SAM}}} \quad (8)$$

$$V_{\text{SAM}} = \frac{N_{\text{SAM}} P_z}{\epsilon_0 \epsilon_{\text{SAM}}}, \quad (9)$$

where C_{ox} is the per unit area capacitance of the oxide layer, C_{SAM} is the per unit area capacitance of the SAM layer, N_{SAM} is the areal packing density of the SAM layer, ϵ_0 and ϵ_{SAM} are the permittivity of free space and relative permittivity of the SAM respectively and P_z is the dipole momentum perpendicular to the interface. This relation however ignores the impact of residual charges and trapped charges in the dielectric layer due to the polarized SAM.

5. High-*k*/low-*k* bilayer-based OTFTs

Since, the surface of low-*k* polymer dielectrics offers favourable conditions for deposition of OSC layers, it is

advisable to use such a layer just beneath the surface of the semiconductor. However, due to their poor dielectric constant they need to be thin for reducing the operating voltage. Thin polymer layers suffer from structural inhomogeneities like pinholes, non-uniformity and tend to be leaky. Therefore, by applying a thin layer of low-*k* polymer dielectrics on the top of high-*k* inorganic dielectrics can improve the overall performance of the OTFT. Various methods have been proposed in past by researchers to improve the OTFT performance by this bilayer approach.

Deman *et al* [81] modified the surface of Ta₂O₅ by a thin layer of polymethylmethacrylate (PMMA) for performance improvement of an OTFT. Annealing of Ta₂O₅ improves its microstructure and hence dielectric performance. Thicker PMMA needs long duration annealing which may not be feasible in OTFTs. If not annealed properly the traces of solvents in PMMA will increase the leakage current. Seo *et al* [93] have used a polyvinyl alcohol (PVA) layer above the polyvinyl-phenol (PVP) layer to reduce the surface roughness and increase the grain size of pentacene. The average grain size has increased from 400 to 1500 nm for bare PVP and PVA-coated PVP. Seol *et al* [48] used a multilayer gate dielectric for reducing gate leakage current in OTFTs. A thin layer (10 nm) of HfO₂ deposited by ALD is inserted between the spin-coated PVP layers. However, the thin layer of HfO₂ did not impact the mechanical flexibility. It is reported that by increasing the thickness of the PVP layer above the HfO₂ the strain on HfO₂ can be made zero.

Wang *et al* [94] demonstrated solution processed HfO_x-based pentacene OTFTs. A thin layer of polystyrene (PS) is used as a coating over the HfO_x. It is reported that the annealing of PS/HfO₂ bilayer gate dielectrics can improve the OTFT performance. This is because annealing reduces the surface energy of the dielectric layer and helps for a better growth of pentacene. Large grain size, high crystallinity and better connectivity between the grains are observed in pentacene grown on the annealed PS layers. Lu *et al* [69] have demonstrated a low cost, simple technique of layer-by-layer deposition (LbL) deposition of TiO₂, which can be employed for large area applications, with good repeatability. The thickness control in the LbL technique is easily achieved by choosing the number of depositions. A non-polar dielectric PS is used on the top of high-*k* inorganic dielectric layer TiO₂ for performance improvement of the OTFT. It is also reported that a brief temperature treatment of the TiO₂ layer improves the overall performance. Huang *et al* [53] improved the reliability of a HfO₂-based BGTC pentacene OTFT by modifying the dielectric surface. The root cause of hysteresis observed in OTFTs is the hydroxyl (–OH) groups present on the dielectric semiconductor interface. The impact of these groups on hysteresis is reported in this work. A systematic study was performed by measuring the hysteresis width, when the HfO₂ surface is treated with (–OH)-rich PVP and PS, which is known to reduce the hydroxyl concentration on the dielectric surface. The overall performance of the OTFT has improved by using a PS/HfO₂-based bilayer as a gate dielectric.

Table 3. A summary of SAM-based OTFTs and their performance parameters.

OSC	Inorganic high- <i>k</i>	SAM	V_T (V)	Mobility ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	SS (V per decade)	$I_{\text{ON}}/I_{\text{OFF}}$	Ref.
Pentacene	SiO ₂	None	-9.4	1	1.6	$\sim 10^6$	[107]
Pentacene	Al ₂ O ₃	None	-6	1.1	0.9	$\sim 10^6$	
Pentacene	Al ₂ O ₃	Alkylphosphonic acid	-2.1 to -5	0.4-2.1	2.3-5.1	10^5-10^6	
Pentacene	SiO ₂	Trichlorosilane	-4.3 to 2.8	0.15-0.96	0.9-2	NR	[85]
Pentacene	ZrO ₂	None	NR	0.12	NR	10^4	[83]
Pentacene	ZrO ₂	Octadecyltrimethoxysilane (OTMS)	NR	0.66	NR	10^5	
Pentacene	SiO ₂	None	13	0.3-0.8	1.5-1.7	10^{12}	[108]
Pentacene	SiO ₂	Phosphonate-linked anthracene	NR	0.3-0.8	NR	10^{11}	
Pentacene	AlO _x	None	-1.7	0.3	0.2	10^4	[87]
Pentacene	AlO _x	Phosphonic acid	-1.3 to -1.5	0.14-0.3	0.09-0.11	10^5	
Pentacene	AlO _x	Phosphonic acid	NR	0.15-0.28	NR	10^5-10^6	[109]
Pentacene	HfO _x	None	-0.75	0.2	0.13	10^5	[88]
Pentacene	HfO _x	Phosphonic acid	-0.5	0.32	0.1	10^5	
TIPS pentacene	HfO _x	Phosphonic acid	-0.5 to -0.6	0.11-0.38	0.13-0.2	10^3-10^5	
Pentacene	SiO ₂	None	NR	0.08	0.42	NR	[110]
Pentacene	SiO ₂	Trimethylsiloxane	NR	0.26-1.03	0.2-0.31	10^5	
Pentacene	HfO ₂	None	-1.18	0.28	0.15	10^5	[111]
Pentacene	HfO ₂	Phosphonic acid	-0.56 to -0.88	1.1-1.5	0.11	10^6	
Pentacene	SiO ₂	None	-7.08	0.25	NR	10^6	[84]
Pentacene	SiO ₂	Disilazane	-10.8 to -11.7	0.42	NR	10^6	
Diketopyrrolopyrrole (DPP)	AlO _x	Octadecylphosphonic acid (ODPA)	NR	0.324	NR	200	[112]
DNTT	Al ₂ O ₃	ODPA	-0.4 to -0.9	NR	NR	NR	[89]
Pentacene	pV3D3	None	-1.5	0.33	0.46	10^3	[40]
Pentacene	pV3D3	HMDS	-0.9	0.59	0.21	10^4	
Pentacene	pV3D3	OTS	-0.2	0.31	0.35	10^5	

Table 3. (continued)

OSC	Inorganic high- <i>k</i>	SAM	V_T (V)	Mobility ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	SS (V per decade)	$I_{\text{ON}}/I_{\text{OFF}}$	Ref.
Pentacene	pV3D3	PFTS	1.1	0.44	0.64	10^4	
DNTT	AlO_x	Phosphonic acid	NR	2–2.7	0.1	NR	[18]
DPh-DNTT	AlO_x	Phosphonic acid	NR	1.6–3.7	0.1–0.16	NR	
C10-DNTT	AlO_x	Phosphonic acid	NR	0.9–3.1	0.14–0.17	NR	
N1100	AlO_x	Phosphonic acid	NR	0.3–0.4	0.17–0.18	NR	
Pentacene	Ta_2O_5	None	3.1	1.8	NR	10^{12}	[113]
Pentacene	Ta_2O_5	OTS	3.8	3.5	NR	10^{10}	
Pentacene	HfTiO_x	None	–1.2	0.43	0.21	$3.00 \times 10^{+04}$	[16]
Pentacene	HfTiO_x	Phosphonic acid	–1	1.34	0.14	10^5	
PTCDI-C13	HfTiO_x	Phosphonic acid	1.6	0.72	0.72	10^3	
Pentacene	SiO_2	None	2	1.2	NR	10^6	[114]
Pentacene	SiO_2	OTS	–0.4	0.035	NR	10^5	
Pentacene	SiO_2	HMDS	–1.5	0.025	NR	10^5	
C8-BTBT	SiO_2	None	–5	1.85	NR	10^8	
C8-BTBT	SiO_2	OTS	–5	0.11	NR	10^7	
C8-BTBT	SiO_2	HMDS	–8	1.7	NR	10^8	
PBTTT	PVP	None	–6	0.0042	NR	NR	[86]
PBTTT	PVP	Sodium dodecyl sulphate (SDS)	–4	0.0049	NR	NR	
PBTTT	PVP	Tridecafluorohexane-1-sulphonic acid potassium salt (PFHKS)	–2	0.0051	NR	NR	
C6-DNT-V	SiO_2	None	1.2	0.7	NR	10^6	[115]
C6-DNT-V	SiO_2	OTS	–2.6	0.28	NR	10^6	
C6-DNT-V	SiO_2	HMDS	–4.8	0.65	NR	10^6	

NR, not reported.

Park *et al* [95] have shown that by using a bilayer structure of CYTOP/Al₂O₃ the threshold voltage shift can be minimized. They fabricated and tested an n-channel OTFT based on *N,N'*-ditridecylperylene-3,4,9,10-tetracarboxylic diimide (PTCDI-C13). A layer of pentacenequinone (PQ) is used above the active layer to reduce the surface trap density. CYTOP-based surface treatment on Al₂O₃ gate dielectric layers has shown superior performance when compared with that of bare Al₂O₃ and HMDS-treated Al₂O₃. Post annealing is necessary to improve the crystallinity of the semiconductor layer. However, post annealing temperature cannot exceed the glass transition temperature (T_g) of the CYTOP layer. CYTOP has a T_g of 110°C and hence does not allow annealing above this temperature. Annealing above the T_g results in intra-domain cracks in the film which degrades the electrical performance of the OTFT. Untreated and HMDS-treated Al₂O₃ OTFTs result in a V_T shift of 6 V while CYTOP-coated Al₂O₃ results in a V_T shift of 0.5 V. PQ-passivated OTFTs showed better performance under bias stress, V_T shift in these devices is lower in comparison with the untreated ones.

Fukuda *et al* [96] have shown that by tuning the thickness of the gate dielectrics in a bilayer threshold voltage shift can be eliminated. Since, the bias stress effects (BSEs) are result of the trapping and de-trapping of the charge carriers near the semiconductor/dielectric interface, surface modification techniques to eliminate them can be employed. Methods like chemical treatment, annealing to eliminate the traps and methods to reduce the surface roughness such as SAM deposition, low- k organic polymer layer can be used to reduce the BSE. The bilayer consists of a layer of parylene-C coated with a fluoropolymer. It is observed that the V_T shifts induced by these dielectric layers, when used individually are in opposite direction. Parylene-C induces a positive shift in V_T while the fluoropolymer induces a negative shift. Therefore, by choosing a proper ratio of their thickness the threshold voltage shift can be nullified and can be maintained constant.

Ha *et al* [51] have reported a solution processed pentacene-based BGBC structure employing high- k ZrO₂ and low- k CYTOP as a bilayer dielectric. The device is processed completely using solution processing techniques only. Due to the chemical modification of the high- k dielectric, the interface trap density induced due to resident water molecules and other aqueous solvents near the interface are reduced from 1.06×10^{13} to $4.13 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. The bilayer OTFTs operated without any hysteresis under both dark and illuminated conditions.

Held *et al* [97] reported low-temperature bottom contact top gate (BCTG) structures using ALD of HfO_x and PMMA bilayer as gate dielectrics. If only a single layer of PMMA is used as a dielectric it needs to be at least 400 nm thick to avoid pinholes. However, by using a thin layer (10 nm) of PMMA above HfO_x operating voltage is lowered, trap states reduced, mobility and stability under bias stress are improved.

Sun *et al* [98] have shown that the life-time of OTFTs can be improved by using a bilayer gate dielectric. The low- k polymer used above the SiO₂ layer in this structure reduces

the hydroxyl groups at the surface and makes the structure impervious to moisture. This increases the life-time of the device. It is also observed that the surface properties of gate dielectric such as hydrophobicity and chemical nature impact the electrical properties of OTFTs rather than film morphology and microstructure. Table 4 summarizes the performance parameters of OTFTs fabricated using various high- k /low- k bilayer gate dielectrics.

6. Nanocomposite-based OTFTs

Stringent conditions necessary for an ideal gate dielectric of OTFTs cannot be met by a single material. Thus, an optimal choice is to club two materials and to obtain desirable characteristics. The gate dielectric materials can be broadly categorized into two groups: inorganic and organic. Inorganic high- k materials, especially metal oxides like Al₂O₃, HfO_x, ZrO₂, TiO₂, Ta₂O₅, BST, BZT etc. require high-temperature processing. But, low cost plastic substrates, the intended material for OTFTs, cannot sustain high temperature. Also they are mechanically rigid and do not support flexible devices. Deposition techniques require high-vacuum conditions which makes their processing expensive. On the other hand, organic dielectrics suffer from low dielectric constant. Therefore to improve C_i , thickness of the insulator layer needs to be reduced. Thin polymer dielectrics are a serious concern for device reliability, due to the presence of pinholes and discontinuities. But, solution processing techniques used for polymer dielectric deposition such as dip coating, spin coating, spray coating, screen printing etc. are attractive due to their low cost and relatively low-temperature processing.

Nanocomposites are a combination of high- k metal-oxide nanoparticles (NPs) dispersed uniformly in a polymer matrix. They are attractive alternative for gate dielectrics in OTFTs. These nanocomposites can be obtained through solution processing techniques, hence offer the advantages of low temperature and low cost. The overall dielectric constant of a nanocomposite is typically greater than the polymer matrix. Hence an increment in C_i and reduction in operating voltage can be achieved. The dielectric constant of nanocomposites can be tuned by adjusting the proportion of metal-oxides NPs in the polymer matrix. The dielectric constant of a nanocomposite layer can be estimated using equation (10), which is commonly referred to as a logarithmic mixing rule [99]:

$$\log(k_{\text{composite}}) = \theta \log(k_{\text{NP}}) + (1 - \theta) \log(k_{\text{polymer-matrix}}) \quad (10)$$

where k_{NP} and $k_{\text{polymer-matrix}}$ are the dielectric constants of the NPs and the polymer matrix respectively and θ is the volume fraction of the NPs in the polymer matrix. The dielectric constant of the NPs can be quite different from its bulk value and the above equation can only be used as a rule of thumb for estimation. Overall, quality of a nanocomposite as

Table 4. A summary of high-*k* inorganic/low-*k* polymer bilayer gate dielectrics in OTFTs.

OSC	High- <i>k</i>	Low- <i>k</i>	V_T (V)	Mobility ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	SS (V per decade)	$I_{\text{ON}}/I_{\text{OFF}}$	Ref.
Pentacene	Ta ₂ O ₅ (no annealing)	None	-0.7	0.035	0.5	67	[81]
Pentacene	Ta ₂ O ₅ (600°C)	None	-0.4	0.03	0.44	170	
Pentacene	Ta ₂ O ₅ (600°C)	PMMA	-3.5 to -4	0.12–0.29	1.04–1.2	10^4 – 10^5	
Pentacene	PVP	None	-4.1	0.023	2.95	NR	[93]
Pentacene	PVP	PVA	-2.9	0.036	1.72	NR	
Pentacene	MgO	None	NR	NR	NR	NR	[37]
Pentacene	MgO	PVP	-2.67	0.66	NR	NR	
Pentacene	None	PVP	-16.3	0.5	NR	10^4	[48]
Pentacene	PVP/HfO ₂	PVP	-5.9	0.16	0.6	10^5	
Pentacene	TiO ₂	None	-0.7	0.001	0.309	10^2	[69]
Pentacene	None	PS	-1.7	0.007	0.413	10^4	
Pentacene	TiO ₂	PS	-1.4	0.2	0.22	10^4	
Pentacene	TiO ₂ (annealed)	PS	-1.5	0.31	0.178	10^7	
Pentacene	HfO _x	None	-1	0.2	0.25	10^3	[94]
Pentacene	HfO _x	PS	-1.5	0.4–1	0.1	10^6	
Pentacene	HfO _x	None	3.2	0.13	1.73	10^3	[53]
Pentacene	HfO _x	PVP	7.7	0.05	54.5	1	
Pentacene	HfO _x	PVP+PS	-2.2	0.24	0.34	10^5	
Pentacene	HfLaO	None	-0.7	0.08	0.13	NR	[116]
Pentacene	HfLaO	PVP	-0.5	0.34	0.9	NR	
Pentacene	Parylene-C	None	-17.5	0.13	NR	NR	[96]
Pentacene	Parylene-C	Teflon	-21.3 to -24.1	0.2–0.3	NR	NR	
IDTBT	<i>p</i> (VDF-TrFE-CFE)	None	-1.52	0.3	0.152	10^5	[13]
IDTBT	<i>p</i> (VDF-TrFE-CFE)	CYTOP	-1.66	1.4	0.158	10^6	
TIPS-pentacene	BaTiO ₃	PMMA	-4.8	0.014	8.3	10^4	[117]
TIPS-pentacene	BaTiO ₃	PMMA	5.3	0.073	3.8	3.1×10^4	
Pentacene	K-PSPI-6F	PVA	-2.2	0.2	0.21	10^5	[118]
C8-BTBT	K-PSPI-6F	PVA	-3.4	0.88	0.2	10^5	
Pentacene	SiO ₂	None	2	0.12	NR	10^6	[119]
Pentacene	SiO ₂	Polyimide (PI)	-0.4	0.012	NR	10^5	
Pentacene	SiO ₂	PMMA	-1	0.004	NR	10^5	
Pentacene	SiO ₂	CYTOP	-8.6	8.5×10^{-4}	NR	10^3	
C6DNT	SiO ₂	None	1.2	0.7	NR	10^6	
C6DNT	SiO ₂	PI	-4.3	1.2	NR	10^6	
C6DNT	SiO ₂	PMMA	-5.3	0.5	NR	10^6	
C6DNT	SiO ₂	CYTOP	-9.8	0.17	NR	10^6	
Pentacene	SiO ₂	None	-12	0.19	8.1	10^5	[98]
Pentacene	SiO ₂	HMDS	-19.7	0.35	4.3	10^5	

Table 4. (continued)

OSC	High- <i>k</i>	Low- <i>k</i>	V_T (V)	Mobility ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	SS (V per decade)	I_{ON}/I_{OFF}	Ref.
Pentacene	SiO ₂	PMMA	-24.1	0.51	4	10^5	[67]
Pentacene	SiO ₂	PS	-15.3	0.97	3.2	10^5	
Pentacene	ZrO ₂	None	-0.73	0.02	NR	1.9×10^4	
Pentacene	ZrO ₂	HMDs	-0.47	0.07	NR	7.2×10^4	
Pentacene	ZrO ₂	PMS	-0.36	0.51	0.26	1.2×10^5	[120]
Pentacene	Si ₃ N ₄	None	-22.7	8.9×10^{-5}	NR	200	
Pentacene	None	PMMA	-10.2	0.2	NR	1.5×10^7	
Pentacene	Si ₃ N ₄	PMMA	-4.9	0.23	NR	2.8×10^7	

NR, not reported.

Figure 5. Nanocomposite dielectric-based BGTC structure OTFT.

a gate dielectric material largely depends upon the uniformity with which NPs are dispersed in the polymer matrix. Uneven distributed NPs can increase the surface roughness of a gate dielectric which reduces the mobility due to surface scattering. Gate dielectric surface roughness also impacts the microstructure and morphology of the OSC deposited over it. Smooth surface is necessary to ensure dendritic growth of the semiconductor material with tightly packed grains. Therefore, an optimum value of volume fraction needs to be chosen to maintain a smooth surface while maintaining high-dielectric constants. It has been reported that increasing the volume fraction of NPs in a polymer matrix also leads to an increase in the gate-leakage current [99–103]. This may be due to the inhomogeneity created in nanocomposites due to large concentration of NPs.

To solve the problem of leakage current and to improve surface quality of nanocomposite dielectrics, a thin polymer dielectric layer (<50 nm) is deposited over a nanocomposite dielectric layer [104–106] as shown in figure 5. This layer acts as a passivation layer. Since it is thin, its impact on the dielectric constant is minimum. The passivation layer also helps in improving the morphology of OSCs. Table 5 lists the various nanocomposite-based dielectrics and their impact on the performance parameters of OTFTs.

7. Future directions

Though various techniques have been explored for improving OTFT performance by modifying gate dielectric, few challenges still exist. A conclusion that can be drawn from the above study is that a single material may not satisfy all the characteristics necessary for an ideal gate dielectric in OTFTs. Therefore, one needs to come up with a suitable combination of two or more materials to realize a good gate dielectric layer in OTFTs. However, the choice of materials, their deposition techniques could be an interesting material design challenge. Given the long list of polymer dielectrics and inorganic materials, it would be desirable to formulate a set of rules for choosing compatible materials from the catalogue. For this,

Table 5. A summary of nanocomposite-based gate dielectric OTFTs.

OSC	Polymer matrix	Nanocomposite	Mobility ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	V_T (V)	I_{ON}/I_{OFF}	Ref.
Pentacene	PVP	TiO ₂	0.2–0.25	–7 to –7.8	$10^3 - 10^4$	[101]
Pentacene	PS	TiO ₂	0.18	–2	535	[121]
Pentacene	PVP	TiO ₂	0.39–0.42	–5.2	$1 \times 10^3 - 5 \times 10^4$	[106]
Pentacene	PVP + P (α -MS)	TiO ₂ (15 wt%)	0.41	–3	3×10^4	[122]
Pentacene	Polyvinyl acetate (PVAc)	Organoclay	NR	–14.7	$10^{2.5}$	[105]
Pentacene	PVAc	No filler	NR	–13.7	10^4	[105]
Pentacene	Nylon-6	TiO ₂	0.1	–5	10^3	[105]
Pentacene	Nylon-6+PVP	TiO ₂	0.7	–5	10^4	[105]
Pentacene	P (α -MS)	ZrO ₂	NR	–1.1	10^6	[123]
Pentacene	P (α -MS)	ZrO ₂	1	NR	10^6	[124]
F16-CuPc	P (α -MS)	ZrO ₂	0.015	NR	10^3	[125]
Pentacene	PI	TiO ₂	0.15	–8	10^5	[125]
Pentacene	PVP	TiO ₂ (4 vol%)	0.51	–7.5	1.07×10^2	[99]
Pentacene	PI	TiO ₂ (4 vol%)	0.61	–7.7	1.05×10^2	[126]
Pentacene	PMMA-co-MMA	TiO ₂ (1 wt%)	0.48–0.53	–13.9 to –16.8	10^5	[126]
Pentacene	P (α -MS)	Barium strontium titanate (BST) (parylene-c)	NR	0.25	NR	[127]
Pentacene	P (α -MS)	BaTiO ₃ (parylene-c)	NR	0.35	NR	[128]
P3HT	PVP+crosslinking agent PMMF	TiO ₂	0.006	3.4	6.5×10^5	[128]
P3HT	PVP+PMF+PMMA	No filler	0.002	2.48	1.5×10^4	[128]
P3HT	PVP+PMF	TiO ₂	1.1×10^{-3}	0.41	5.7×10^2	[129]
P3HT	SU-8	BaTiO ₃	3.4×10^{-3}	–1.7	10^3	[129]
P3HT	SU-8	No filler	4.9×10^{-3}	–5	10^3	[129]
Pentacene	PVP	TiO ₂ (3 wt%)	0.147	–0.24 to –0.39	100–300	[100]
P3HT	Cyanoethyl pullulan (CYLEP)	ZrO ₂	0.04–0.08	–1 to –1.8	600–1200	[130]
Pentacene	PI	BaTiO ₃	0.02–0.06	–3.0 to –4.1	10^5	[131]
Pentacene+P (α -MS)	P(VDF-HFP)+PVP	BST	0.06	–0.55	10^3	[104]
Pentacene+P (α -MS)	P(VDF-HFP)+PVP	Barium zirconate	0.08	–0.85	10^3	[104]
PDPPTT	P(VDF-HFP)+PVP	BST	0.14	–0.5	10^3	[104]
TIPS-pentacene	P(VDF-TrFE)+PMMA	No filler	0.02	–16	10^4	[102]
TIPS-pentacene	P(VDF-TrFE)+PMMA	BaTiO ₃ (9 wt%)	0.01–0.004	–15	10^4	[102]
Pentacene	PI	HfO ₂	NR	–3.8	NR	[103]
Pentacene	PI	ZrO ₂	NR	–2.87	NR	[103]
Pentacene	PI	HfO ₂ + ZrO ₂	NR	–0.71	2.42×10^4	[103]
Pentacene	PI	HfO ₂ + ZrO ₂	NR	–0.69	NR	[103]

chemical, mechanical and thermal properties of these materials need to be closely examined. Choosing a proper deposition technique from various techniques like evaporation, spin coating, spray coating, dip coating, iCVD, sputtering etc. is also a crucial aspect in determining both the budget as well as performance of OTFTs. Once the materials and their deposition techniques are selected, optimizing device structure, which includes thickness of the layer, annealing temperature and time, surface modifications, volume or weight fraction in the case of nanocomposites is to be explored. A unique feature of organic electronics, that is availability of wide variety of semiconductor materials, adds another dimension to these challenges.

Inorganic high- k dielectrics though appear promising because of their high-dielectric constant and low-leakage current their high-surface energy remains a serious concern. In the recent past, a few studies conducted on ceramic oxides by incorporating rare-earth materials have improved the dielectric properties of the material but, could not reduce the surface energy. This issue is important because low-surface energy is critical for improving the crystallinity and microstructure of the OSC and hence increasing the performance of OTFTs. Apart from high-surface energy, another major drawback with inorganic high- k materials is their deposition technique. Traditional techniques like RF sputtering, CVD and anodization require high vacuum. Generation and sustenance of high vacuum need highly sophisticated and expensive equipment increasing the overall budget. Therefore, cost-effective techniques, especially solution processing techniques for depositing inorganic dielectrics need to be developed. Developing solution processing techniques that can produce good quality dielectric films comparable with vacuum-based deposition techniques could be a challenge. Mechanical flexibility is another key attribute in organic electronics. Particularly flexible displays demand flexible OTFTs. Hence sufficient attention should be paid towards improving mechanical flexibility of inorganic dielectrics.

Organic dielectrics appear promising because of their low cost, low-temperature solution processability, mechanical flexibility and low-surface energy. However, their characteristics like poor dielectric constant, large number of interface traps, structural defects and early dielectric breakdown are undesirable. Future studies in organic dielectrics should focus on increasing their dielectric constant, minimizing interface traps and optimizing the deposition conditions. A major concern for organic dielectric-based OTFTs is hysteresis. Elimination of hysteresis by tailoring the surface properties of organic dielectrics and to minimize V_T shift is necessary for fabricating reliable OTFTs.

Surface modification of high- k inorganic dielectrics by an ultrathin polymer layer is another interesting approach. Because, a thin layer covers the inorganic high- k the overall dielectric constant is comparable with high- k materials. Major advantage however, will be with the improvement in surface properties. A smooth, low-surface energy modifier

helps in forming a continuous, densely packed, OSC layer. This enhances the mobility. Despite these advantages, V_T shift remains a serious concern in surface-modified high- k dielectric-based OTFTs. Hybrid bilayers which use a low- k organic dielectric above a high- k inorganic utilize the best properties out of both inorganic and organic materials. High value of dielectric constant of high- k materials and surface properties of organic dielectrics can be best used in this approach. These high- k /low- k bilayers can also address the issue of threshold voltage instability, which can be solved partially by choosing a proper thickness ratio of the two layers. However, the influence of interface between high- k and low- k materials on the device performance needs to be further investigated.

Nanocomposite-based dielectrics are a new addition to the choice of dielectric materials for an OTFT. These materials offer the advantage of tunable dielectric constant by varying the volume fraction of inorganic NPs in a polymer matrix. However, the surface roughness of nanocomposite dielectrics remains an issue. Rougher dielectric surfaces are unfavourable for OSC layer deposition. Leakage current increases in OTFTs which use rough gate dielectrics. Therefore, further investigation on these materials needs to be done to study the long-term device stability issues.

Since, a wide variety of materials can be used as semiconductor layers in OTFTs, optimizing the dielectric layer for each of these materials is a stiff challenge. Obtaining the dielectric properties similar to that of vacuum-deposited dielectric layers through solution processing is another interesting challenge. Due to their multi-disciplinary nature and unconventional transport nature involved OTFTs need further investigation, to improve their reliability, reduce operating voltage and allow mass production.

8. Conclusion

We have summarized the recent progress and practices in the field of gate dielectric materials for performance improvement in OTFTs and have summarized the properties of these materials for improving the performance of OTFTs. Conventional inorganic dielectrics are readily accessible and hence can be used as a test bed for new OSC materials. However, these materials do not support flexibility because inorganic films tend to crack when subjected to bending. Polymer dielectrics are readily accessible and can be deposited by solution processing. However, these films offer lower capacitance which results in high-operating voltage for the corresponding OTFTs. Surface modified layers, especially hybrid dielectric, allow us to preserve both the high capacitance as in the case of an inorganic dielectric and smooth surface with low-surface energy like polymer dielectrics. We conclude that choice of gate dielectric is very crucial in determining overall performance of OTFTs. Various factors which need to be considered while choosing a gate dielectric material are dielectric

constant, method of deposition, energy band gap, temperature coefficient, polarity and mechanical properties like Poisson's ratio and tensile strength. In addition to these bulk properties, surface characteristics like surface roughness and surface energy of dielectric layer plays a crucial role in improving the performance of OTFTs.

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