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On the structural and electrical properties of metal–ferroelectric–high k dielectric–silicon structure for non-volatile memory applications

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Abstract. In this article, we report the structural and electrical properties of metal–ferroelectric–high k dielectric–silicon (MFeIS) gate stack for non-volatile memory applications. Thin film of sputtered $SrBi_2Nb_2O_9$ (SBN) was used as ferroelectric material on 5–15 nm thick high-k dielectric (Al_2O_3) buffer layer deposited using plasma-enhanced atomic layer deposition (PEALD). The effect of annealing on structural and electrical properties of SBN and Al_2O_3 films was investigated in the temperature range of 350–1000°C. X-ray diffraction results of the SBN and Al_2O_3 show multiple phase changes with an increase in the annealing temperature. Multiple angle ellipsometry data show the change in the refractive index (n) of SBN film from 2.0941 to 2.1804 for non-annealed to samples annealed at 600°C. For Al_2O_3 film, $n < 1.7$ in the case of PEALD and $n > 1.7$ for sputtered film was observed. The leakage current density in MFeIS structure was observed to two orders of magnitude lower than metal/ferroelectric/silicon (MFeS) structures. Capacitance–voltage (C–V) characteristics for the voltage sweep of −10 to 10 V in dual mode show the maximum memory window of 1.977 V in MFeS structure, 2.88 V with sputtered Al_2O_3 and 2.957 V with PEALD Al_2O_3 in the MFeIS structures at the annealing temperature of 500°C.

Keywords. Ferroelectric; high-k dielectric; memory window; PEALD; XRD.

1. Introduction

In recent years, ferroelectric thin films were extensively studied for the non-volatile memory applications due to their unique electrical properties [1,2]. Currently, there are two types of ferroelectric random access memory (FeRAM) technology: the destructive readout type consisting of one transistor plus one capacitor [3] and the non-destructive readout with only one transistor memory cell made of ferroelectric gate stack [4]. Also, in future, these non-destructive readout–FeRAM have potential to replace the FLASH and EEPROMs (electrically erasable programmable read-only memory)-based non-volatile memories due to their lower writing voltages, faster writing speeds and better endurance. Owing to this reason, the considerable research effort is focussed to improve the properties of single transistor-based FeRAM structure.

Amongst the various ferroelectric materials with general formula ABO_3 such as $Pb[Zr_xTi_{1-x}]O_3$ (PZT), $Bi_4Ti_3O_{12}$ (BIT), $SrBi_2Nb_2O_9$ (SBN) and $SrBiTa_2O_9$ (SBT), PZT has received considerable attention for their application as the gate material for MFeIS structure-based non-volatile memories [5–10]. PZT shows large data retention capabilities [11] than the bismuth-layered perovskite material, but the lead content, its diffusion in silicon and the fatigue results difficulty in its incorporation with silicon and hence, non-reliable [12,13]. In spite of relatively low remnant polarization and high temperature processing [14], bismuth-layered perovskite material like SBN possesses high fatigue resistance and low leakage current that makes it one of the promising candidate for the MFeIS-based FeRAM [15–17]. Recently, SBN with different compositions of strontium and bismuth, prepared by sol–gel [18,19], pulsed laser deposition [20], metalorganic chemical vapour deposition [21], solid-state reaction process [22,23] was studied. However, it is very difficult to form a ferroelectric-semiconductor interface with good electrical properties in MFeS structures due to ferroelectric/silicon interdiffusion and poor quality of interface [24,25]. To overcome these problems of MFeS structure, MFeIS structure was proposed with a thin film of insulating buffer layer compatible with the ferroelectric and silicon. The buffer layer prevents the reaction and interdiffusion between the ferroelectric layer and the silicon substrate and as well as provide a potential barrier for charge injection from the silicon substrate thus, improving the retention time in particular. Although the retention time in MFeIS structure can be improved when compared to MFeS structure, the MFeIS structure still suffers from the problem of depolarization field [26] and voltage drop across the buffer layer. Several materials, such as SiO_2, MgO, Si_3N_4, CeO_2, etc. [27–29] with different dielectric constant values were proposed and studied as the buffer layers, but the use of high-k dielectrics such as ZrO_2, Al_2O_3, HfO_2 are preferred to minimize the voltage drop across the insulator and the

Table 1. Deposition conditions for sputtering and PEALD.

Material	SBN	Al_2O_3	Al_2O_3
Deposition process	Sputtering	Sputtering	PEALD
Process material	99.99% pure SBN target	99.99% pure Al_2O_3 target	99.999 + % pure trimethylaluminum precursor
Base pressure	5×10^{-5} Torr	5×10^{-5} Torr	3.3 Pascal
Working pressure	1.1×10^{-2} Torr	1.1×10^{-2} Torr	27.13 Pascal
Argon gas flow rate	19.6 sccm	19.6 sccm	—
Oxygen gas flow rate	—	—	75 sccm
RF power	100 W	100 W	200 W
Substrate temperature	Room temperature	Room temperature	200°C

possibility of using high physical thickness for reduced leakage thus, improving the retention time. In this case, the coupling between the ferroelectric polarization and surface charge on Si substrate also not reduced. Further, the thickness of the buffer layer plays very crucial role in minimizing the charge injection and interdiffusion and needs to be optimized and precisely to be controlled for a particular ferroelectric layer.

In this study, we have investigated the behaviour of plasma-enhanced atomic layer deposited (PEALD)-Al_2O_3 as the buffer layer because of its good thermodynamic stability with the ferroelectric material due to its high Gibbs formation energy as compared to other oxides [30]. Al_2O_3 thin film annealing temperature was optimized to obtain higher negative charges and lower leakage current. Constant thickness of 100 nm-sputtered SBN layer was used, since the ferroelectric properties are observed to be independent of the thickness of ferroelectric layer [31,32]. The deposited thin film of Al_2O_3 and SBN were analysed through X-ray diffraction (XRD) for structural properties. Electrical characterization was carried out to obtain the device memory window, capacitance behaviour and leakage current density using the MFeIS capacitors.

2. Experimental

Single side polished, p-type, 2″ diameter, CZ-silicon wafer of orientation ⟨100⟩ with resistivity of 1–10 Ω-cm was used as the substrate material for the fabrication of MFeS and MFeIS structures. The substrates were chemically cleaned using standard Radio Corporation of America (RCA) developed RCA-1 and RCA-2 processes followed by thorough rinsing in deionized water and nitrogen drying before loading to the deposition chamber. For sputtering, 99.99% pure $SrBiNb_2O_9$ target procured from Advanced Engineering Materials, USA, was used, whereas the aluminium oxide was sputter-deposited using 99.99% pure target obtained from Process Material Inc., USA. In PEALD system, 99.999% pure trimethylaluminium precursor obtained from STREM Chemicals, USA, was used to deposit high-quality Al_2O_3 layer. The mono layer of Al_2O_3 was deposited at the rate of 0.143 nm per cycle in the presence of oxygen plasma for the period of 1 s per cycle in SENTECH SI-ALD System procured from M/s SENTECH, GmbH, Germany. The precursor is heated and kept at the temperature of 80°C and nitrogen at a flow rate of 20 standard cubic centimeters per minute (sccm), acts as a carrier for the precursor to the reaction chamber. Different deposition conditions for the sputtering and PEALD are summarized in table 1.

After deposition, annealing of thin films was carried out in the quartz tube furnace procured from M/s Thermco Systems, UK, in the temperature range of 350–500°C for Al_2O_3 and from 500 to 1000°C for the SBN film in the presence of nitrogen flowing at the rate of 20 sccm for 30 min. After annealing, aluminium electrodes are deposited by thermal evaporation at the chamber pressure of 5×10^{-5} Torr with a circular area of 2.28×10^{-3} cm^2 through a shadow mask. Metal/Al_2O_3/silicon, metal/SBN/silicon and metal/SBN/Al_2O_3/silicon structures were fabricated and electrically characterized.

SE400adv multiple angle laser ellipsometer equipped with HeNe laser and operating at 632.8 nm, procured from SENTECH Instruments GmbH, Germany, was used to determine the thickness, refractive index (n), adsorption constant (k) and degree of polarization of the SBN and Al_2O_3 thin films. For the structural characterization of ferroelectric and Al_2O_3 buffer layers, XRD system with 1.54 Å CuK α laser wavelength was used. Keithley 4200 Semiconductor system procured from Keithley Instruments, USA, was used for C–V and current *vs*. voltage (I–V) measurements. C–V characterization was carried out at the frequency of 70 kHz for voltage range of −10 to 10 V at the step size of 0.1 V in dual sweep mode to obtain the memory window. The leakage current density is obtained by current *vs*. voltage characteristic for the voltage range of −10 to 10 V.

3. Results and discussion

3.1 *Structural analysis*

Figure 1 shows the XRD pattern of SBN/Si structure annealed in the temperature range of 400–1000°C in nitrogen ambient for 30 min. SBN directly deposited on silicon shows the dominant peak at $2\theta = 28.3°$, which corresponds to

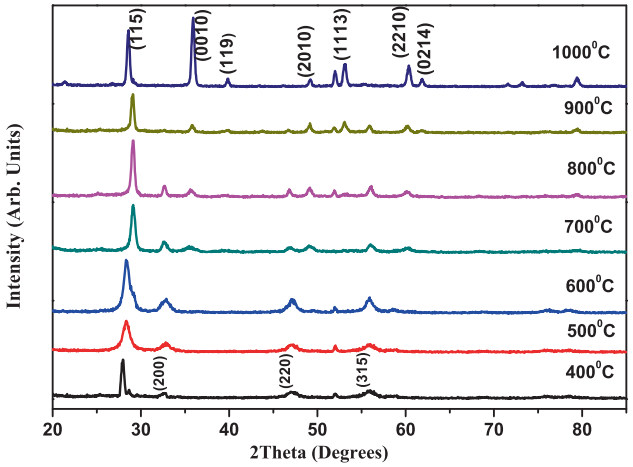

Figure 1. XRD pattern of SBN 100 nm annealed in the temperature range of 500–1000°C in nitrogen ambient for 30 min.

the ⟨115⟩ orientation and denotes the perovskite structure. The peak intensity at $2\theta = 28.3°$ increases with annealing up to 800°C and decreases with further increase in the temperature. At the annealing temperature of 500°C, the secondary peaks of lower intensities are observed at $2\theta = 32.9$, 47.17, 52.5 and 55.96°, which correspond to orientations of ⟨200⟩, ⟨220⟩, ⟨1113⟩ and ⟨315⟩. XRD results clearly indicate that the deposited SBN film has single-phase perovskite structure compared to the data JCPDS-89-8156 and the crystal lattice constant decreases with an increase in the annealing temperature. The intensities of secondary phase peaks do not increase significantly till the annealing temperature reaches 900°C. Secondary phase at $2\theta = 34.9°$ corresponds to the crystal orientation of ⟨0010⟩ arises significantly at the annealing temperature of 1000°C. Several other peaks of low intensities were observed at 1000°C, which are due to the interdiffusion between ferroelectric and silicon [33]. Interdiffusion causes Sr and Bi deficiencies in the SBN crystal attributed to the decrease in the ferroelectric and dielectric characteristics.

Figure 2a and b shows the XRD pattern of sputtered and PEALD Al_2O_3/Si structures, respectively, annealed at different temperatures for 30 min in the presence of nitrogen ambient. High intensity peak observed at $2\theta = 52°$ is due to the silicon substrate. Further, there is no secondary sharp peak in the PEALD and sputtered Al_2O_3 was observed confirming the amorphous nature of Al_2O_3, a major requirement for the gate dielectric [34]. Low intensity peaks at $2\theta = 55°$ were observed in all the samples corresponding to ⟨312⟩ orientation of the Al_2O_3 film compared to the data JCPDS-86-1410. When compared with the XRD pattern of Al_2O_3 films annealed at different temperatures, it is observed that the film annealed at 425°C has minimum intensity peaks indicating the fully amorphous nature [35].

Multiple angle ellipsometric analysis was carried out to assess the quality of thin films of SBN and Al_2O_3 and to help in optimization of deposition and annealing conditions. Measurements were performed in the range of incident angle

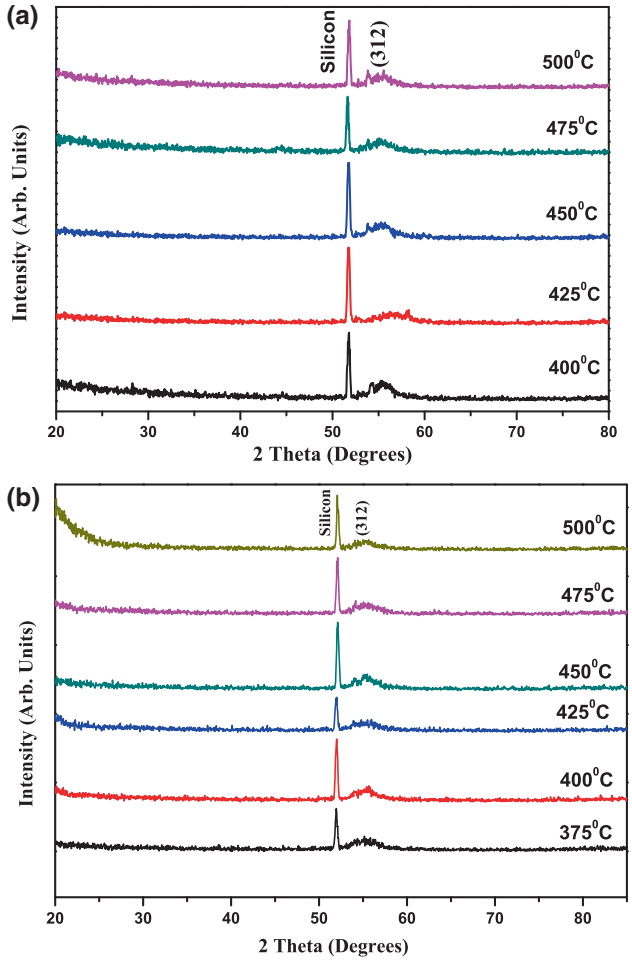

Figure 2. XRD pattern of (**a**) sputtered and (**b**) PEALD Al_2O_3, annealed at different temperatures in nitrogen ambient for 30 min.

from 60 to 80° at 5° steps to find out the refractive index (n), absorption constant (k), thickness (t) and polarization of the films. Experimentally, it was observed that non-annealed film of 100 nm SBN shows the absorption constant (k) of 0.0124, whereas other films do not show any absorption effect. Theoretical studies indicate that higher refractive index of the film corresponds to high density, indicating high quality of thin films [36]. The dependence of refractive index (n) on annealing temperature for both SBN and Al_2O_3 obtained by ellipsometric technique is shown in figure 3.

It is evident from the figure that the SBN films annealed between 400 and 600°C have almost constant refractive index of 2.1804, indicating that the density and stoichiometry of the film is maintained. In SBN film, high atomic mass of the Sr (87.62), Bi (208) and Nb (93) atom along with the deposition technique, results in its high density. Further, the refractive index of sputtered Al_2O_3 (1.7011–1.7411) is observed to be higher indicating higher density of sputtered film than PEALD Al_2O_3 (1.6560–1.6957). Perhaps, in sputtered Al_2O_3, high energy neutral ion bombardment during deposition provides a local re-arrangement of atoms, allowing them to relax in

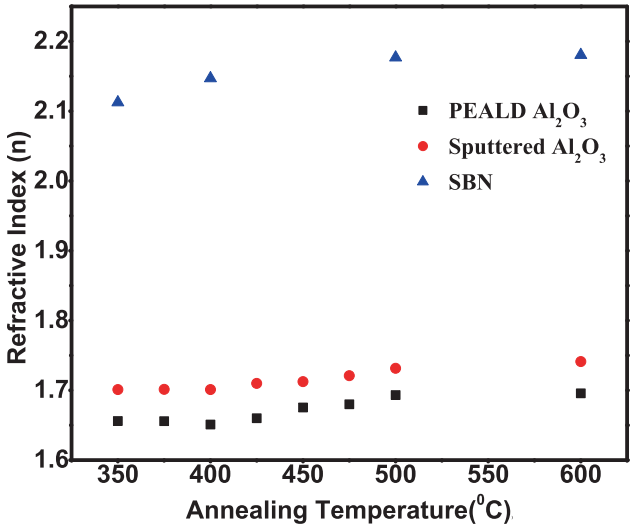

Figure 3. Refractive index (n) of PEALD Al_2O_3, sputtered Al_2O_3 and sputtered SBN film annealed at the temperature range of 350–600°C.

lower energy sites, results in high density, but also causes residual damage to the film. This residual damage can be further minimized by annealing.

3.2 *Electrical characterization*

3.2a *Al_2O_3 film optimization*: To quantitatively assess the charge storage properties of SBN, systematic experiments followed by characterization were carried out. First of all, it was essential for us to obtain an optimized buffer layer deposition and annealing condition, which result in excellent high-k/Si interface with low leakage current, oxide charge and interface trap density. For this, initial experiments were carried out using metal/insulator/silicon (MIS) structure with differently deposited and annealed capacitor structures. C–V characteristics of a MIS capacitor with 10 nm thickness of Al_2O_3 insulator layer deposited by sputtering and PEALD annealed at different temperatures for 30 min in nitrogen ambient is shown in figure 4a and b.

It can be seen from the figure that the flat band voltage shifts towards positive with annealing up to 425°C and reverses its trend with further increase in annealing temperature. This clearly indicates the build-up of negative charges at the interface for both sputtered as well as PEALD-deposited Al_2O_3 films at 425°C. Further, Al_2O_3 deposited using PEALD show a large flat band shift of about 5.0 V, indicating large negative build up of charges at the interface as compared to the sputtered Al_2O_3 film. After optimization of the deposition and annealing conditions, Al_2O_3 film thicknesses of 5, 10 and 15 nm deposited by PEALD were used as the buffer layers in further investigation.

3.2b *Metal/SBN/silicon (MFeS) capacitor*: The optimization of SBN film deposition and annealing condition was

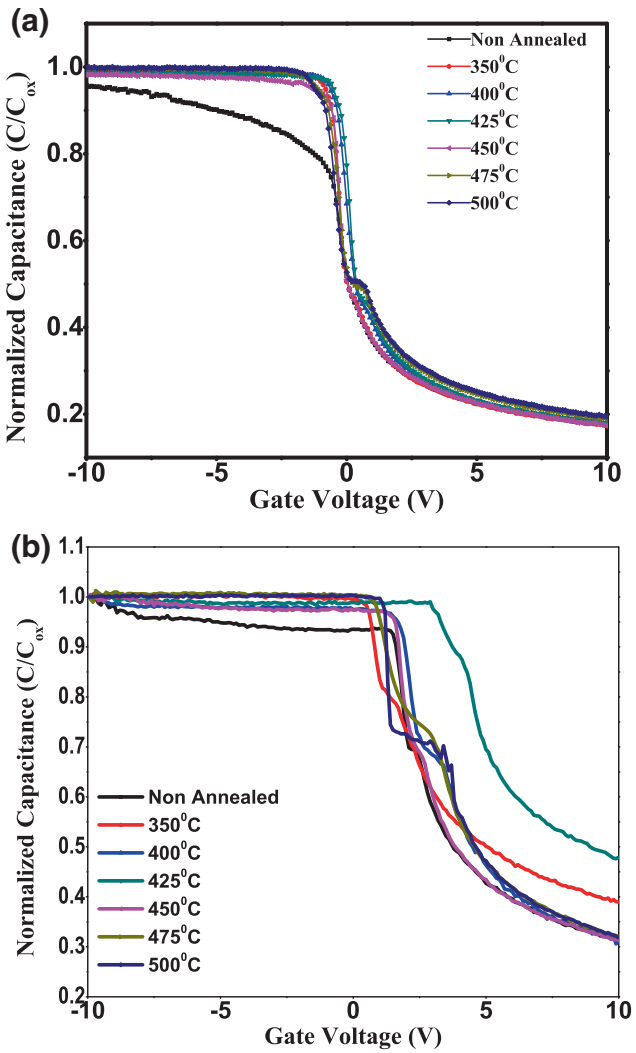

Figure 4. C–V characteristics of MIS capacitors with Al_2O_3 deposited by (**a**) sputtering and (**b**) PEALD, annealed at different temperatures.

also carried out using MFeS capacitor structures. A constant thickness of 100 nm SBN deposited by magnetron sputtering was used as the ferroelectric layer. The leakage current and memory window were used as an indicator of the quality of the ferroelectric films.

Figure 5 shows the leakage current density *vs.* gate voltage characteristic of the Al/SBN/Si structures annealed at different temperatures. The reduction in leakage current density with annealing temperature is indicative of the fact that annealing improves the film and interface properties. Lowest leakage current density of the order of 10^{-3}–10^{-4} A cm^{-2} was observed for the devices annealed in the temperature range of 500–600°C. Significant reduction in the leakage current in devices annealed at 500°C is attributed to the reduction in trap density, improvement in SBN/Si interface and deposited film properties. Two–three orders of increased leakage current densities are observed for the devices annealed at higher temperatures (700–800°C). A difference of minimum one order

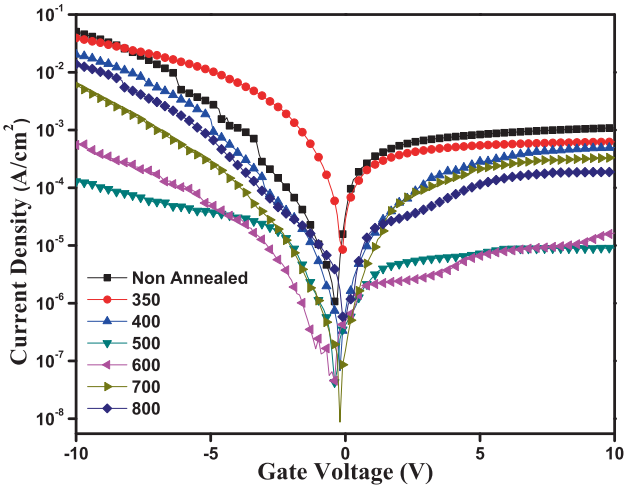

Figure 5. J–V characteristics of the Al/SBN/Si structure annealed at different temperatures.

was observed in the leakage current density of the device for negative and positive gate biases, which is attributed to the charge injection from the substrate into the ferroelectric film on the application of negative potential at the gate. On the application of high gate voltages, high electric field induces large charge injection from silicon to ferroelectric through buffer layer and vice versa, resulting in large leakage current density. Increasing annealing temperature degrades the dielectric property of the SBN film due to the damage to the stack and increase in interface trap density causes trap-assisted tunnelling and increase in leakage current in MFeS structure.

The dependence of memory window and flat band voltage on annealing temperature measured for the MFeS structure is presented in table 2. Consistent with the leakage current data (figure 5), it can be seen from the table that maximum memory window of 1.977 V was obtained on devices annealed at 500°C. Increase in memory window is due to the SBN film crystallization and reduction in the defect arises during sputtering. Also, large positive flat band voltage shift of 0.9 V observed at this annealing temperature, signifies the build up of large negative fixed charge density at the SBN/Si interface. In the MFeS structure, the memory hysteresis increases with annealing temperature up to 500°C and decreases with further increase in the temperature. Increase in annealing temperature above 500°C starts interdiffusion between the ferroelectric layer and silicon substrate along with the depletion of Sr and Bi atoms from the SBN film (loss in stoichiometry), leading to decrease in the net polarization and memory retention capacity. Depletion of Bi atoms from the SBN film causes reduction in negative charges and degradation in the SBN/Si interface, responsible for the shift in flat band voltage towards negative.

3.2c *Metal/SBN/PEALD Al_2O_3/silicon (MFeIS) capacitor structure*: After optimizing the buffer layer and ferroelectric layer deposition and annealing condition independently, we further looked into the effects of annealing on the composite layer in the temperature range of 350–600°C. MFeIS structures were fabricated with fixed SBN thickness of 100 nm by sputtering on the PEALD Al_2O_3 films of 5, 10 and 15 nm thicknesses. The electrical characterization is carried out to investigate the memory window, flat band voltage and leakage current density. The leakage current density *vs.* gate voltage measured in MFeIS structures annealed at 425°C with different buffer layer thicknesses is shown in figure 6.

The leakage current density was observed to decrease with increase in buffer layer thickness. Minimum leakage current densities of 9×10^{-5} and 9×10^{-6} A cm^{-2} at the gate voltages of -10 and $+10$ V, respectively, were observed in the MFeIS structure with 15 nm buffer layer thickness. MFeIS structure shows non-symmetric leakage current behaviour for 15 nm buffer layer thickness at low gate voltage (near 0 V), which is due to the large potential barrier provided by the thick buffer layer to the charges to tunnel trough. At high gate voltages of ± 10 V, trap-assisted conduction and tunnelling become dominant resulting in symmetrical leakage current density.

The data extracted from the C–V characteristics of MFeIS structures with different buffer layer thicknesses are summarized in table 3.

C–V result indicates that the MFeIS structure with 10 nm buffer layer annealed at 500°C shows the maximum memory window that is 2.957 V and the flat band voltage shift of

Table 2. Memory window and flat band voltage in metal/SBN/silicon structure annealed for the temperature range of 350–800°C.

	SBN (100 nm)	
Annealing temperature (°C)	Memory window (V)	Flat band voltage (V)
Non-annealed	1.21	− 1.3
350	1.464	− 0.3
400	1.791	0.3
500	1.977	0.9
600	1.11	− 0.2
700	0.17	− 1.7
800	0.149	− 6.1

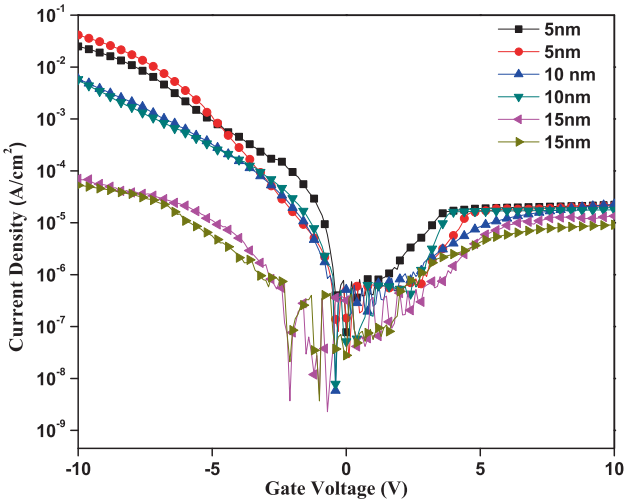

Figure 6. J–V characteristic of MFeIS structure with different buffer layer thicknesses.

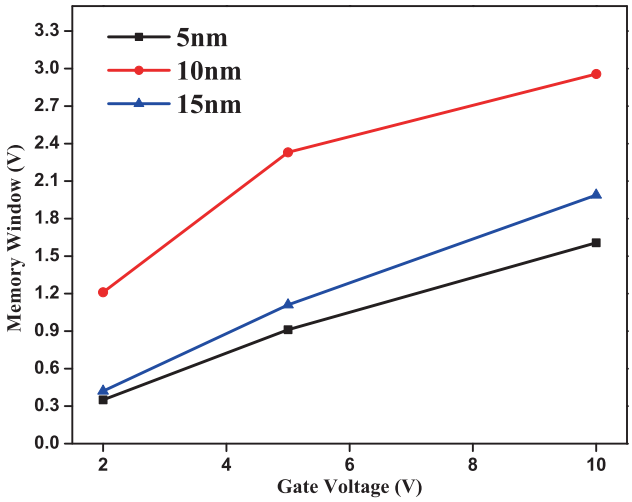

Figure 7. Memory window of MFeIS structures with different buffer layers2 annealed at 500°C and at different gate voltages.

7.8 V. Large memory window at 500°C is due to the crystallization of SBN film and reduction in interface trap density as discussed in section 3.2b. The crystallization to perovskite structure observed at an annealing temperature of 500°C is also supported by our XRD analysis. At the same annealing temperature, MFeIS structures with 5 and 15 nm buffer layers show a memory window of 1.6 and 1.988 V, respectively. For thin insulating buffer layer, the possibility of charge tunnelling become maximum on the application of high electric field resulting in lower charge retention capacity and memory window. Memory window of the MFeIS structure with different buffer layer thicknesses annealed at 500°C and for different gate voltages is shown in figure 7.

For 10 nm buffer layer thickness, the memory window observed is maximum, i.e., in the range of 1.2–2.957 V for the gate voltages of 2–10 V, respectively. In the MFeIS capacitor operation, the voltage applied at the gate (V_G) appears across the ferroelectric layer (V_F) and buffer layer (V_I), the reason behind the significant high voltage operation of MFIS–FET. Since the charge matching condition indicates that for constant ferroelectric thickness, the device memory window should decrease with increasing insulating buffer layer thickness [36]. But, in present experiment, we have observed that the device with 5 nm buffer layer shows a lower memory window than 10 nm buffer layer. It is due to the reason that when a gate voltage is applied to the thin buffer layer of 5 nm than this layer, turns a moderate gate voltage into a high electric field that causes severe stress and high interface trap charges [37] resulting in lower memory window and data retention capacity.

Also, the memory window measured by C–V characterization in MFeS, MFeIS (sputtered Al_2O_3) and MFeIS (PEALD Al_2O_3) structures is shown in figure 8.

The results clearly indicate that insulating buffer layer between the ferroelectric and silicon substrate improves the memory window along with a large negative charge at the Si/Al_2O_3 and Al_2O_3/SBN interfaces. For the sputtered Al_2O_3 buffer layer, the improvement in memory window and shift in flat band voltage is lower as compared to the PEALD Al_2O_3 buffer layer of the same thickness and annealing conditions. Improvement in memory hysteresis is the indicative of lower leakage current as discussed in section 3.2c. Data comparison also indicates that deposition technique along with the buffer layer thickness plays an important role in the memory window and leakage behaviour of the M/Fe/high-k/Si devices.

Table 3. Electrical characteristics of MFeIS structures with 5, 10 and 15 nm PEALD Al_2O_3 buffer layers.

		Annealing temperature (°C)			
Buffer layer thickness (nm)	Electrical parameters (V)	350	400	500	600
5	Memory window	0.523	1.1	1.6066	1.0923
	Flat band voltage	3.8	5	5.8	5
10	Memory window	1.231	2.7305	2.957	1.43119
	Flat band voltage	5.8	6.6	7.8	6.2
15	Memory window	0.852	1.3499	1.988	1.012
	Flat band voltage	4.5	5.5	6	5.2

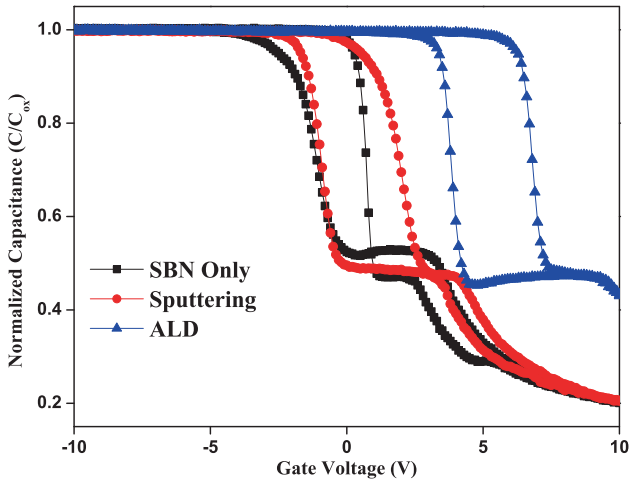

Figure 8. C–V characteristics of metal/SBN/silicon, metal/SBN/sputtered Al_2O_3/silicon and metal/SBN/PEALD Al_2O_3/silicon structures annealed at 500°C.

4. Conclusion

The structural and electrical characterizations of MFeS and MFeIS structures with SBN as ferroelectric layer and high-k dielectric Al_2O_3 as buffer layer deposited using PEALD, was investigated. Sputtered Al_2O_3 layer of same thickness was used for comparison. XRD characteristics show the single phase perovskite structure of the SBN film in the temperature range of 400–800°C. Ellipsometric analysis indicates the refractive index (n) between 2.0941 and 2.1804 for SBN, $n < 1.7$ for PEALD Al_2O_3 and $n > 1.7$ for sputtered Al_2O_3 films. Electrical characterization shows the memory hysteresis of 1.977 V for metal/SBN/silicon, 2.88 V for metal/SBN/sputtered Al_2O_3/silicon and 2.957 V for metal/SBN/PEALD Al_2O_3/silicon structures. With the introduction of insulator layer, there is a reduction in leakage current density of the order of one. This characteristic indicates that the MFeIS capacitor with SBN as the ferroelectric layer and Al_2O_3 deposited by sputtering and PEALD is a potential candidate in non-volatile FeFET applications.

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