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Investigation of capacitance characteristics in metal/high-*k* semiconductor devices at different parameters and with and without interface state density (traps)

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Abstract. Capacitance *vs.* voltage ($C-V$) curves at AC high frequency of a metal–insulator–semiconductor (MIS) capacitor are investigated in this paper. Bi-dimensional simulations with Silvaco TCAD were carried out to study the effect of oxide thickness, the surface of the structure, frequency, temperature and fixed charge in the oxide on the $C-V$ curves. We evaluate also the analysis of MIS capacitor structures by different substrate doping concentrations with and without interface state density at different temperatures (100, 300 and 600 K). These studies indicate that the doping substrate concentration and the traps enormously affect the high-frequency $C-V$ curve behaviour. We also demonstrate that for low and high temperatures, the high-frequency $C-V$ curves behaviour changes, indicating that the capacitance due to the substrate is significantly influenced in these conditions (bias and substrate doping concentration).

Keywords. $C-V$ characteristic; high-*k* dielectric; interface state density; MIS structure; nanotechnology; TCAD simulation.

1. Introduction

Microelectronics knowledge mostly based on silicon and silicon dioxide (SiO_2) thin films has been used over the last three decades in integrated circuits. The continued reduction of device size has now necessitated the diminution of the thickness of the gate oxide layer to a few nanometres in order to maintain the same degree of gate control over the channel from a high leakage current [1]. Replacing SiO_2 with high-*k* materials is the prime technological challenge [2]. In recent years there has been a growing interest in metal oxides as dielectric materials for gate oxides of MOSFETs and stable capacitors in ultra-large-scale integrated electronic circuits (ULSI). Extensive research is now in progress to find other insulators with a higher dielectric constant, large band gap, significant conduction band offset and high breakdown strength for use in sub-100-nm silicon technology [3,4]. New dielectric conductor combinations should be tuned for the right metal work function as well as the optimum thermochemical stability of the layer stack. Hence, much effort has been made to explore new combinations of dielectric and conductive layers so that miniaturization of MOS-based devices can be continued following Moore's law. The TiN/Al_2O_3 combination has been identified as a promising and especially reliable candidate, thanks to its chemical compatibility and thermal stability, good adhesion properties on various substrates and low interface trap densities in TiN/Al_2O_3/p-Si devices [5]. Furthermore, both materials can be relatively easily synthesized by atomic layer deposition (ALD) under compatible processing conditions. Al_2O_3 is known for its modest dielectric permittivity of $\sim$9 and high breakdown electric field due to its large band gap (9 eV) [6,7]. Moreover, it has a large band offset with Si, which is crucial in maintaining low leakage currents through devices [8]. The metal nitride TiN has a well-established midgap, with a low electrical resistance. Therefore, it is commonly used as an electrode material that blocks the outdiffusion of Si more efficiently than Al. Metal-oxide-semiconductor (MOS)-type structures play a crucial role in many devices, especially in microelectronics and optoelectronics. The performance and reliability of MOS devices are strongly dependent on the formation of insulator layer (native or deposited), interface states (N_{ss}) localized at the semiconductor–insulator interface and the series resistance (R_s). The electrical and dielectric properties of these devices strongly depend on the applied voltage, frequency and temperature. In this paper, we present a theoretical study through bi-dimensional simulator ATLAS [9], to investigate capacitance–voltage characteristics of metal–insulator (high k: Al_2O_3) semiconductor (p-Si) devices.

We report on the effect of bias voltage, silicon substrate doping concentration, frequency and temperature on the electrical and dielectric properties of TiN/Al_2O_3/p-Si structure in

which the Al_2O_3 dielectric layer is deposited by ALD. Our approach is based on numerical bi-dimensional (2D) simulation by self-consistently solving Schrodinger and Poisson equations using a finite-difference method with non-uniform mesh sizes.

2. Device characteristics

The metal/insulator/semiconductor (MIS) capacitor used during the simulations performed for this study is composed of a titanium nitride gate, an Al_2O_3 insulator layer with $T_{ox} = 5$ nm and a p-type silicon substrate with a doping concentration $N_A = 1e16$ cm^{-3}. The surface of our MIS structure is assumed to be 100×100 μm^2 for all bi-dimensional simulations. A DC voltage (V_G) was applied to the capacitor gate, varying from –3 to 2 V, and a study of AC high-frequency $C-V$ curve was performed, maintaining frequency at 1 kHz for all simulations.

3. Bi-dimensional numerical simulation of $C-V$ curves: results and analyses

3.1 *Experimental validation*

We first illustrate $C-V$ characteristics by comparing, in figure 1, our simulated results and experimental data [10] for three (10 kHz, 500 kHz and 1 MHz) high-frequency curves for an Al/CeO_2/p-Si MOS capacitor. Structure simulated where CeO_2 thin film having a thickness of ≈55 nm and dielectric constant value of ≈22.

Simulated and experimental data are in good agreement in accumulation, depletion and inversion regimes, which enables us to adapt our simulation code to determine $C-V$ characteristics for different physical parameters and with and without interface traps for our study structure TiN/Al_2O_3/p-Si.

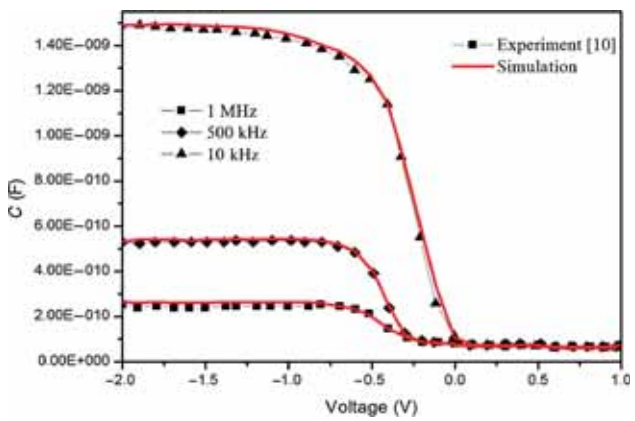

Figure 1. Comparison between experimental data [10] (symbol) and simulated (line) $C-V$ curves for Al/CeO_2/p-Si MOS capacitor.

3.2 *C–V for different physical parameters*

$C-V$ analysis is considered as one of the most important tools for characterizing MOS systems [11]. The first $C-V$ curve obtained is shown in figure 1. Figure 2b presents the different regimes. The working conditions of a MIS device depend on the applied continuous voltage V_G. Essentially, three typical bias voltage regions are considered. Referring to a device on a p-type semiconductor, the first region corresponds to V_G lower than the flat-band voltage V_{FB}, the second is between V_{FB} and a threshold voltage V_T (termed as inversion threshold) and the third is when V_G is larger than V_T.

The regimes of accumulation and depletion are clear. The changeover plan is generally more difficult to observe on MIS structures based on silicon at room temperature, due to a low generation rate of minority carriers. The deep depletion regime is most often reported in the literature [12,13].

The total capacitance of the MOS structure is expressed by the series association of the oxide capacitance C_{OX}, which is constant for a given T_{ox} thickness, and the semiconductor capacitance C_{SC}, which is the sum of the depletion capacitance C_D, which varies with width W_d, and the inversion capacitance C_{inv}, which is dependent on the minority carriers accumulated in the depletion region, as shown in Eq. (1):

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{(C_D + C_{inv})}. \tag{1}$$

We changed the thickness of Al_2O_3 to show the influence of oxide thickness on the C–V curve, while maintaining the doping at 1e16 cm^{-3} and frequency at 1 kHz. Figure 2 shows the $C-V$ characteristics simulated for different oxide thicknesses $T_{Al_2O_3}$ varying from 1 up to 5 nm. From this curve, we notice that the variation of oxide thickness acts on the $C-V$ characteristics in the accumulation and depletion regime, whereas in the inversion regime there is no variation in capacitance.

In fact, in the accumulation regime, the ability of the interface can be negligible and the equivalent capacitance of the structure is then

$$\frac{1}{C} = \frac{1}{C_{ox}}. \tag{2}$$

The MIS capacity is equivalent to a thickness of plane capacitor equal to the thickness T_{ox} of the insulator, whose capacity of the oxide layer is inversely proportional to the thickness of the oxide:

$$C_{ox} = \frac{\varepsilon_{ox} S}{T_{ox}}. \tag{3}$$

According to this equation, in the accumulation regime, we can see that the difference between the $C-V$ curves increases with decreasing oxide thickness and this is clear by the proportional characteristic shown in figure 2c. The surface of the

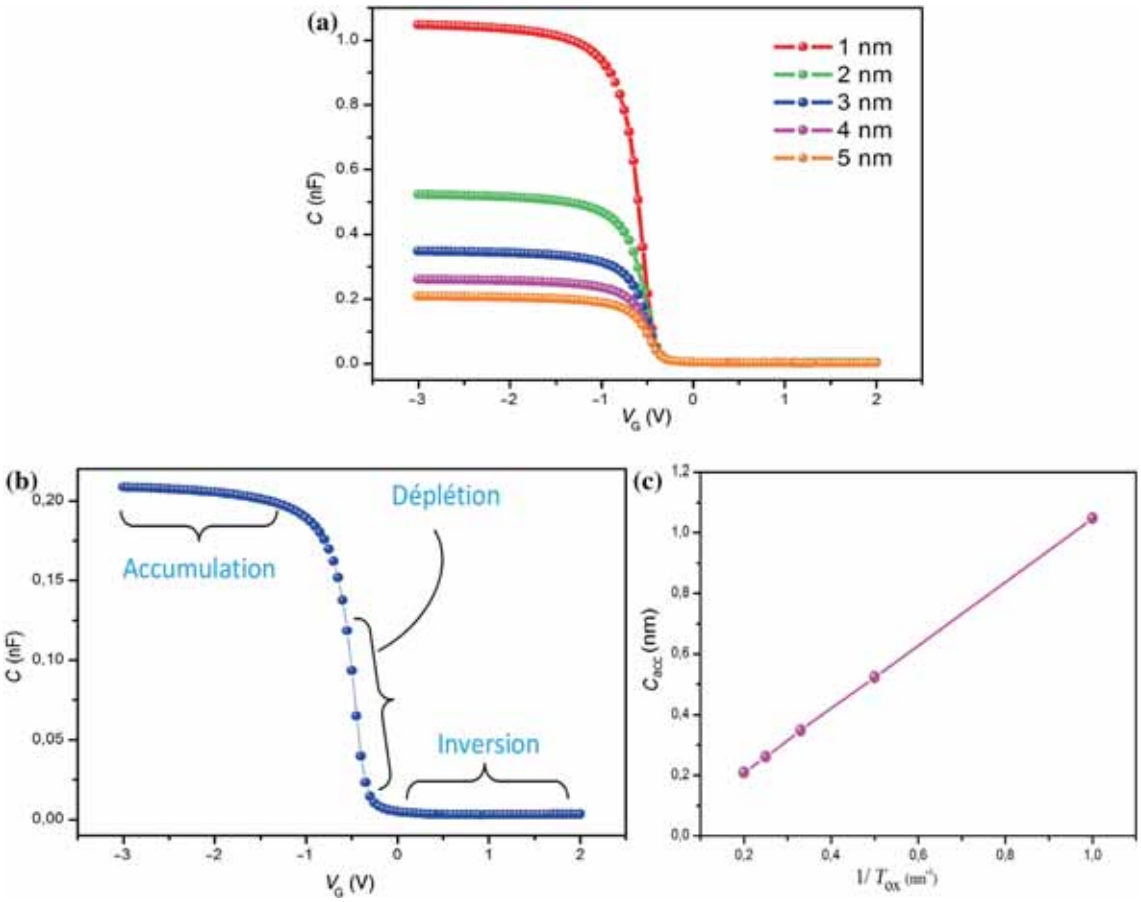

Figure 2. (**a**) $C-V$ characteristics of the MIS structure for different thicknesses of Al_2O_3. (**b**) High-frequency $C-V$ curves for $T_{ox} = 5$ nm, $N_A = 1e16$ cm^{-3} with the different regimes at room temperature. (**c**) Variation of the accumulation capacitance C_{acc} *vs.* different thicknesses of Al_2O_3.

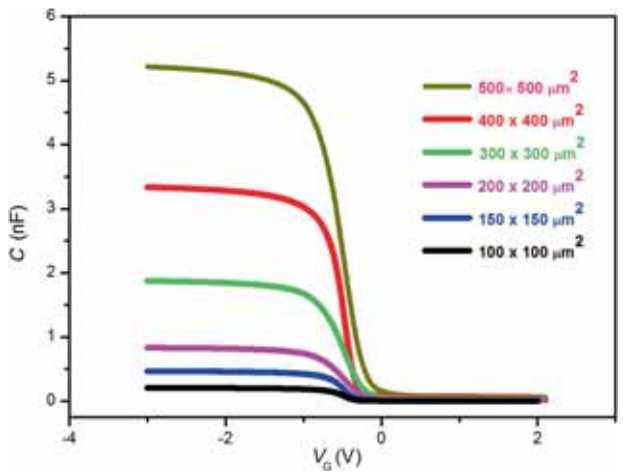

Figure 3. Variation of capacitance *vs.* voltage for different surfaces at a high frequency of 1 kHz and a silicon doping value $N_A = 1e16$ cm^{-3}.

structure has a great importance in the field of nanoelectronics. A study of capacitance *vs.* voltage for different surfaces is given in figure 3.

Figure 3 shows the proportional relation between capacity and surface. This is theoretically shown by Eq. (3). It is noted from this graph that the value of capacitance in the regime of accumulation increases with the increase of surface of the structure. In the inversion regime, it is noted that there is a superposition of capacity curves for different values of the surfaces. It is, therefore, deduced that the surface of the MIS acts on the $C-V$ characteristics only in the regime of accumulation and depletion. To investigate the electrical properties of MOS interfaces, we simulated the $C-V$ curves of MOS capacitors at different frequencies ranging from 1 kHz to 1 GHz. This is shown in figure 4.

The $C-V$ curves of the TiN/Al_2O_3/p-Si MOS capacitor show well-behaved characteristics with no frequency dispersion at 1 kHz up to 100 MHz, implying that ALD Al_2O_3 can passivate Si surfaces well [15]. We deduce from this curve that the effect of frequency on the $C-V$ characteristic appears only at 500 MHz and above, while for the frequencies ranging from 1 kHz up to 100 MHz, $C-V$ characteristics do not change and are superimposed one on the other. The high-frequency $C-V$ characteristics show a strong decrease in the capacity for frequencies higher than 100 MHz. The dispersion may also result from the series resistance created by the

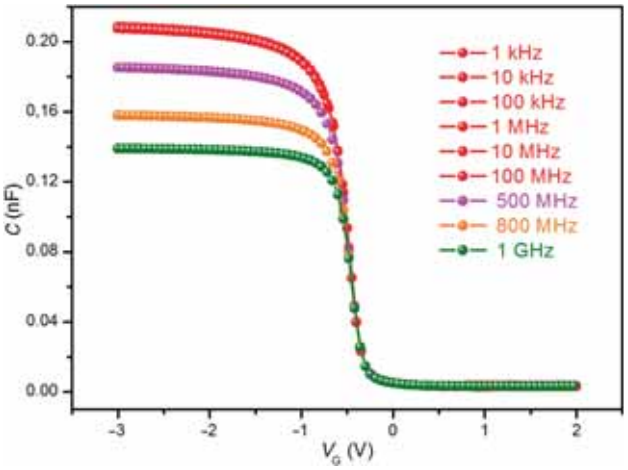

Figure 4. The variation of capacitance *vs.* voltage for different frequencies from 1 kHz to 1 GHz ($T_{Al_2O_3} = 5$ nm, $N_A = 1e16$ cm^{-3}).

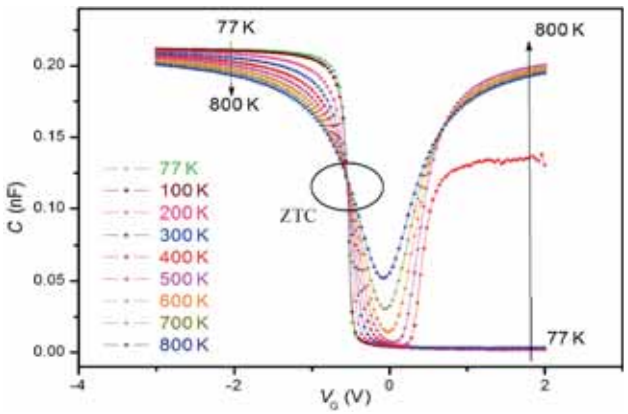

Figure 5. High-frequency $C-V$ curves for $T_{ox} = 5$ nm and $N_A = 1e16$ cm^{-3} with surface area of 100×100 μm^2 for a range of temperatures $T = [77-800]$ K.

weakly doped semiconductor [16]. The capacity at 1 GHz frequency decreases and reaches a value of about 1.4e–10 F. It is also noted that the frequency variation is only in the accumulation regime of the $C-V$ curve. On varying the temperature, curves in figure 5 show that when a positive gate voltage is applied to the MOS capacitor structure ($V_G > 0$ V), the $C-V$ characteristics for 400 K temperature and up to 800 K present a behaviour tendency that diverges from that of the room temperature high-frequency $C-V$ characteristic. This is the inversion area and the tendency suggests that, although the frequency was maintained at 1 kHz, the curves come close to showing a low-frequency $C-V$ curve behaviour for higher temperature values. The rise in the total capacitance value for $V_G > 0$ V indicates that there are physical effects influencing the MOS capacitor structure. More exactly, in the silicon substrate, since the capacitance in the inversion region of the high-frequency $C-V$ curve is mainly due to the substrate depletion region, the capacitance associated with the oxide layer does not change when T_{ox} is maintained constant.

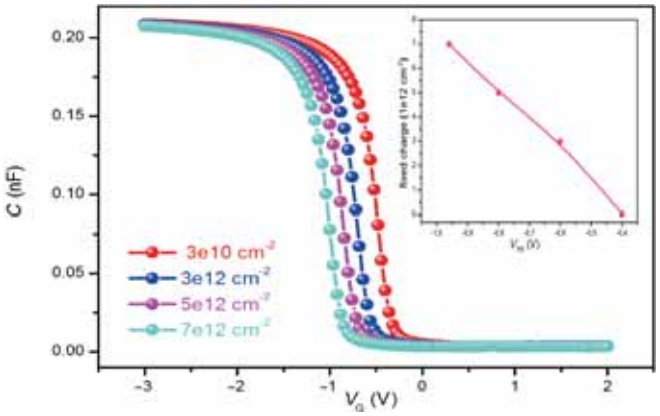

Figure 6. $C-V$ characteristics for different values of fixed charge Q_f at the interface of Al_2O_3/p-Si. Inset: Variation of the fixed charge *vs.* the flat-band voltage V_{FB}.

In the curves of figure 5 it is possible to note the ZTC point (zero temperature coefficient), where the device's electrical characteristics are identical, independent of the operating temperature [17]. Here, we show that $C-V$ curves of the MIS structure for high temperature behave like $C-V$ curves at a low frequency for positive voltages. At high temperature, $C-V$ curves show an increase of capacitance value in the silicon substrate when the device operates in the inversion region. At room temperature, this effect is not present as the carrier generation in the substrate does not undergo the large influence of temperature. On increasing the temperature, the thermal generation of carriers starts to take place in the silicon substrate and becomes the predominant mechanism of electron–hole pair generation, causing intrinsic silicon carrier concentration n_i to increase exponentially with temperature [18–20]. The dependence of n_i on temperature is given by Eq. (4) [20,21]:

$$n_i = 3.9 \times 10^{16} T^{3/2} \exp\left(\frac{-E_g}{2KT}\right). \tag{4}$$

When the device reaches the temperature of 600 K, for example, the intrinsic concentration assumes a value of $n_i \approx 3.9 \times 10^{15}$ cm^{-3}, which is significantly greater than n_i at room temperature, which is about 1.5×10^{10} cm^{-3}. Concerning the effect of the fixed charge on the $C-V$ characteristics, at the Al_2O_3/p-S interface, we simulate the $C-V$ curve for different values of fixed charge. This is shown in figure 6.

It is clear that the flat-band voltage is shifted towards negative voltages when the interface charge density increases. The negative flat band voltages V_{FB} indicate the presence of positive fixed charge in the Al_2O_3/p-Si interface. Al_2O_3 stacks are reported to contain negative charge, with densities ranging from 10e12 up to 1.3e13 cm^{-2} [22]. However, it is shown that the presence of a metal can strongly influence this charge, possibly leading to a total positive charge and this is demonstrated by the work of Loozen *et al* [23]. The Q_f induces a flat-band

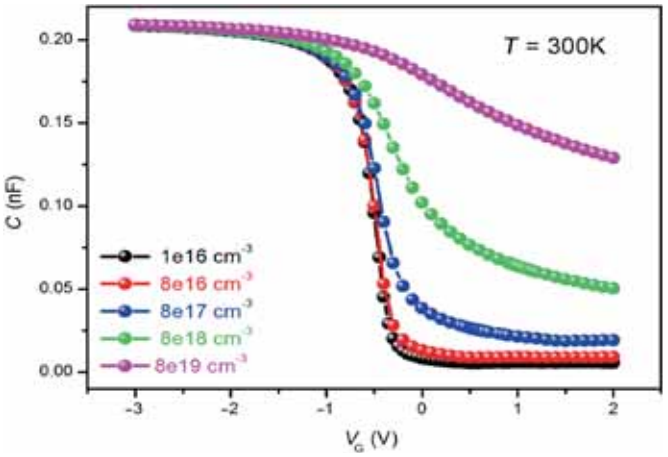

Figure 7. Variation of capacity as a function of voltage for different values of the substrate doping.

voltage shift (V_{FB}) of the gate electrode through capacitive coupling of the gate dielectric, which adversely affects the CMOSFET operation (shift in the threshold voltage) [24]. Shifting of the MIS structure $C-V$ curves is explained by the presence of defects in the insulator, which causes the variation of the threshold voltage V_{TH} or the flat-band voltage V_{FB}. Indeed, fixed charges Q_f located along the insulation interface cause a translation of the $C-V$ curve. If $Q_f > 0$, we have a translation with $\Delta V_{FB} < 0$ and when $Q_f < 0$, we have a translation with $\Delta V_{FB} > 0$. Fixed charge is a limiting factor of the capacitor's lifetime since the associated shift in V_{FB} requires a higher operating voltage and correspondingly higher power consumption [25]. From the results shown in the inset of figure 6, it is possible to notice the decrease of flat-band voltage *vs.* the increase of fixed charge for MIS structure TiN/Al_2O_3 (5 nm)/p-Si. In this section, we present a model to simulate the substrate doping effect on the $C-V$ characteristic of our structure TiN/Al_2O_3 (5 nm)/p-Si for an area of $100\times 100\ \mu m^2$ and high frequency of 1 kHz. The deformations of $C-V$ curves caused by various doping values are shown in figure 7. The uniformity of insulation thickness on the entire surface of a wafer (silicon wafer) is a key parameter to ensure the same electrical characteristics from one component to another.

This curve shows the evolution of the $C-V$ curve for different substrate dopings. The portions of the $C-V$ curve that depend only on the doping of the substrate correspond to the depletion and inversion regimes. However, the accumulation regime is not affected by this variation of the doping profile. Tension flat band varies with the variation of the doping value of the $C-V$ characteristic for MIS structure.

3.3 *C–V characteristics with and without interface traps*

The influence of the substrate implanted doping concentration N_A when the MIS capacitor operates with and without traps at different temperatures 100, 300 and 600 K is shown in figure 8.

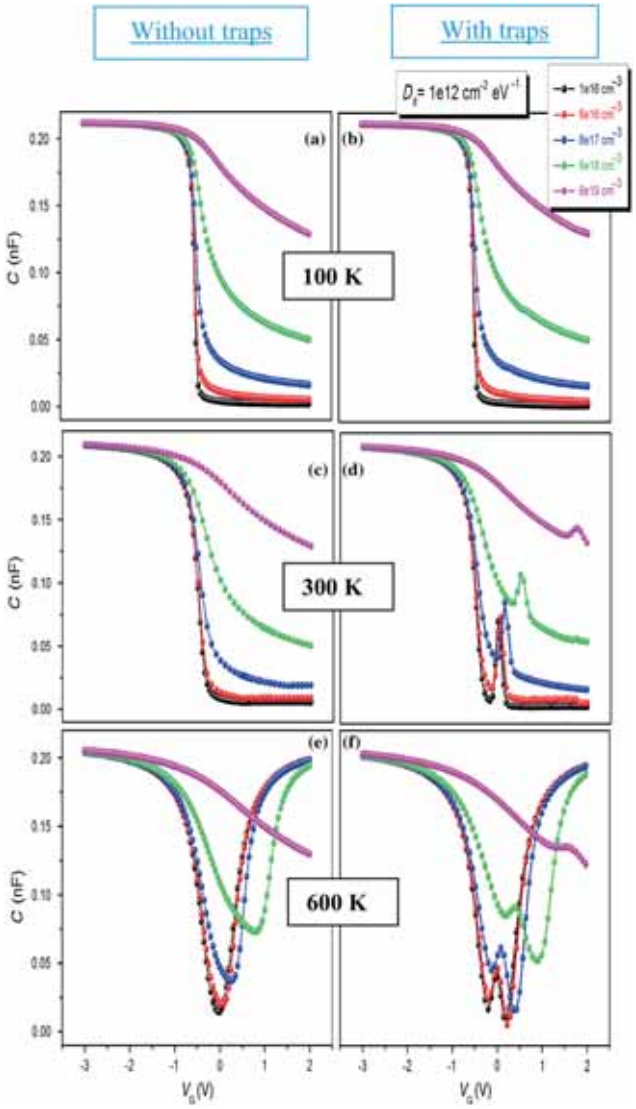

Figure 8. $C-V$ characteristics at different temperatures (100, 300 and 600 K) with and without traps for different substrate doping values ranging from N_A = 1e16 cm^{-3} up to N_A = 8e19 cm^{-3}.

In figure 8a and b at a low temperature of 100 K and for different doping values ranging from 1e16 to 8e19 cm^{-3}, we can see that the introduction of the interface states density D_{it} = 1e12 $cm^{-2}\ eV^{-1}$ in the MIS structure has no effect on the $C-V$ characteristics. It is worth mentioning, through the tendency behaviour of the $C-V$ curves shown in figure 8c–f, that the substrate concentration N_A influences the minimum capacitance value in the inversion region.

The silicon substrate capacitance in the depletion region depends on the maximum depletion region width (W_{dmax}), as published in Eqs. (1) [26] and (2) [27]. It is possible to conclude that the increase of substrate doping concentration causes the inversion region total MIS capacitance to increase

as well, since the capacitance due to the silicon depletion region (C_{Si}) is inversely proportional to the maximum depletion width (W_{dmax}):

$$C_{Si} = \frac{\varepsilon_{Si}}{W_{dmax}}, \tag{5}$$

with

$$W_{dmax} = \sqrt{\frac{2\varepsilon_{Si}2\phi_F}{qN_A}}. \tag{6}$$

In figure 8c and d and at room temperature of 300 K, it is noted that the substrate doping effect is clear for $C-V$ curves. The $C-V$ curves increase in the depletion and inversion regions with increasing doping of the substrate. On introducing the interface state density D_{it} (figure 8d at the Al_2O_3/Si interface for MIS structure, the peak in the $C-V$ curve shifts to the positive voltage with increased substrate doping. The amplitude of this peak decreases with increasing doping of the substrate and becomes negligible for a high concentration of doping. At a higher temperature of 600 K, as shown in figure 8e, we see that the capacity in accumulation or in inversion is equal to the oxide capacity. The interface state density effect is noticed on the $C-V$ curve. There is a change of tendency of $C-V$ compared with $C-V$ without traps. This change is remarkable in the weak inversion region, where the capacitance values are minimal. The peaks due to interface state density are clearer for low doping concentration. These peaks decrease with the increase of doping of the substrate and shift also to the positive voltage.

4. Conclusion

In this work, after experimental validation, we have studied by numerical simulation the effect of different electrical parameters like frequency, oxide thickness, surface of our compound's structure, temperature, substrate doping concentration for different temperatures with and without traps and the oxide charge on the $C-V$ characteristics of the MIS structure TiN/Al_2O_3(5 nm)/p-Si.

These studies of the MIS capacitor at different temperatures (100, 300 and 600 K) indicate that the doping substrate concentration influences high-frequency $C-V$ curve behaviour. It was observed that for gate voltage higher than 0 V, the capacitance values change as the substrate doping concentration increases. Furthermore, it was also noticed that for low and high temperatures, the high frequency $C-V$ curves behaviour changes, indicating that the capacitance due to the substrate is significantly influenced in these conditions (bias and substrate doping concentration). The trend observed in the high-frequency $C-V$ curves in inversion regime operating at high temperature 600 K needs an accurate study in order to elucidate the physical effects that create this deviation observed in MIS capacitor operating in such conditions. The presence of a metal can strongly influence the charge at the interface of Al_2O_3/p-Si, possibly leading to a total positive charge. We demonstrate also that $C-V$ curves of the TiN/Al_2O_3(5nm)/p-Si structure for a high temperature (>300 K) behave like $C-V$ curves at low frequencies for positive voltages. We have shown a decrease of $C-V$ curve in the accumulation regime at 500 MHz; however, from 1 kHz to 100 MHz, the $C-V$ curves are superimposed one over the other.

Hence, the novelty associated with the simulation work is to point out the $C-V$ characteristics for a new structure TiN/Al_2O_3/p-Si with many important parameters like the frequency, temperature and the effect of traps at the interface, etc. These structures satisfy many needs in the fabrication of devices by the nanoelectronic industries.

Acknowledgements

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