Electrical characteristics of metal–insulator–semiconductor and metal–insulator–semiconductor–insulator–metal capacitors under different high- k gate dielectrics investigated in the semi-classical and quantum mechanical models

SLAH HLALI*, NEILA HIZEM and ADEL KALBOUSSI

Laboratoire de Microélectronique et Instrumentation (LR13ES12), Faculté des Sciences de Monastir, Avenue de l'environnement, Université de Monastir, 5019 Monastir, Tunisie

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Abstract. In this paper the electrical characteristics of metal–insulator–semiconductor (MIS) and metal–insulator–semiconductor–insulator–metal (MISIM) capacitors with (100)-oriented p-type silicon as a substrate under different high- k gate dielectrics (SiO_2 , HfO_2 , La_2O_3 and TiO_2) are investigated in the semi-classical and quantum mechanical models. We review the quantum correction in the inversion layer charge density for p-doped structures. The purpose of this paper is to point out the differences between the semi-classical and quantum mechanical charge descriptions at the insulator–semiconductor interface and the effect of the type of oxide and their position (gate oxide or buried oxide) in our structures. In particular, capacitance–voltage (C – V), relative position of the sub-band energies and their wavefunctions are studied to examine qualitatively and quantitatively the electron states and charging mechanisms in our devices. We find that parameters such as threshold voltage and device trans-conductance are enormously sensitive to the proper treatment of quantization effects.

Keywords. Nanotechnology; MIS device; MISIM device; quantum-mechanical model; semi-classical model; metal gate.

1. Introduction

Nowadays, the characteristics of metal-oxide-semiconductor (MOS) devices are extensively influenced by quantum mechanical (QM) effects due to the aggressive complementary metal-oxide-semiconductor (CMOS) scaling. As the gate oxide thickness is scaled down to only a few atomic layers, quantum-confinement effects have a strong influence on the threshold voltage and the gate capacitance [1].

The reduction of the gate oxide thickness is necessary to maintain an acceptable scaling of MOS transistor dimensions and high capacitance [2] in future generation integrated circuits. Caused by the occurrence of high level direct tunnelling currents, we are approaching the limits in reducing silicon dioxide (SiO_2) gate thickness [3].

Therefore, to attain a large current drive in a MOS, a large interfacial layer capacitance is required. Thus, tunnel current can flow between gate and substrate on reducing the thickness of the gate oxide to a few nanometres. The solution used to increase interfacial layer capacitance without generating excess gate current is to use materials other than SiO_2 as the dielectric gate [4]. The alternative to SiO_2 is the high dielectric constant (high- k) materials [5]; these materials have a high dielectric constant value, compared with SiO_2 . That is, the high-dielectric-constant oxides such as titanium dioxide (TiO_2), lanthanum oxide (La_2O_3) and hafnium oxide (HfO_2) offer MOS gate dielectric electronic applications.

Future CMOS technology nodes will require the introduction of these alternative high- k dielectrics, which appear at present as the most appropriate candidate.

In order to get the high-density integration of MOS devices, it is obligatory to reduce the gate oxide thickness and increase the substrate doping concentration. This results in a narrow and deep potential well in which electrons are confined at the semiconductor–insulator interface and it becomes necessary to take quantum mechanical (QM) effects into consideration [6].

Under such conditions, quantum effects in the inverted channel of MOSFET become important and strongly influence the device behaviour and performance [7]. Modelling of MOS devices is usually performed using drift diffusion algorithms and much work about the classical model has been described in references [8,9]. Several commercial simulators based on such classical approach exist. According to the National Technological Roadmap for Semiconductors (NTRS) [10], metal/high- k gate stacks have been implemented in the most recent technology generated in order to allow scaling of the EOT, consistent with the overall transistor scaling while keeping gate leakage currents within tolerable limits. The scaling tendency for gate dielectrics is such that for sub-100 nm generation device, an equivalent gate oxide thickness of less than 3.0 nm will be required [11]. The combination of thin gate dielectrics and high level gate bias results in a deep sub-micron ($<0.25 \mu\text{m}$) MOS device in large transverse electric fields at the interface. When the transverse electric fields become large enough to cause the formation of a 2-D electron (or hole) gas, the

* Author for correspondence (hlalislh@yahoo.fr)

modelling of QM effects becomes very important. In such context, the consideration of quantum effects has been obtained via a one-dimensional solution of Schrodinger's equation on a section of the channel perpendicular to the gate contact [12,13]. However, it is not precise enough to predict the performance of nano-devices [14]. At the nanometre size, highly developed tools are necessary to describe the wave nature of electrons and quantum effects like energy quantization.

In this work, quantum correction in the inversion layer charge density calculation has been studied. Calculations are carried out for both metal–insulator–semiconductor (MIS) and metal–insulator–semiconductor–insulator–metal (MISIM) structures with (100)-oriented p-type silicon as substrate. The oxide thickness T_{ox} is 1 nm and uniform doping profile is used for the silicon layer ($1 \times 10^{18} \text{ cm}^{-3}$). The Fermi–Dirac distribution and the standard effective-mass approximation in a parabolic band are assumed. In what follows, we will describe the operation of MIS and MISIM capacitors by assuming both semi-classical and quantum mechanical charge distribution. When the charge is treated semi-classically, only 1D Poisson equation needs to be solved. When the charge in the triangular quantum well is treated quantum mechanically, self-consistent solution of the 1D Poisson and Schrödinger equations has to be found.

The objective of this paper is to examine some basic concepts for MOS capacitors with high- k dielectric materials to fabricate devices with reliable and high-quality characteristics. The differences between the semi-classical and QM charge description at the interface are investigated. In this example, we will examine MIS and MISIM capacitors with the following properties: the gate is made of metal with a work function equal to the silicon affinity; the gate dielectric materials are SiO_2 , HfO_2 , La_2O_3 and TiO_2 with p-type silicon as substrate.

In this context, we have studied some electronic properties of our MIS device in a semi-classical and a QM model using different gate insulators. However, so far there are only a few theoretical studies of quantum confinement effects (QCEs) for high- k materials in the literature. In particular, capacitance–voltage (C – V), relative position of the sub-band energies and their wavefunctions are used to examine qualitatively and quantitatively the electron states and charging mechanisms in our structure. While most of the published studies on similar systems concentrate mainly on the C – V measurements, the highlighting here is on the energies and wavefunctions, which are found to be more sensitive to some aspects of carrier exchange mechanisms and permit acquiring additional information that cannot be accessed through capacitance measurements alone.

2. MIS and MISIM capacitors and their characteristics

For the correct description of charge quantization in MOS capacitors, we will just focus on solving the Schrodinger–Poisson problem. This can be achieved with SCHRED

Figure 1. A schematic representation of the studied structures (a) MIS and (b) MISIM.

First Generation tools that are installed on the Network for Computational Nanotechnology. Good understanding of the quantum mechanical size quantization effects in device simulators is achieved by solving the Schrodinger–Poisson–Boltzmann problem. This approach was discussed in detail in reference [15].

The MIS and MISIM structures used in this study were made on (100) p-type substrate with carrier concentration of $1 \times 10^{18} \text{ cm}^{-3}$. A schematic representation of the studied structures discussed in this paper is shown in figure 1. Particularly, the structure analysed is shown in figure 1(b). It consists of a substrate body and two gate/insulator structures which need not be symmetrical (they can have different insulator thicknesses, surface charges, mobilities and work functions). Voltage applied to the body region is assumed to be zero. The analysis conducted is applicable to inversion-type transistors.

Capacitance–voltage (C – V) characteristics in the semi-classical and QM model of both MIS and MISIM devices are simulated at room temperature. Also, relative position of the sub-band energies and their wavefunctions are carried out.

The periodic crystal potential in the bulk of semiconducting materials is such that, for a given energy in the conduction band, the allowed electron wave vectors trace out a surface in k -space. In the effective-mass approximation for silicon, these constant-energy surfaces can be visualized as six equivalent minima of the bulk silicon conduction band split into two sets of sub-bands. One set consists of the two equivalent valleys that have the longitudinal mass perpendicular to the interface.

3. Results and discussion

3.1 MIS structure: single-gate capacitors

3.1a Metallic gate: In figure 2, we show C – V simulation carried out at room temperature for four different gate

insulators: SiO_2 ($\epsilon_r = 3.9$), HfO_2 ($\epsilon_r = 25$), La_2O_3 ($\epsilon_r = 30$) and TiO_2 ($\epsilon_r = 80$). We analyse each time the C - V characteristics in the semi-classical and QM model.

From figure 2, it is seen that in the quantum approach, the simulated capacity is less than the capacity of the semi-classical model and this due to the inclusion in the account of the thickness of darkspace. The 'darkspace' can be modelled as an additional contribution to effective gate oxide thickness [16,17].

The low-frequency C - V curve goes from accumulation through depletion towards inversion region. The threshold voltage for the semi-classical model is lower than the threshold voltage for the quantum model for all structures whatever the oxide. As a result the use of the quantum model gives rise to a threshold voltage shift of about 100 mV, which is a significant and physically justified value. The range of threshold voltage shift of a high- k (HfO_2 , La_2O_3 and TiO_2) gate dielectric is smaller than that for a SiO_2 gate dielectric [18], which can be attributed to the Fermi level pinning effect [19,20].

It is clear that the difference between the semi-classical and quantum model appears only in the inversion zone and this is connected directly to the type of substrate doping. In our case the substrate is p-doped; hence electrons are treated quantum mechanically only in the inversion area for positive voltages. As shown in figure 3, the C - V difference ($C_{\text{SC}} - C_{\text{QM}}$) in inversion region increases with increasing oxide dielectric permittivity. We have found that at a fixed oxide thickness (1 nm), TiO_2 has the highest percentage. The degradation of quantum capacitance in an inversion region as verified by reference [21] can be accounted for by using effective oxide thickness ($T_{\text{eff}} > T_{\text{ox}}$). This indicates that the QCEs should cause $\approx 12\%$ error of thickness [22]. This degradation is almost constant because our gate is a metal. The average distance of the carriers from the insulator-semiconductor interface ($x = 0$) is bigger in the QM case; this leads to a reduction of the inversion layer capacitance and degradation of device trans-conductance.

Figure 2. Semi-classical (blue) and quantum model (red) capacitance vs. voltage for different gate insulators: SiO_2 , HfO_2 , La_2O_3 and TiO_2 for PMIS structure.

As shown in figure 3, the percentage difference in the inversion zone between the semi-classical and quantum model is higher for TiO₂ oxide. This proves that for the same physical thickness of 1 nm, the effective thickness for TiO₂ in the quantum approach is more than those of the others oxides.

We have used the high-permittivity (titanium oxide: TiO₂) layer to control the flat-band voltage V_{FB} of p-type metal-oxide-semiconductor field effect transistors [23]. Also, many researchers have focused on TiO₂ thin film as an attractive candidate to replace SiO₂ thin film because of its high dielectric constant (80). Nevertheless, TiO₂ thin film has a weak point such as relatively large leakage current due to its small bandgap (3.5 eV) energy and a low band offset with silicon (1.2 eV) [24].

In table 1 we present the values of some important properties of high- k dielectric materials.

In what follows, we will describe the operation of NMIS capacitors by assuming both semi-classical and QM charge distributions as shown in figure 4.

In the NMIS structure case, the quantum phenomenon on the C - V characteristic appears only in the accumulation region for negative voltages. As a result, if the bulk is n-type silicon, holes are treated quantum mechanically in the accumulation range.

This threshold voltage shift must be taken into account in the design of ultra-thin body device [25]. Therefore, the

Figure 3. Difference percentage between the semi-classical and quantum model capacitance in the inversion zone for different gate insulators: SiO₂, HfO₂, La₂O₃ and TiO₂.

Table 1. Values of some important properties of high- k dielectric materials.

Material	Dielectric constant	Energy gap, E_g (eV) to Si (eV)	Conduction band offsets
SiO ₂	3.9	8.9	3.2
HfO ₂	25	5.7	1.5
La ₂ O ₃	30	4.3	2.3
TiO ₂	80	3.5	1.2

classical threshold condition should be modified to $\psi_s = 2\psi_B + \Delta\psi_s^{QM}$ as mentioned by Ku *et al* [26], where

$$\Delta\psi_s^{QM} = \frac{KT}{q} \ln \left(\frac{Q_i(\psi_s = 0)}{Q_i^{QM}(\psi_s = 0)} \right). \quad (1)$$

Here Q_i , the total inversion charge density by the classical manner per unit area, is expressed as

$$Q_i = \frac{KTn_i^2}{E_s N_{body}}, \quad (2)$$

where E_s is the electric field at the interface given by $E_s = \frac{qN_{body}T_{si}}{\epsilon_{si}}$, and N_{body} is the doping concentration at the edge of the depletion layer.

Q_i^{QM} , the total inversion charge corrected by quantum confinement per unit area, is expressed as

$$Q_i^{QM} = \frac{4\pi qKT}{h^2} \left(g_m \sum_j \ln \left(1 + e^{\frac{E_f - E'_c - E_f}{KT}} \right) + g'_m \sum_j \ln \left(1 + e^{\frac{E_f - E'_c - E_f}{KT}} \right) \right), \quad (3)$$

where g and g' are the numbers of degeneracy, m_d and m'_d are the density of states effective masses and $E_f - E'_c$ is the difference between the Fermi level and the bottom of the conduction band at the interface (figure 5).

Assuming that only the ground state is occupied by electrons, equation (1) becomes

$$\Delta\psi_s^{QM} \approx \frac{E_0}{q} - \frac{KT}{q} \ln \left(\frac{8\pi qm_d E_s}{h^2 N_V} \right). \quad (4)$$

For NMOS, N_V is simply replaced by N_c , and the sign and the effective mass in equation (4) is changed. Note that the ground energy state plays a crucial role in finding the surface potential change by the quantum confinement effect. The ground energy state is powerfully influenced by the potential form. Finally, the expression of threshold voltage in the case of quantum mechanical model for PMOS and NMOS is given by

$$\begin{aligned} \Delta V_{th}^{QM} &= \frac{dV_g}{d\psi_s} \Delta\psi_s^{QM} \\ &= \left(1 + \frac{3T_{ox}}{T_{si}} \right) \left[\pm \frac{E_0}{q} \pm \frac{KT}{q} \ln \left(\frac{8\pi qm_d E_s}{h^2 N_c} \right) \right]. \end{aligned} \quad (5)$$

The sub-band and the Fermi energy variation as functions of gate voltage in (100) silicon substrate from both unprimed ($\Delta 2$) and primed ($\Delta 4$) ladder of sub-bands with four gate insulators is presented in figure 6. From this result, we study two clearly pronounced characteristics: high value for the sub-band energies and increased sub-band separation obtained because of the narrowing of the triangular potential. With increasing gate bias, we move into the electronic quantum limit in which most of the carriers stay in the ground sub-band of the unprimed ($\Delta 2$) ladder of sub-bands [21].

Figure 4. Semi-classical (blue) and quantum model (red) capacitance vs. voltage for different gate insulators: SiO₂, HfO₂, La₂O₃ and TiO₂ for NMIS structure.

Figure 5. Difference between semi-classical and quantum-mechanical capacity in the accumulation region for different gate insulators.

For (100) orientation of the interface, the carriers have light mass in the transport direction and subsequently increased electron mobility.

The channel potential could be approximated as an infinite triangular well [27]. The substrate dielectric is approximated as an infinite potential barrier and the slope of the potential in the substrate is defined by the electric field at the interface. After that the magnitudes of the bound-state eigenenergies relative to the band edge could be obtained as

$$E_i \approx \left(\frac{\hbar^2}{2m^*} \right)^{1/3} \left[\frac{3}{2} \pi e F_s \left(i + \frac{3}{4} \right) \right]^{2/3}, \quad (6)$$

using Airy functions with negligible difference as compared to numerical calculations. Here, m^* is the quantization effective mass and i labels the eigenstate with $i = 0$ corresponding to the ground state.

Primed or unprimed sub-band energies are described at the interfaces SiO₂–Si, HfO₂–Si, La₂O₃–Si and TiO₂–Si and more precisely in the triangular quantum wells as shown

Figure 6. Relative position of the sub-band energies with respect to the Fermi level E_F vs. applied gate bias for different gate insulators.

Figure 7. Energy band diagrams of the metal/high- k /p-Si structure where the notation E_{ij} (i : band, j = sub-band) refers to the j th sub-band from either the $\Delta 2$ -band ($i = 1$) or $\Delta 4$ -band ($i = 2$). In our case, for $\langle 100 \rangle$ orientation of the surface, the $\Delta 2$ -band has the longitudinal mass (m_l) perpendicular to the semiconductor interface and the $\Delta 4$ -band has the transverse mass (m_t) perpendicular to the interface.

in figure 7. We observe that the Fermi level is higher than the first sub-band for positive voltage; for this reason the semiconductor is degenerate.

In the case of the QM model we have taken 4 sub-bands from the unprimed ladder of sub-bands and 2 sub-bands from the primed ladder of sub-bands. The spatial variation of the corresponding wavefunctions is shown in figure 8. We observed the delocalization of the electron wavefunction at the insulator–silicon interface [28]. This delocalization

of the electron wavefunction at the interface between high- k and semiconductor has been confirmed in references [29,30].

From the results shown in figure 8, we can deduce several important things. The shape of the wavefunctions resembles Airy functions that are the solution to the 1D Schrodinger equations with linear potential energy term as mentioned in reference [31]. From figures 6 and 7 we notice that the minimum energy band in the quantum well whether with primed

Figure 8. Spatial wavefunctions for MIS structure with different gate insulators corresponding to the lowest 2 sub-bands from the primed ($\Delta 4$) ladder of sub-bands, and wavefunctions corresponding to the lowest 4 sub-bands from unprimed ($\Delta 2$) ladder of sub-bands.

Figure 9. Maximum of wavefunction for both primed and unprimed sub-band in MIS structure for different gate insulators.

or unprimed ladder of sub-bands corresponds to the highest amplitude wavefunction. Then, if we compare the first two wavefunctions from both the unprimed and primed ladder of sub-bands, we see that the unprimed wavefunctions are more squeezed as the energies are lower and for those energies (see figure 6) the well is squeezed; therefore there exists larger localization of the carriers. We also noticed that the first wavefunction has zero intersections with the x -axis, the second one has one, the third one has two, etc. The wavefunctions have a maximum in the case of primed or unprimed sub-band as shown in figure 9; this maximum depends on the nature of the existing oxide between the metal and the semiconductor and shifts with the distance.

3.1b Polysilicon gate: Now we consider a simple MIS capacitor, where the gate is made of p+ polysilicon. The thickness of different gate insulators is $T_{ox} = 1$ nm and the doping of the p-type substrate is $N_A = 1 \times 10^{18} \text{ cm}^{-3}$.

Figure 10. Influence of poly-gate depletion on the MIS structure in the semi-classical (blue) and quantum model (red) for different gate insulators: SiO₂, HfO₂, La₂O₃ and TiO₂.

Figure 11. C - V characteristics for four different p-doped semiconductors ($N_A = 1 \times 10^{18} \text{ cm}^{-3}$) with an HfO_2 gate dielectric layer of 1 nm.

The doping value of the polysilicon gate is equal to $N_A = 1 \times 10^{20} \text{ cm}^{-3}$. The C - V characteristics with a polysilicon gate at different gate dielectrics for semi-classical and QM approach are shown in figure 10.

We are therefore interested in a p-type polysilicon, which may limit boron diffusion through the structure and minimize gate depletion while keeping the benefits of polysilicon, such as the self-alignment of the gate zones, low resistivity and adjustment of the Fermi level.

The use of low- k dielectric materials as gate insulators reduces efficiency of an MIS in terms of current, threshold voltage and sub-threshold swing; hence high- k gate dielectric materials are much preferred with proper optimizations.

The currently proposed solutions consist of replacing the polysilicon by a metal, whose work function is appropriate for the type of the gate electrode. However, this return to metal gate poses two problems: first, it does not solve the problem of instability of the threshold voltage of the transistor. Secondly, the introduction of metallization induces a complexity and a higher cost to the realization.

The gate depletion corresponds to the area of the space charge in the polysilicon gate at the interface with the gate oxide. Certainly, the gate is not completely degenerate at its interface with the oxide; hence there is an energy band bending under an external bias. This desertion by the carriers corresponds to the existence of a negative image charge related to the depletion of the gate material and channel side inversion regime. This negative charge compensates the positive charge substrate side (+ poly_p case and sub_p).

Desertion area is larger when the doping of the grid is low. This area is equivalent to a capacitance that is added in series with the surface capacitance C_{ox} gate oxide, also reducing the total equivalent capacitance C_{tot} , which is given by

$$C_{\text{tot}} = \frac{\epsilon_{\text{ox}}}{T_{\text{ox}} + \frac{\epsilon_{\text{ox}}}{\epsilon_{\text{Si}}} T_{\text{poly-dep}}} \quad (7)$$

During inversion, in the QM model, there is about 10% degradation of the total gate capacitance. In accumulation,

if the gate is metal, the capacitance degradation is almost constant and can be accounted for by using effective oxide thickness. In the case of a poly-gate, the low-frequency capacitance in accumulation conditions has pronounced gate voltage dependence and the total gate capacitance C_{tot} increases with increasing V_G .

In the accumulation region, the tendency of C - V characteristic is changed by changing the nature of the oxide. Indeed, with increasing permittivity of the oxide, the portion of the C - V curve in the accumulation region is hollow, from which the C - V curve increases again to the accumulation.

Table 2. Main physical parameters of IV (Si)- and III-V (GaAs, InAs and CdTe)-type semiconductors used for MIS device simulation.

Physical parameters (300 K) [32–34]									
Semiconductors	E_g (eV)	$\varepsilon/\varepsilon_0$	χ (eV)	n_i (cm $^{-3}$)	N_c (cm $^{-3}$)	N_v (cm $^{-3}$)	μ_e (m 2 V $^{-1}$ s $^{-1}$)	μ_h (m 2 V $^{-1}$ s $^{-1}$)	Band offsets for HfO $_2$ on each semiconductor
IV									
Si	1.12	11.8	4.05	1.15×10^{10}	3.24×10^{19}	3.11×10^{19}	1350	450	1.48
GaAs	1.424	13.2	4.07	2.15×10^6	3.97×10^{17}	9.73×10^{18}	8500	400	1.51
III-V									
InAs	0.354	12.3	4.9	1.02×10^{15}	1.37×10^{17}	6.69×10^{18}	33000	460	2.48
CdTe	1.5	10.9	4.28	2.51×10^{-13}	1	1	1050	100	—

Figure 12. Total gate capacitance of MISIM structure (with a DG capacitor and double oxides (gate oxide and buried oxide)) in the semi-classical (blue line) and quantum-mechanical charge model (red line).

In order to study the influence of the semiconductor in the semi-classical and quantum charge model on the C - V behaviour of our MIS device, we illustrate C - V response of various MOS structures based on high-mobility semiconductors. Hence, in figure 11, we compare the two models for low-frequency curves in four different p-doped substrate types: Si, GaAs, InAs and CdTe. Here, we fixed the HfO_2 as a high- k insulator and the gate is a polysilicon gate that is p+ doped ($N_A = 1 \times 10^{20} \text{ cm}^{-3}$). The main material parameters used in simulations are presented in table 2.

3.2 MISIM structure: dual gate capacitor

Today there is an extensive research in double-gate (DG) structures, and FinFET transistors, which have better electrostatic integrity and theoretically have better transport properties than single-gated FETs. It is difficult to find a single dielectric that satisfies all the requirements for end-of-roadmap MOS gate dielectrics (high dielectric constant, low interface trap density, high thermal stability, etc.); hence these bilayer gate dielectrics are an interesting option [35].

In this part, we reflect on a DG capacitor. The gate is a metal with the value of the metal work function equal to 4.05 eV, the thickness of the front and back high- k layers is $T_{\text{ox}} = 1 \text{ nm}$ and the doping of the p-type substrate is $N_A = 1 \times 10^{18} \text{ cm}^{-3}$. For this device structure, using both semi-classical and quantum mechanical charge model we examine both the difference of the total gate capacitance as a function of the charge model for different oxides and the shift in the threshold voltage with substrate (body) thickness.

Low-power applications require dynamic control of the threshold voltage (V_{th}) to control simultaneously power and performance. A potential solution is the back-gate biasing that modifies V_{th} due to the body effectively. However, few works deal with this effect on multi-gate MOSFETs [36,37].

As shown in figure 12, similar to single-gate capacitors, the use of the quantum model leads to increase of the average distance of the carriers from the interface and degradation of the total gate capacitance for both positive and negative gate bias. The back gate voltage was set to -2 V in these simulations. The more pronounced quantum mechanical nature of the charge transport in the DG capacitors with smaller body thickness leads to larger shift in the threshold voltage.

We observe that QM effects lead to an important decrease of the capacitance in accumulation and inversion regimes due to the reduction of free carrier concentrations in the semiconductor film [38]. The quantum confinement is larger with decreasing T_{ox} ; in this case, the vertical electric field increases, which induces a deeper potential well. This increases the carrier confinement.

In low dimension, quantum confinement induces a significant increase of the threshold voltage (absolute value), resulting in a strong impact on the accurate evaluation of the equivalent oxide thickness (EOT) and of the threshold voltage [39,40]. The extracted EOT may be overestimated, if

quantum confinement is not considered in the extraction of the EOT value from the measured characteristics.

4. Conclusion

In summary, a sandwich single- and double-gate vertical tunnel field effect transistors are proposed and simulated. We theoretically investigate the differences between the semi-classical and QM charge description at the interface: high- k /Si-(100) orientation for MIS and MISIM. To examine qualitatively and quantitatively the electron states and charging mechanisms in our devices, C - V and relative position of the sub-band energies and their wavefunctions are studied. C - V characteristics in the semi-classical and QM model of both MIS (metal and polysilicon gate) and MISIM devices are simulated at room temperature with SiO_2 and alternative high- k dielectrics like HfO_2 , La_2O_3 and TiO_2 . Also, relative positions of the sub-band energies and their wavefunctions are determined. In the quantum approach, the simulated capacity is less than the capacity of the semi-classical model and this due to the inclusion in the account of the thickness of darkspace. It is clear that the difference between the semi-classical and quantum model appears only in the inversion or in the accumulation zone and this is connected directly to the type of substrate doping. If the substrate is p-doped, electrons are treated quantum mechanically only in the inversion area for positive voltages. We have found that at a fixed oxide thickness (1 nm), TiO_2 has the highest percentage of the C - V difference ($C_{\text{SC}} - C_{\text{QM}}$) in inversion region. In the QM case, the average distance of the carriers from the insulator-semiconductor interface is bigger and this leads to a reduction of the inversion layer capacitance and degradation of device trans-conductance.

Primed or unprimed sub-band energies are described at the interfaces SiO_2 -Si, HfO_2 -Si, La_2O_3 -Si and TiO_2 -Si and more precisely in the triangular quantum wells. Higher value for the sub-band energies and increased sub-band separation are obtained because of the narrowing of the triangular potential. By increasing the gate bias, we move into the electronic quantum limit in which most of the carriers stay in the ground sub-band of the unprimed (Δ_2) ladder of sub-bands. The wavefunctions have a maximum in the primed or unprimed sub-band; this maximum depends on the nature of the oxide localized between the metal and the semiconductor.

For DG capacitor, we observe that QM effects lead to an important decrease of the capacitance in accumulation and inversion regimes due to the reduction of free carrier concentrations in the semiconductor film.

Finally, the quantum-confinement effects have a strong influence on the threshold voltage and the nature of the gate capacitance for MIS and MISIM devices.

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