Series-connected substrate-integrated lead-carbon hybrid ultracapacitors with voltage-management circuit

A BANERJEE^{1,*}, R SRINIVASAN² and A K SHUKLA¹

¹Solid State and Structural Chemistry Unit, Indian Institute of Science, Bangalore 560 012, India

²enArka Instruments, Bangalore 560 040, India

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Abstract. Cell voltage for a fully charged-substrate-integrated lead-carbon hybrid ultracapacitor is about 2.3 V. Therefore, for applications requiring higher DC voltage, several of these ultracapacitors need to be connected in series. However, voltage distribution across each series-connected ultracapacitor tends to be uneven due to tolerance in capacitance and parasitic parallel-resistance values. Accordingly, voltage-management circuit is required to protect constituent ultracapacitors from exceeding their rated voltage. In this study, the design and characterization of the substrate-integrated lead-carbon hybrid ultracapacitor with co-located terminals is discussed. Voltage-management circuit for the ultracapacitor is presented, and its effectiveness is validated experimentally.

Keywords. Ultracapacitor; substrate-integrated lead-dioxide electrode; voltage-management cell-balancing circuit.

1. Introduction

The recognition that carbon added in small amounts into the negative plate of lead-acid batteries resists accumulation of lead sulphate¹ and its subsequent partial or total replacement with a carbon-coated plate has led to a new class of energy-storage devices, namely, ultrabattery^{2,3} and lead-carbon asymmetric ultracapacitor,^{1,4} respectively. Substrate-integrated lead-carbon hybrid ultracapacitor is a type of lead-carbon asymmetric ultracapacitor.⁵ Typical cell voltage for a substrate-integrated lead-carbon hybrid ultracapacitor is about 2.3 V. Therefore, for applications requiring energy storage at higher DC voltage, several of these hybrid ultracapacitors with similar capacitance values need to be connected in series. It is noteworthy that voltage distribution in the series string is determined by the individual capacitance and its internal parallel-resistance value; the latter causes charge leakage in the ultracapacitor and reduces its operational voltage.

In practice, both capacitance and internal-resistance values can vary for ultracapacitors and from one production batch to another due to manufacturing process tolerance.^{6–8} The manufacturing tolerance in capacitance value of $\pm 20\%$ is quite common. For example, consider two similar ultracapacitors, namely C_1 and C_2 , of nominal capacitance value, C is same, connected in series, and assume that C_1 is at -20% of its nominal value, i.e., $0.8C$, and C_2 is at $+20\%$ of its nominal value, i.e., $1.2C$. As the charge, Q , on both the ultracapacitors is same; the voltage distribution on C_1 and C_2 is given by Eqs (1) and (2), respectively.

$$V_1 = \frac{Q}{0.8C}, \quad (1)$$

$$V_2 = \frac{Q}{1.2C}. \quad (2)$$

If the total voltage applied across the ultracapacitors is 4.6 V, then the voltage distribution due to tolerance in their respective capacitance values is such that: $V_1 = 2.76$ V and $V_2 = 1.84$ V. Clearly, ultracapacitor C_1 is operating beyond its maximum rated voltage of 2.3 V. This can result in reduced life and early failure of the ultracapacitor, and can affect the reliability of the overall system. Therefore, in practice, voltage-management circuitry is almost always used in a series-connected ultracapacitor string to achieve uniform distribution of voltage across each ultracapacitor.

In general, two different voltage-management schemes are employed for series-connected ultracapacitors, namely (a) active-balancing scheme (DC-to-DC power converter) and (b) passive-balancing scheme. In an active-balancing circuit, charge transfer occurs from ultracapacitors having higher voltage to ultracapacitors with lower voltage until voltage across all ultracapacitors is balanced. Although the energy efficiency of active balancing schemes is high, they are not cost-effective. By contrast, passive schemes balance the voltage by using resistors and semiconductor switches to dissipate excess energy from ultracapacitors that are charged to higher voltage. It is noteworthy that passive schemes, although less efficient, are cost-effective.

In this communication, we discuss design, fabrication and experimental validation of a passive voltage-management circuit for a series-connected ultracapacitor string comprising six 2 V/1500 F substrate-integrated lead-carbon hybrid ultracapacitors. The passive voltage-management circuit is employed for this series arrangement, and its performance is validated experimentally.

*Author for correspondence (anjansc.ac@gmail.com)

2. Experimental

2.1 Development of substrate-integrated lead-carbon hybrid ultracapacitor

Details on the development of substrate-integrated lead-carbon hybrid ultracapacitors are presented elsewhere.^{5,9–16} In brief, substrate-integrated lead-dioxide-positive electrodes were obtained by immersing 99.9% pure etched lead sheets in 6 M aqueous sulphuric acid. Thin layer of lead sulphate thus formed on the surface of the lead sheet was electrochemically oxidized to form lead dioxide. Activated carbon-coated-negative electrodes were fabricated using dimethyl formamide as a solvent, and 5 wt% poly(vinylidene fluoride) as a binder. This mixture was then blended with 85 wt% of Meadwestvaco X-090177 activated carbon (US) and 10 wt% of activated charcoal (from SD Fine-Chem, India) to form an ink. The carbon ink thus formed was applied onto the iso-statically compressed graphite substrates (current collectors). The electrodes were dried in an air-oven at 80°C for 6 h.

A 2 V/1500 F ultracapacitor was constructed by alternatively stacking nine positive and eight negative electrodes in a plastic enclosure, with 0.5 mm-thick polyethylene mesh separators and polymeric silica gel with 1.4 g cm⁻³ aqueous sulphuric acid as electrolyte followed by group connecting the positive and negative electrodes in parallel. Subsequently, 12 V/250 F ultracapacitor was fabricated by connecting six 2 V/1500 F ultracapacitors in series. A schematic diagram of 12 V ultracapacitor monoblock having co-located terminals is shown in figure 1, with constituent 2 V ultracapacitor cell numbered as Cell-1 through Cell-6.

Each of the individual ultracapacitor and the bank of six series-connected ultracapacitors were then characterized by various electrochemical DC and AC test protocols using Bitrode Instrument and Autolab Potentiostat/Galvanostat-Model 30, respectively. All the experiments were carried out at room temperature (~28°C).

2.2 Design of voltage-management cell-balancing circuitry

A passive voltage-management-circuit implementation for each of the 2 V/1500 F ultracapacitor is depicted in figure 2a.

Figure 1. Schematic representation for 12 V substrate-integrated lead-carbon hybrid ultracapacitor monoblock comprising six 2 V cells connected in series with co-located terminals.

Circuit description is as follows. The integrated circuit, U1, is an ON semiconductor part (NCP301LSN22T1G) and essentially comprises: (a) 2.2 V precision-voltage reference, (b) a voltage comparator with about 100 mV hysteresis and (c) an open-drain Metal-Oxide Silicon Field Effect Transistor (MOSFET). Figure 2b depicts the block schematic representation of U1. Positive terminal of the ultracapacitor was connected to the input (Pin-2) terminal of U1 and the negative terminal was connected to the ground (Pin-3) terminal of U1. The open-drain pin (Pin-1) of U1 was pulled-up to the positive terminal of the ultracapacitor using a 5.1 K resistor. Output pin (Pin-1) of U1 drives a NPN Bipolar Junction Transistor (BJT) in the switching mode (ON/OFF mode). Collector of BJT was pulled-up to the positive terminal of the ultracapacitor using a 15 Ω /1 W power resistor.

3. Results and discussion

3.1 Performance data for substrate-integrated lead-carbon hybrid ultracapacitor

3.1a Capacitance: Series-connected ultracapacitor string is first charged in constant-current mode until the voltage reaches 13.8 V. Subsequently, the ultracapacitor voltage is maintained at 13.8 V in constant-voltage mode for 1 h. The series string is then discharged up to 6 V at varying constant-current loads between 0.3 and 1.5 A. For each of the discharge currents, the voltage slope is obtained from the voltage-time discharge curve, and the capacitance value is calculated by dividing the discharge current with the corresponding voltage slope.¹⁷ The same method is used for obtaining the capacitance values for the other constituent ultracapacitors in the string. Appreciable variation in the capacitance values for individual ultracapacitors is clearly manifested in table 1. This variation in a series-string arrangement is also attributed to nonuniform current distribution owing to the physical location of individual ultracapacitor with respect to the device terminals.¹⁸ In the present co-located terminal arrangements (see figure 1), Cell-1 is physically closer to the positive terminal and Cell-6 is physically closer to the negative terminal of the 12 V ultracapacitor monoblock.

3.1b Faradaic efficiency: Faradaic efficiency for the 12 V ultracapacitor is obtained to be as 89% from constant-current charge/discharge data. In doing so, the current is set at 0.3 A, and the ultracapacitor is charged up to 13.8 V and discharged down to 6 V. This corresponds to a voltage window of 2.3–1 V at the individual ultracapacitor level. The charge/discharge profiles for constituent cells are shown in figure 3a, and the respective faradaic-efficiency data are summarized in table 1. As can be seen from table 1, there is a marginal variation in faradaic efficiency from one ultracapacitor to another within the series string.

Figure 2. (a) Voltage-management cell-balancing circuit for a 2.3 V/1500 F substrate-integrated lead-carbon hybrid ultracapacitor and (b) block schematic representation for U1 (NCP301LSN22T1G).

Table 1. Performance imbalance studies for constituent 2 V cells of 12 V substrate-integrated lead-carbon hybrid ultracapacitor (HUC).

	12 V HUC	Cell-1	Cell-2	Cell-3	Cell-4	Cell-5	Cell-6
Capacitance (F)							
0.3 A	268	1327	1374	1636	1680	1811	1827
0.6 A	255	1298	1578	1540	1578	1722	1736
0.9 A	239	1261	1420	1365	1419	1550	1558
1.2 A	222	1126	1319	1254	1320	1438	1446
1.5 A	208	1056	1236	1165	1236	1348	1350
Faradaic efficiency (%)	89	89	88	90	89	88	90
Internal resistance (mΩ)	120	19.6	17.2	21.3	21.0	17.3	22.1
Voltage-loss over 24 h (%)	15.50	15.35	15.37	15.38	15.39	15.40	15.54

3.1c Internal resistance: Internal-resistance values for the constituent ultracapacitors are obtained using AC impedance technique. The X-intercept (Z'/Ω) value at high-frequency region in the Nyquist plot gives the internal-resistance value.¹⁷ Internal-resistance values for constituent ultracapacitors are measured at 2 V state-of-charge. Nyquist plots for an individual cell are shown in figure 3b, and the internal-resistance data are presented in table 1. Substantial variations in slopes, which are modelled as Warburg diffusion elements, at lower frequency region of Nyquist plots for different cells are observed along with the varying internal-resistance values from one cell to another.

3.1d Self-discharge: Self-discharge voltage-loss behaviours for constituent 2 V ultracapacitors differ due to the voltage imbalance among them as presented in table 1. As explained earlier, voltage imbalance is caused due to tolerance in capacitance and internal parallel-resistance values. Self-discharge voltage-loss data are collected over 24 h for the constituent ultracapacitors. Self-discharge voltage-loss characteristics depend on the thermal randomization of electrical double-layer structure and parasitic faradaic reactions. According to the electrical model, the self-discharge voltage-loss is on account of the leakage current flow through the internal parallel resistance. Leakage current and internal

Figure 3. (a) Constant-current charge/discharge profiles and (b) Nyquist plots at 2 V for constituent ultracapacitor cells in series string.

parallel-resistance values vary from one cell to another, due to the variation in electrical double-layer structures and nature of faradaic parasitic reactions.

3.2 Voltage management for series-connected substrate-integrated lead-carbon hybrid ultracapacitors

Under normal operation, when the ultracapacitor is charged to less than 2.3 V, the output pin (Pin-1) of U1 is low, and hence the BJT is OFF and no power loss is seen on 15 Ω resistor. If the ultracapacitor is subjected to charging to a voltage greater than 2.3 V, the voltage comparator within U1 will turn OFF and the open-drain MOSFET will turn ON the BJT. The 15 Ω resistor is now applied across the ultracapacitor draining about 150 mA of current and thus limiting further voltage rise. In realizing the 12 V/250 F ultracapacitor, the aforementioned circuit is repeated six times.

The ultracapacitor with the voltage-management circuit is tested, and the data are summarized in figure 4. It is

Figure 4. Balancing of constituent-cell voltages by applying voltage-management circuitry. The inset shows voltage vs. time profile for 12 V hybrid ultracapacitor.

clearly seen that in steady state, the voltage tends to distribute uniformly across the individual ultracapacitor in the series arrangement.

4. Conclusions

Construction of a 12 V/250 F substrate-integrated lead-carbon hybrid ultracapacitor employing polymeric silica-gel electrolyte by connecting six 2 V/1500 F ultracapacitors in series with voltage-management cell-balancing circuit is described. Uneven voltage distribution across the series-connected ultracapacitors is explained to be due to the tolerance in capacitance and parasitic parallel-resistance values of the ultracapacitors. Need for a voltage-management circuit to limit the voltage across each of the ultracapacitors within its rated voltage is established. Implementation of a passive voltage-management circuit is discussed. The performance of voltage-management circuit is experimentally validated in enhancing the overall reliability of the series arrangement.

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