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Hybrid orientation technology and strain engineering for ultra-high speed MOSFETs

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Abstract. **We report here RF MOSFET performance in sub-45-nm hybrid orientation CMOS technology. Based on the combination of hybrid orientation technology (HOT) and process-induced local strain engineering, MOSFET RF performance is investigated using CAD (TCAD) technology. Transistor optimization on (100) substrate via silicon nitride (Si_3N_4) cap layer thickness for *n*-MOSFETs, Ge mole fraction optimization for *p*-MOSFETs on (110) substrates and channel length scaling have resulted in record RF performance, viz. the cut-off frequency, f_T.**

Keywords. **Hybrid orientation technology; technology CAD; process-induced strain; CMOS integrated circuits; mobility; strained-Si.**

1. Introduction

Scaling of Si CMOS devices beyond 45 nm technology node will require performance boosters in order to meet the International Technology Roadmap for Semiconductors (ITRS) requirements for drive current (Semiconductor Industry Association 2010). Amongst the preferred near-term solutions, transport-enhanced MOSFETs utilizing strained-Si channel have shown their high potential (Maiti 2004). In order to realize high-speed scaled CMOS devices, it is very important to increase the carrier mobility. The hole mobility on (100) substrates is low and results in *p*-FET drive current typically half the value of *n*-FET. Traditionally, a larger *p*-FET size is used to balance *n*-FET drive current, which increases gate and parasitic capacitances and also large area.

It has been shown that the hole mobility on (110) surface is about two times as high as that on (100) surface (Sato *et al* 1971; Momose *et al* 2002). It has been reported that on (100) silicon substrate itself, by changing the channel direction from ⟨110⟩ to ⟨100⟩, one can improve *p*-FET performance. However, further work has focussed on alternative surface orientations, such as (110) and (111), which can provide a greater benefit for hole mobility (Yang *et al* 2003). It has also been found that hole mobility is highest on (110) surface with channel direction along ⟨110⟩, with a peak value more than twice that of a (100) surface (Yang *et al* 2004; Sheraw *et al* 2005). However, application of such a crystal orientation for the fabrication of *n*-FET is difficult. The electron mobility of (110)-surface *n*-FETs is much lower and about one half of that of (100)-surface *n*-FETs. In addition, the (110) hole mobility itself is still lower than the (110) electron mobility. This anisotropy in mobility, rather, orientation-dependent mobility engineering is now being introduced in Si CMOS technology, which is known as hybrid orientation technology (HOT).

Although above discussion qualitatively indicates the superiority of (110) channel compared to (100), quantitative comparison has not yet been reported. Mizuno *et al* (2005a, b) have developed (110)-surface strained silicon-on-insulator (SOI) *n*- and *p*-MOSFETs on (110)-surface relaxed SiGe-on-insulator (SGOI) substrates with a Ge content of 25%. For the fabrication of substrates, the Ge condensation technique was used to form SiGe layers grown on (110)-surface SOI wafers. For an overview of hybrid orientation technology, a novel approach to improve carrier mobility through wafer and channel orientation optimization, the reader may refer to the paper by Yang *et al* (2006). The authors have developed a novel planar silicon CMOS structure, based on hybrid orientation technique, comprising *n*-FETs on silicon (100) surface orientation and *p*-FETs on (110) surface orientation. HOT structures may be fabricated in various ways. Simple HOT structures may include two types of structures; type-I with *p*-FET on the (110) SOI and *n*-FET on the (100) silicon epitaxial layer and type-II with *n*-FET on the (100) SOI and *p*-FET on the (110) silicon epitaxial layer.

Currently, CMOS circuits are typically fabricated on silicon substrates with a (100) crystalline orientation due to the low oxide–interface charge density and highest electron mobility (Sato *et al* 1971; Takagi *et al* 1994; Goebel *et al* 2001). There are many issues involved in the device design and process integration for these new hybrid orientation substrates. These include device isolation, epitaxy quality and scalability. Other issues, specific to the (110) surface

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orientation, for example, are gate oxide reliability, dopant implantation, and process-induced strain effects.

Uniaxial strain engineering has become now one of the mainstream techniques to enhance performance of the nanoscale MOSFETs (IEEE 2006). Semiconductor manufacturers have successfully adopted strain engineering for the 90-nm technology node to improve transistor performance (Thompson *et al* 2004a). Local strain techniques are the favourable options due to their low cost and ease in integration. Local stress may be induced by shallow trench isolation (STI), strained-Si_3N_4 cap layers, silicidation, and SiGe or SiC pockets. A compressive strain is introduced in the *p*-MOS channel using embedded SiGe pockets in the source and drain areas. Tensile strain is introduced in the *n*-MOS channels by using a post-salicide silicon nitride cap layer.

In this paper, we propose to combine the advantages of hybrid orientation technology (HOT) and process-induced local strain engineering, as discussed above, to improve the carrier mobility (hence the performance) for both the *p*-MOSFETs (through process-induced strain, wafer and channel orientation) and *n*-MOSFETs (via Si_3N_4 stressor for local strain), respectively. This is a novel procedure because the fabrication processes are fully compatible with conventional Si CMOS technology without incorporation of any new material.

As the gate length shrinks into nanoscale regime, prediction of strain-induced performance enhancement becomes more complicated for state-of-the-art CMOS technologies, for example, the hybrid orientation technology involving process-induced strain. Therefore, in order to take full advantage of both strain engineering and HOT in nanoscale strained CMOS, it is essential to understand clearly the correlation between device structures and electrical parameters. It is the purpose of this work to extend the simulation analysis for MOSFETs realized in HOT (also employing process-induced local strain) to the sub-65 nm technology node.

Process simulations have been performed using Sentaurus Process in which strained-Si models are implemented (Synopsys Inc. 2008a). These models take into account strain induced by the lattice mismatch between silicon and $Si_{1-x}Ge_x$ layers as well as the influence of strain and presence of germanium on diffusion of dopants. The electrical characteristics of the strained-Si *n*- and *p*-MOSFETs were simulated with Sentaurus Device (Synopsys Inc. 2008b) using the strain-induced mobility models to account for the change of mobility in highly strained regions (Kanda 1982). The paper is organized as follows; in § 2, we briefly review the stress and mobility models used in simulation. Process and device simulation for benchmark device results are presented in § 3. Device optimization results are presented in § 4 and the scaling issues on f_T are discussed in § 5.

2. Modeling of stress

A typical semiconductor device consists of materials with very different mechanical behaviour. In crystalline materials, like silicon, mechanical properties vary along different crystal orientations. This type of mechanical anisotropy can result in ~30% difference in stress strain responses in silicon (Lu 1994). In semiconductor devices, the mechanical stresses are known to affect process yield and device reliability (Smeys *et al* 1999). For example, stress-induced bandgap narrowing increases junction leakage and reduces carrier mobility. Stress-induced defect generation increases the leakage currents. Interestingly, 'stress' which was so far been considered detrimental, now scaled-down devices, on the contrary, take advantage of stresses by engineering a performance-enhancing stress distribution and bandgap structure using SiGe with variable Ge content (for hole mobility enhancement) and localized Si_3N_4 layers (for electron mobility enhancement).

In the following, we briefly review the different aspects of modeling of stress on silicon fabrication processes and device behaviour. The models account for the stresses due to (i) the thermal mismatch during the temperature ramps, (ii) volume expansion, (iii) shrinkage, and (iv) lattice mismatch stress, due to the material composition and impurities in the lattice (Moroz *et al* 2003, 2004). To model crystalline anisotropy, Sentaurus Process and Device simulators employ an anisotropic elastic model following the work of Bir and Pikus (1974):

$$\sigma_i = C_{ij}\varepsilon_j, \tag{1}$$

the σ ($i = 1\ldots.6$) represents the stress components $\sigma_{xx}, \sigma_{yy}, \sigma_{zz}, \sigma_{xy}, \sigma_{xz}, \sigma_{yz}$, and the ε_j ($j = 1\ldots.6$) represent the strain components ε_{xx}, ε_{yy}, ε_{zz}, $2\varepsilon_{xy}$, 2_{xz}, 2_{yz}. Due to the crystal symmetry for a coordinate system with its axes aligned along the crystal axes in a cubic crystal, the symmetrical stiffness matrix, C, has only the following non-zero components: $C_{11} = C_{22} = C_{33}$, $C_{12} = C_{13} = C_{23}$, $C_{44} = C_{55} = C_{66}$. Under the uniaxial tensile force (F), σ becomes

(a) along [100] crystal orientation as:

$$\sigma_{ij} = F\begin{pmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix},$$

$$\varepsilon_{zz} = FS_{11},$$
$$\varepsilon_{xx} = \varepsilon_{yy} = FS_{12},$$
$$\varepsilon_{yz} = \varepsilon_{zx} = \varepsilon_{xy} = 0,$$

and (b) along [011] crystal orientation as:

$$\sigma_{ij} = \frac{F}{2}\begin{pmatrix} 0 & 0 & 0 \\ 0 & 1 & 1 \\ 0 & 1 & 1 \end{pmatrix},$$

$$\varepsilon_{yy} = \varepsilon_{zz} = F\left(\frac{S_{11} + S_{12}}{2}\right),$$
$$\varepsilon_{xx} = FS_{12},$$
$$\varepsilon_{zx} = \varepsilon_{xy} = 0,$$
$$\varepsilon_{yz} = F\frac{S_{44}}{2},$$

where the coefficients S_{11}, S_{12} and S_{44} correspond to parallel, perpendicular and shear component, respectively. When the crystal is subjected to a uniform strain, ε, due to uniaxial and biaxial external forces, the lattice is distorted and the crystal potential V changes to V_ε. In linear approximation for small strain, ε is given by

$$V_\varepsilon = V_0 + \sum_{ij} \frac{\partial V}{\partial \varepsilon_{ij}} \varepsilon_{ij}. \tag{2}$$

The energy shifts under strain tensor ε in the crystallographic coordinate system can be computed using the standard deformation potential theory from Bir and Pikus (1974) as:

$$\Delta E_{C,i} = \Xi_d \left(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}\right) + \Xi_u \varepsilon_{ii}, \tag{3}$$

$$\Delta E_{V,(h,l)} = -a \left(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}\right) \pm \sqrt{\xi}, \tag{4}$$

where $\xi = \frac{b^2}{2}\left[\left(\varepsilon_{xx} - \varepsilon_{yy}\right)^2 + \left(\varepsilon_{yy} - \varepsilon_{zz}\right)^2 + \left(\varepsilon_{zz} - \varepsilon_{xx}\right)^2\right] + c^2\left(\varepsilon_{xy}^2 + \varepsilon_{xz}^2 + \varepsilon_{yz}^2\right)$, $\Delta E_{C,i}$ the shift in the band edge of the i ellipsoidal conduction minimum, $\Delta E_{V,h}$ and $\Delta E_{V,l}$ are the shifts in the band edges for the light and heavy maxima, respectively and the deformation potential parameters are given by Ξ_d, Ξ_u, a, b and c. From these shifts to the band extrema, effective changes to the conduction and valence band edges used in continuum device simulation can be generated. These modifications to the band structure modify the bandgap and carrier transport.

For general applied stress in the rigid-shift stress model, the electron mobility tensor is diagonal in the crystallographic coordinate system and can be written as (Egley and Chidambarrao 1993):

$$\mu_n = \mu_{n0} \begin{pmatrix} 1+\beta_1 & 0 & 0 \\ 0 & 1+\beta_1 & 0 \\ 0 & 0 & 1+\beta_1 \end{pmatrix}, \tag{5}$$

where μ_{n0} is the nominal, isotropic mobility without stress, and

$$\beta_i = \left(\frac{1 - \frac{m_L}{m_T}}{1 + \frac{2m_L}{m_T}}\right)\left\{\exp\left(\frac{\Delta E_C - \Delta E_{C,i}}{KT}\right)^{-1}\right\} \tag{6}$$

where ΔE_C is the net effective shift of the conduction band. Similarly, a mobility model for holes can also be developed based on the relative occupancy of the hole valleys (Egley and Chidambarrao 1993). As device dimensions continue to shrink, the control of local strains becomes increasingly challenging due to the complexity of stress patterns arising in a two-dimensional local geometry. The effects of stress on transistor performance are usually estimated using a piezoresistance mobility model (Smith 1954; Thompson *et al* 2004b) and the performance change can be expressed as a linear function of various local stress components.

External strain leads to a change in the effective masses and anisotropic scattering. Following the work reported by Kanda (1982), the first effect is described by an independent constant term, $\pi^{\alpha}_{ij,\text{kon}}$, but the second effect, the scattering, can be calculated at room temperature for low-doping concentrations; $\pi^{\alpha}_{ij,\text{ var}}$ and multiplied by a doping-dependent and temperature-dependent factor, $P_\alpha\,(N, T)$. Both the effects are considered in the piezoresistive coefficients by

$$\pi^{\alpha}_{ij} = \pi^{\alpha}_{ij,\text{var}} P_\alpha\,(N, T) + \pi^{\alpha}_{ij,\text{kon}}. \tag{7}$$

In the case of electrons, the scalar mobility used in the drift-diffusion and hydrodynamic equations is a mean value averaged over different conduction band minima. If the symmetry of the crystal is destroyed, for example, by external strain, the conduction band valleys shift and, therefore, yield electron transfers between the valleys. This redistribution of electrons in the conduction band leads to anisotropic scattering. In the case of holes, the mobility is an averaged quantity including heavy and light holes. External strain leads to a lift of the degeneracy at the valence band maximum. The doping and temperature dependent factor, $P_\alpha\,(N, T)$, can be expressed as (Synopsys Inc. 2008a):

$$P_\alpha\,(N, T) = \frac{300K}{T} \frac{F'_{1/2}\left(\frac{E_{F,\alpha}}{KT}\right)}{F_{1/2}\left(\frac{E_{F,\alpha}}{KT}\right)} \tag{8}$$

where $F_{1/2}\left(\frac{E_{F,\alpha}}{KT}\right)$ and $F'_{1/2}\left(\frac{E_{F,\alpha}}{KT}\right)$ are the Fermi integrals of the order 1/2 and its first derivative. The Fermi energy, $E_{F,\alpha}$, is equal to F_n–E_C for electrons and E_V–F_p for holes. They are calculated by using appropriate analytical approximations (Selberherr 1984), where the charge neutrality is assumed between carrier and doping (N), and it gives

Table 1. Longitudinal and transverse piezoresistance coefficients evaluated for standard layout and wafer orientation.

$1 \times 10\ \text{cm}^2\text{dyn}^{-1}$	⟨100⟩		⟨110⟩	
Polarity	$\pi_{\|\|}$	$\pi_\perp$	$\pi_{\|\|}$	$\pi_\perp$
n or p	$\pi_{11,\text{var}}$	$\pi_{12,\text{var}}$	$\left(\pi_{11,\text{var}} + \pi_{12,\text{var}} + \pi_{44,\text{var}}\right)/2$	$\left(\pi_{11,\text{var}} + \pi_{12,\text{var}} - \pi_{44,\text{var}}\right)/2$
n-type	−102·6	53·4	−31·4	−17·8
p-type	1·5	1·5	56·5	−53·5
n or p	$\pi_{11,\text{var}}$	$\pi_{12,\text{var}}$	$\left(\pi_{11,\text{var}} + \pi_{12,\text{var}} + \pi_{44,\text{var}}\right)/2$	$\left(\pi_{11,\text{var}} + \pi_{12,\text{var}} - \pi_{44,\text{var}}\right)/2$
n-type	0	0	0	0
p-type	5·1	−2·6	15·25	−12·75

doping dependence of the model. The numeric evaluation of $P_\alpha(N, T)$ is based on an analytical fit of the Fermi integrals (Wolfram 1991). The longitudinal and transverse piezoresistance coefficients for low-doped silicon at 300 K and the standard layouts are given in table 1.

To quantify strained-Si mobility enhancement, one uses the piezoresistance coefficients for bulk Si wafer with (001) surface and wafer notch on the [110] axis, since uniaxial process-induced strain is generally applied either parallelly (longitudinal) or perpendicularly (transverse) to the direction of MOSFET current flow, aligned to the ⟨100⟩ axes. The effect of mechanical stress on the mobility can then be expressed as follows (Thompson *et al* 2004b):

$$\frac{\Delta\mu}{\mu} \approx \left|\pi_{||}\sigma_{||} + \pi_{\perp}\sigma_{\perp}\right|, \tag{9}$$

where the subscripts || and ⊥ refer to the directions parallel and transverse to the current flow in the plane of MOSFETs, $\Delta\mu/\mu$ the fractional change in mobility, $\sigma_{||}$ and $\sigma_{\perp}$ the longitudinal and transverse stresses, $\pi_{||}$ and $\pi_{\perp}$ the piezoresistance coefficients expressed in Pa^{-1}. $\pi_{||}$ and $\pi_{\perp}$ can be expressed in terms of the three fundamental cubic piezoresistance coefficients, π_{11}, π_{12} and π_{44}.

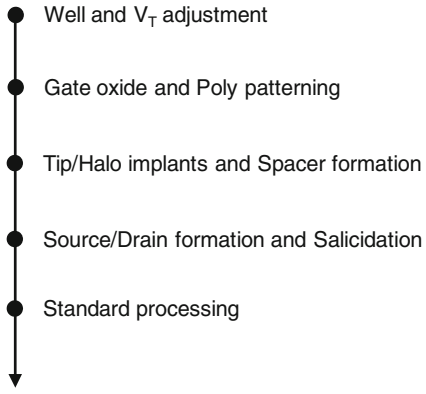

Figure 1. Typical process flow used in simulation.

3. Process/device simulation

As device dimensions continue to decrease, control of local strain becomes increasingly challenging due to the complexity of stress pattern arising in a three-dimensional local geometry. Full 2-*D*/3-*D* modeling is necessary to account for realistic transistor geometry, processing and layout and to understand their influence on the final stress distribution. Sentaurus Process and Device simulators are used to simulate and optimize CMOS process flow, including substrate surface orientation channel, halo, source/drain (*S*/*D*) profile engineering, oxidation, deposition, etching and annealing for

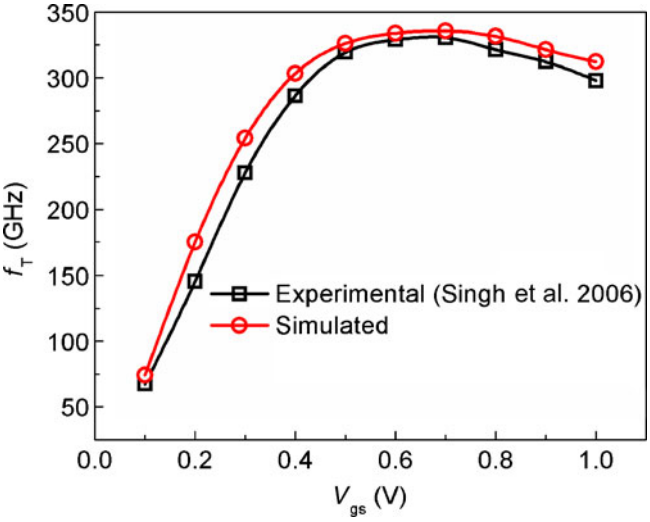

Figure 3. Comparison of gate bias dependence of f_T with experimental data of Singh *et al* (2006) and simulation for *n*-MOSFETs.

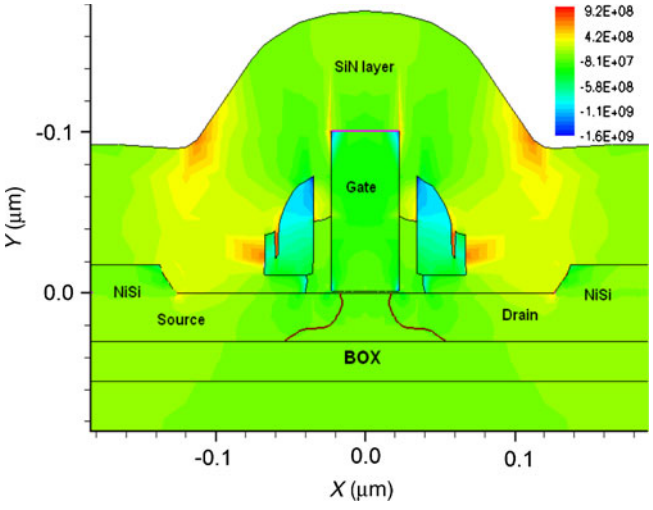

Figure 2. Stress distribution (*yy* component) of stress tensor (σ_{yy}) in device at end of process flow.

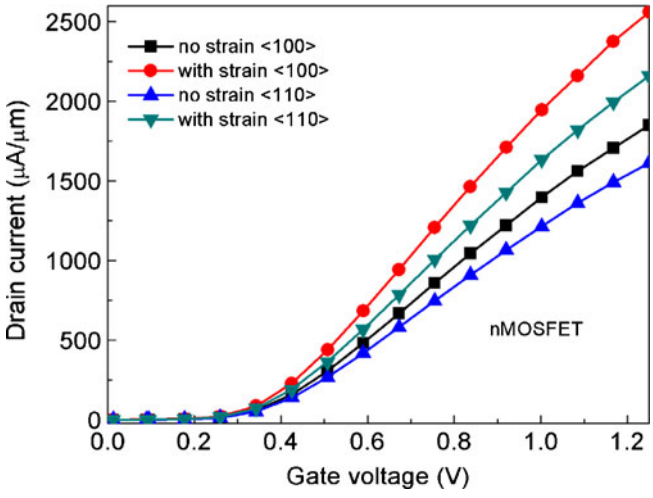

Figure 4. Comparison of $I_{DS} - V_{GS}$ characteristics for devices with a highly tensile cap layer and a relaxed cap layer.

dopant activation. The structure generated by Sentaurus Process is then characterized using device simulator Sentaurus Device. The simulation results have been bench-marked with reported experimental *n*-MOSFET results.

The hydrodynamic transport model was used in all simulations. In addition to this transport model, two strain specific models were used to capture the influence of stress on carrier transport: the Egley strained-Si mobility model and the six-band hole mobility model, which describe dependency of the bandgap on stress, as discussed in § 2. Given that the silicon–germanium (SiGe) pockets in the source and drain areas of the *p*-MOSFET lead to heterojunction, Sentaurus Device automatically accounts for the transport across this hetero-interface.

Recently, Singh *et al* (2006) fabricated strain-engineered *n*-MOSFETs on ultrathin SOI using channel stress engineering. The authors have studied the effects of (a) stressed contact liners, (b) stress memorization, and (c) a combination of both methods, on the a.c. performance of ultrathin SOI devices with a body thickness of 18 nm. It has been shown that the combination of both stress methods result in record cut-off frequencies as high as 330 GHz, highest ever reported for a Si-based MOSFETs (Singh *et al* 2006). In this work, towards calibration of simulation results, we have chosen a strain-engineered *n*-MOSFET for benchmarking. In process simulation, we adopted the process flow from Singh *et al* (2006) as shown in figure 1.

A highly tensile capping layer was deposited at the end of the process. It is known that the high tensile stress in the cap layer creates compressive stress in the source and drain regions. The stress also induces tensile stress in the channel area. The distribution of the *yy* component of the stress tensor σ_{yy} at the end of the process flow is shown in figure 2. This stress component describes the stress in the direction parallel to the channel of the device.

Figure 3 shows both simulated and reported experimental gate bias dependence of f_T for *n*-MOSFETs with stress and exhibits a f_T of 330 GHz and shows significantly higher than the measured on the "no stress" control device (Singh *et al* 2006). Since f_T depends on both C_{gs} and g_m, it is important to understand the impact of stress. To a first order, C_{gs} increases linearly with L_{poly} and is almost identical for the different stress conditions. Thus, improvement in observed devices is driven primarily by stress-induced enhancement of g_m. C_{gs} is almost identical for devices with different stress and orientation configurations, showing that the enhancement results in stress-induced enhancements g_m. An excellent match between the experimental data and simulation is observed which shows reliability of the predictive simulation using TCAD.

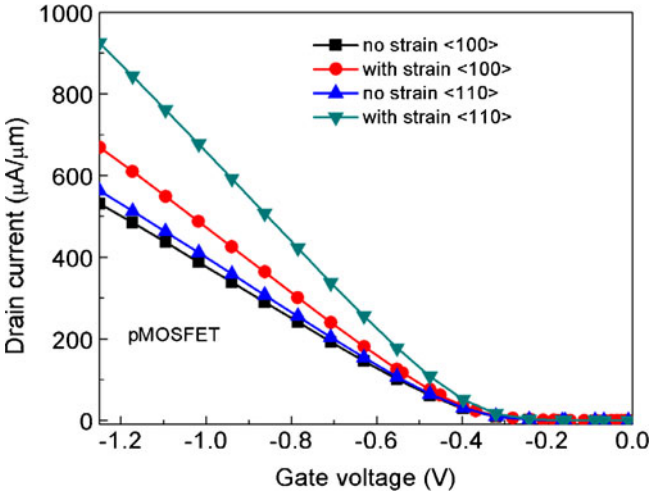

Figure 5. Drain current vs gate voltage ($I_{DS} - V_{GS}$) characteristics for *p*-MOS devices with and without compressive stress.

4. Device optimization

In this section, we present computer-aided design technology and simulation results for both the *n*- and *p*-MOSFETs on ⟨100⟩ and ⟨110⟩ hybrid orientation substrates, respectively. As described in § 3, the two-dimensional (2-*D*) process and device simulators in Sentaurus TCAD tools from Synopsys were used for simulation. The gate length (L_G) of the devices was varied between 35 and 90 nm, while the cap layer thickness was varied from 10 to 250 nm. The oxide thickness of the devices is kept constant and fixed at 1.3 nm, while the source/drain overlap is adjusted to the gate length to represent 10–15% of L_G on each side. The source and drain regions are idealized by a short box doped at 1×10^{20} cm^{-3} and present negligible series resistance. The value of the gate resistance (R_{gate}) is added via post processing to the TCAD simulations. Also, in the simulation, the drain source voltage (V_{DS}) was set to 1.2 V and the gate voltage was varied.

Table 2. Several important device parameters for 45-nm gate length MOSFETs.

	n-MOSFET				*p*-MOSFET			
	⟨100⟩		⟨110⟩		⟨100⟩		⟨110⟩	
Parameters	No stress	With stress	No stress	With stress	No stress	With stress	No stress	With stress
V_T (V)	0·195	0·178	0·196	0·186	−0·441	−0·304	−0·442	−0·286
I_{on}(A/μm)	1·69e–03	2·35e–03	1·46e–03	1·99e–03	4·89e–04	6·10e–04	5·09e–04	8·52e–04
I_{off} (A/μm)	2·27e–08	3·39e–08	2·21e–08	2.77e–08	7·66e–11	1·16e–09	7·68e–11	1·76e–09
g_m(S/μm)	2·19e–03	2·97e–03	2·14e–03	2·53e–03	8·01e–04	9·05e–04	8·15e–04	1·06e–03

For comparison, sub-45 nm node process-induced strained channel n-MOSFETs with different surface orientations were simulated. In figure 4 a comparison of the drain current against the gate voltage ($I_{DS} - V_{GS}$) characteristics for the devices with a highly tensile cap layer and a relaxed capping layer is shown.

The corresponding 2-D simulation shows a slightly higher current gain due to stress (of the order of 14–15%). It gives drive current improvement in the ⟨100⟩ direction and is of significance than in the ⟨110⟩ under the longitudinal uniaxial tensile stress.

Process-induced strained p-MOSFETs with sub 45 nm node have been simulated for different surface orientations. Figure 5 compares the drain current against the gate voltage characteristics for the devices with compressive stress. The corresponding 2-D simulation shows a slightly higher current gain due to stress. It produces a drive current improvement in the ⟨110⟩ direction and is much more than in the ⟨100⟩ direction under the longitudinal uniaxial tensile stress.

Important device parameters for both the n- and p-MOSFETs are shown in table 2 from which it is observed that most of the parameters are enhanced due to inclusion of strain in simulation showing advantage of combining both HOT technology and process-induced strain.

5. Scaling issues

In this §, we present the effects of scaling on d.c. and RF performances of process-induced strained n- and p-MOSFETs in hybrid orientation technology.

5.1 *Gate length scaling*

In simulation, we considered devices with gate length from 35–90 nm. As expected, f_T increases with the decrease of gate length. This indicates improvement in n-MOSFET mobility in the ⟨100⟩ direction over the ⟨110⟩ direction using higher tensile stress (see figure 6) due to SiN cap layer.

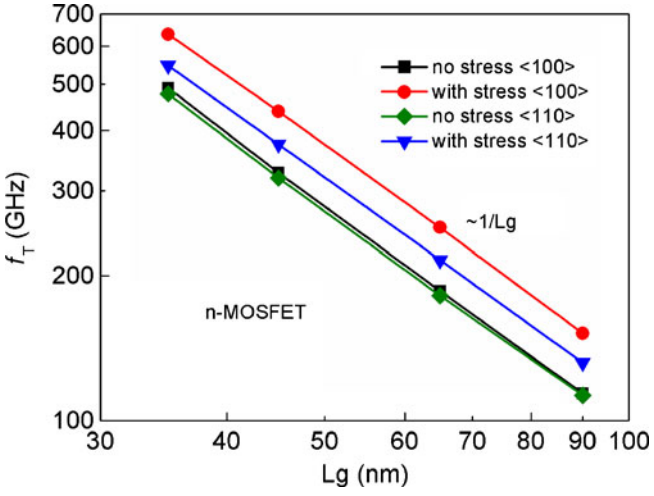

Figure 6. f_T vs gate length for different orientations for n-MOSFETs.

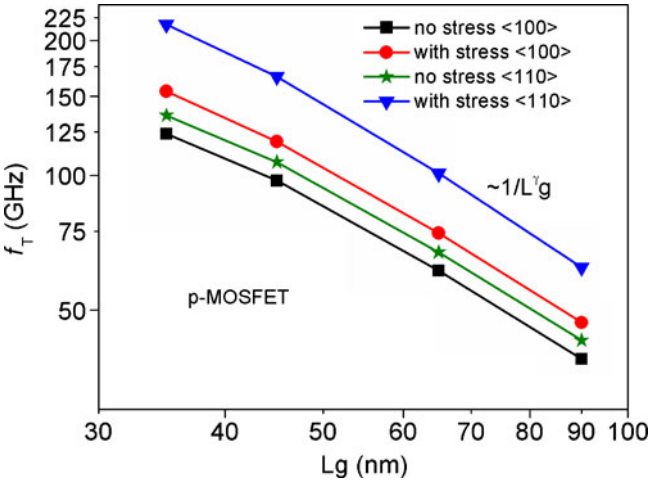

Figure 7. f_T vs gate length for different orientations for p-MOSFETs.

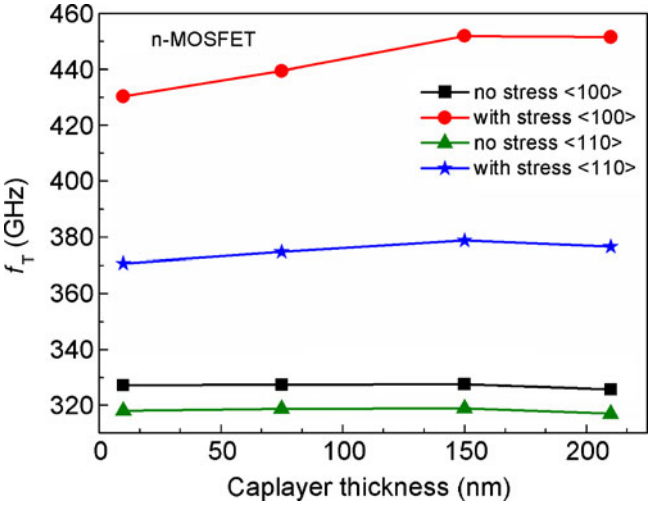

Figure 8. Effect of cap layer thickness on f_T for various channels stress condition in n-MOSFETs.

Figure 6 also illustrates the fact that the reduction of gate length affects the cut-off frequency as the mobility enhancement takes place via process-induced strain. Figure 6 shows a higher f_T in the ⟨100⟩ direction with high tensile capping layer and an f_T of above 600 GHz is predicted for 35-nm gate length. Similarly, figure 7 shows effect of gate length on ⟨100⟩ and ⟨110⟩ orientation p-MOSFETs. For instance, p-MOSFET f_T on ⟨100⟩ orientation is less sensitive than that of ⟨110⟩ orientation.

Non-quasistatic small-signal a.c. model for the short channel MOSFETs are dominated by velocity-saturation (V_s) effects. The effective saturation velocity (V_s) increases with decreasing gate length (L_g) and follows a $1/L_g^{\gamma}$ law with $1 \leq \gamma \leq 2$ in the submicron regime (Kang 1991).

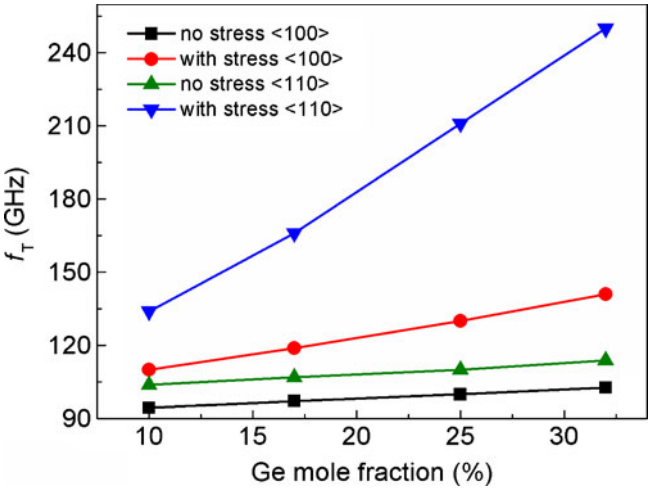

Figure 9. Variation of f_T as a function Ge mole fraction in *p*-MOSFETs.

5.2 *Cap layer thickness scaling*

n-MOSFETs use a highly tensile silicon nitride capping layer to induce tensile strain in the channel region. A significant increase of f_T on different thicknesses of capping Si_3N_4-layer with various orientations has been observed and is shown in figure 8. As expected, f_T increases with increase in cap layer thickness for process-induced strained *n*-MOSFETs. For a given cap layer thickness, f_T is larger in the ⟨100⟩ direction than the ⟨110⟩ direction under high tensile uniaxial stress. The f_T of *n*-MOSFET with Si_3N_4 250-nm shows a significant increase compared to 10-nm Si_3N_4 and higher f_T in the ⟨100⟩ direction than the ⟨110⟩ direction. Variation of f_T with cap layer thickness is negligible for bulk silicon MOSFETs for both orientations. It signifies that there are no stress effects on bulk Si MOS device performances.

5.3 *Effect of SiGe stressor*

Figure 9 shows Ge mole fraction dependence of f_T for various channel stress conditions in case of *p*-MOSFETs. The mechanical properties of binary compounds change with the ratio of substance concentration. The elastic moduli and mechanical stress change linearly with Ge mole fraction in $Si_{1-x}Ge_x$. As expected, f_T increases linearly with increase of Ge content as the stress is increased.

6. Conclusions

RF performance of process-induced strained-Si *n*- and *p*-MOSFETs in hybrid orientation technology has been studied via simulation using CAD tools technology which properly account for the physical mechanisms, such as orientation-dependent and process-induced strain-dependent mobility models. We have studied the effects of mobility enhancement, induced by surface orientation change and also process-induced strain, simultaneously, on the RF performance of CMOS devices. Our predictive simulation results have shown superiority of hybrid orientation technology.

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