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DLTS study of annihilation of oxidation induced deep-level defects in Ni/SiO_2/*n*-Si MOS structures

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Abstract. **This paper describes the fabrication of MOS capacitor and DLTS study of annihilation of deep-level defects upon thermal annealing. Ni/SiO_2/*n*-Si MOS structures fabricated on *n*-type Si wafers were investigated for process-induced deep-level defects. The deep-level traps in Si substrates induced during the processing of Ni/SiO_2/*n*-Si have been investigated using deep-level transient spectroscopy (DLTS). A characteristic deep-level defect at E_C = 0·49 eV which was introduced during high-temperature thermal oxidation process was detected. The trap position was found to shift to different energy levels (E_C = 0·43, 0·46 and 0·34 eV) during thermal annealing process. The deep-level trap completely anneals at 350°C. Significant reduction in trap density with an increase in recombination life time and substrate doping concentration as a function of isochronal annealing were observed.**

Keywords. **MOS capacitor; DLTS; deep-level defect; thermal annealing.**

1. Introduction

The behaviour of defects in semiconductor structures induced during fabrication process is a major concern for microelectronics device technologies. As technology is moving towards very large-scale integration, millions of components are to be fabricated on a single chip. To ensure proper functioning of the chip, the fraction of the defective components must be smaller than 10^{-6} components per chip (Umeda *et al* 2004). This implies that even a small number of defects may potentially cause a serious threat to the functionality and reliability of semiconductor devices. Semiconductor device processing includes a number of steps, viz. oxidation, diffusion, ion implantation, metallization, etc which may lead to the introduction of defects in the substrate. Some of the high-temperature processing like thermal oxidation is found to generate dislocations in the silicon bulk (Sze 1988; Murarka and Peckerar 1989). The lattice defects are usually characterized by highly localized states situated deep in the band gap as well as even close to the valence or conduction band edges which are commonly called deep-level defects. Impurities, vacancies, interstitials or their clusters are some of the examples of such deep-level defects. Deep-level defects have larger capture cross sections than hydrogenic shallow defects and, in most cases, determine the minority carrier lifetime. Therefore, these defects play an important role in manufacturing high-speed electronic and optoelectronic devices. With technological scaling of semiconductor devices, the processing steps tend to become more complicated and are likely to result in more process-induced defects. Hence, defect investigation and characterization are interesting from the cognitive and practical point of view, as they govern the effective production of perfect semiconductor devices (Gelczuk *et al* 2005).

Several techniques like electrically detected magnetic resonance (EDMR), electron paramagnetic resonance (EPR), thermally stimulated current (TSC) and thermally stimulated capacitance (TSCAP) are in practice for the characterization of defects in Si devices. In our present study, a more recent and widely used technique, namely, deep-level transient spectroscopy (DLTS), is employed for characterization of deep levels in the silicon band gap. DLTS is a capacitance transient thermal scanning technique and it overcomes the drawbacks of other conventional techniques like TSC and TSCAP in view of its better immunity to noise and surface channel leakage current. It is sensitive (detects trap concentrations as low as 10^{-4} in order), spectroscopic (exhibits a peak for each trap detected) and allows to obtain parameters from either minority (positive peak in the spectrum) or majority (negative peak) carrier traps. Easy and direct interpretation of experimental results obtained from DLTS study makes it a valuable tool for defect analysis (Lang 1974; Sumathi *et al* 1999; Garcia and Reyes Barranca 2002).

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2. Materials and methods

2.1 *Fabrication of MOS structure*

The MOS capacitor structures were prepared in the clean room facilities at Central Electronics Engineering Research Institute (CEERI), Pilani. Structures were fabricated on silicon wafer ⟨100⟩ oriented, 0·08–0·2 Ω-cm resistivity, *n*-type phosphorous doped, 1·5 in diameter and 220 μm thick. The Si wafer was degreased for 5 min in boiling tri-chloro ethylene, acetone and methanol consecutively. Standard cleaning procedures like RCA-I, RCA-II and Piranha were followed to remove organic residues and metal ions from Si wafer. In case of RCA-I, the wafer was dipped in a solution of $H_2O : H_2O_2 : NH_4OH$ (5 : 1 : 1). In the case of RCA-II, the wafer was dipped in a solution of $H_2O : HCl : H_2O_2$ (6 : 1 : 1) and in the case of Piranha, the wafer was dipped in $H_2SO_4 : H_2O_2$ (7 : 1) solution. After each cleaning procedure, the wafer was thoroughly cleaned with de-ionized water and dipped in HF for few seconds to remove native oxides. Finally, the wafer was again dipped in methanol and dried using nitrogen gun. A sacrificial cleaning oxide was grown for 20 min (keeping other process parameters same as during gate oxidation) which was completely etched off before gate oxidation. For gate oxidation, the wafer was loaded into the oxidation furnace at 800°C in N_2 ambient. The thermal oxide growth was done at 1050°C in dry oxygen atmosphere for 40 min. The wafer was cooled at a rate of ~ 1°C/s in N_2 ambient and unloaded from the furnace at 800°C. The oxide thickness was measured to be 82 nm on Ellipsometer. Ni was selected for the gate contact. Metallization for the gate was done under vacuum of 10^{-7} torr using Varian's e-beam metallization unit. Circular Ni dots with 2 mm diameter were formed uniformly all over the wafer, which was defined using metal mask. Silver was used to provide ohmic contact on the back of the wafer.

2.2 *DLTS measurements*

Since its introduction by Lang in 1974, DLTS has become a widely used method to investigate deep traps in semiconductors (Langfeld 1987). The DLTS system (IMS-2000) employed for the present study consists of a boxcar averager, a pulse generator, a thousand point digitizer, a voltage generator and a high-speed capacitance meter. The pulse generator is capable of generating pulses with widths ranging from 100 ns to 10 s. The pulse height could be programmed from –12 to +12 V. The boxcar averager is capable of generating seven rate windows. The time constants can be varied from 1 ms to 2 s. In the present study, DLTS spectra are recorded with a reverse bias of 5 V and pulse width of 20 ms applied between the gate and the substrate. DLTS spectra were recorded for 'as processed' MOS capacitor. The device was subjected to isochronal annealing for 30 min at various temperatures (200, 250, 300 and 350°C) and the DLTS spectra were recorded after annealing at each temperature. The trap concentration, activation energy and capture cross section of different deep-levels were determined by DLTS data.

3. Results and discussion

Figure 1 exhibits the DLTS spectra of MOS capacitor before and after annealing at four different annealing

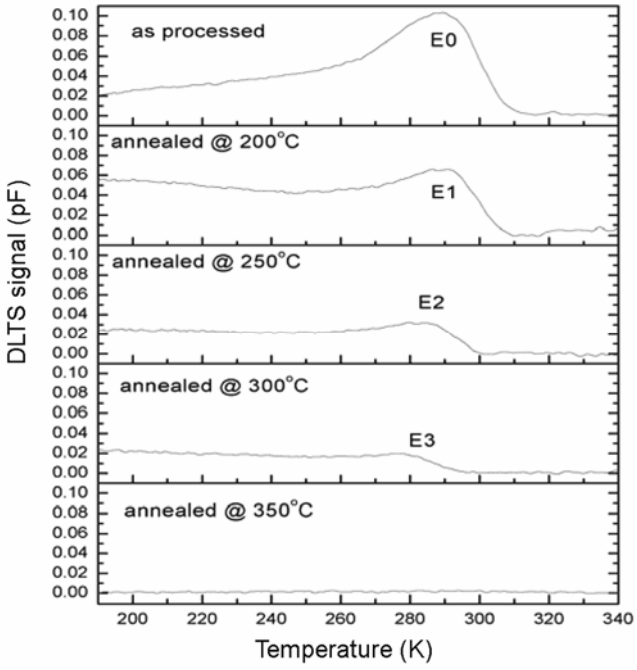

Figure 1. DLTS spectra of *n*-type Si–SiO_2 structure before and after annealing.

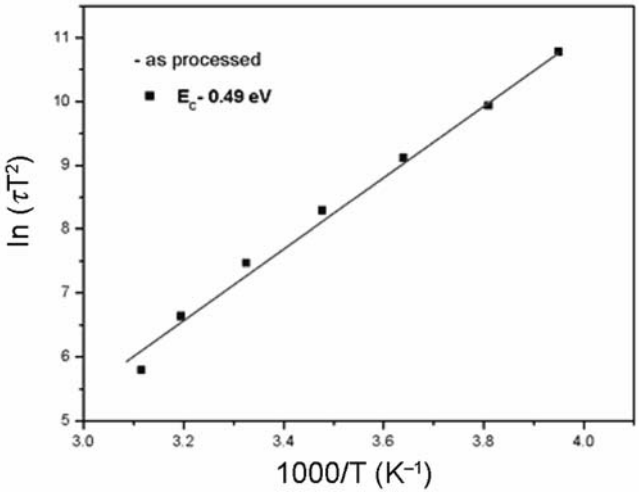

Figure 2. Arrhenius plot for 'as processed' device.

temperatures. The DLTS spectrum is a plot of difference in capacitance (δC) versus temperature. The trap concentration (N_T) can be determined by knowing the peak height (δC_{max}) in the DLTS spectrum. Activation energy (ΔE) and capture cross section (σ) of the deep levels are calculated by using the following equation

$$\tau T^2 = \frac{\exp[(\Delta E)/kT]}{\gamma\sigma}. \quad (1)$$

In the above equation, γ is the material coefficient, T the temperature and τ the time constant. A plot of $\ln(\tau T^2)$ versus $1/T$ is known as the Arrhenius plot; the activation energy ΔE is obtained from the slope of the plot and the capture cross section is obtained by extrapolating the plot on the Y-axis. Figures 2–5 exhibit the Arrhenius plots of deep-level defects for 'as processed' and annealed MOS samples.

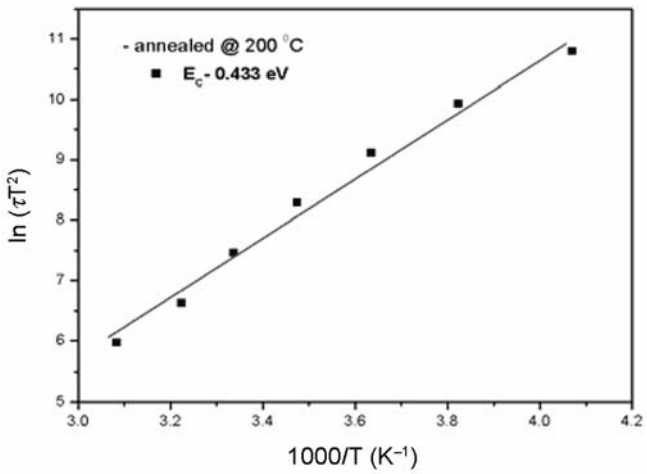

Figure 3. Arrhenius plot for device annealed at 200°C.

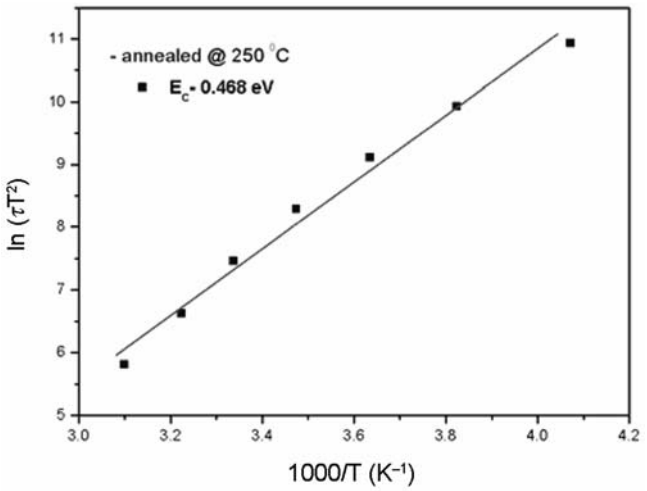

Figure 4. Arrhenius plot for device annealed at 250°C.

The trap concentration and capture cross section of all the deep-level defects are calculated from the DLTS spectra. The activation energy of all the defects has been measured to an accuracy of 0·001 eV. The recombination of electron–hole pairs at the defect levels is dependent on trap concentration. The recombination lifetime is calculated using the following equation

$$\tau = \frac{1}{\sigma_n v_{th} N_T}. \quad (2)$$

In (2), σ_n is the minority carrier capture cross section, v_{th} the thermal velocity of the carriers and N_T the total trap concentration. The deep level defects in silicon devices have been studied by many research groups (Lafevre 1980, 1982; Shinoda and Ohta 1992; Vujicic *et al* 2000; Kaschieva *et al* 2009) and the identification of

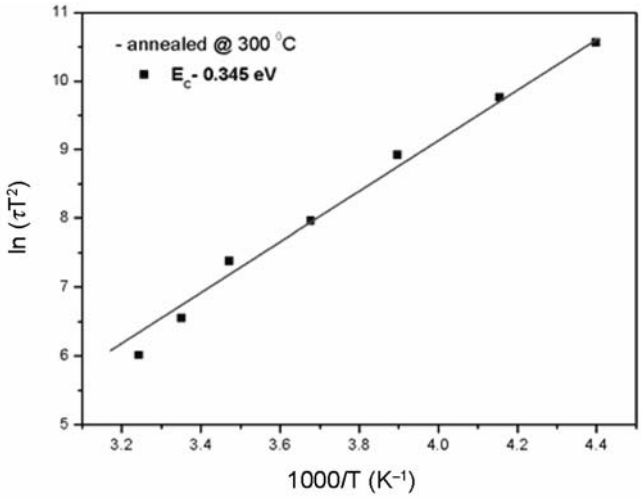

Figure 5. Arrhenius plot for device annealed at 300°C.

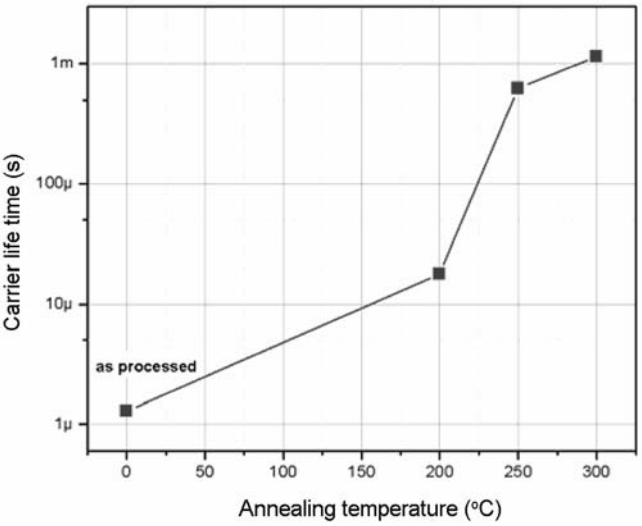

Figure 6. Carrier lifetimes as a function of annealing temperature.

Table 1. Characteristics of the deep-level defects after thermal annealing at different temperatures in MOS capacitor.

Annealing temperature (°C)	Defect type	Activation energy E_C (eV)	Trap concentration (cm^{-3})	Capture cross- section (cm^{-2})	References
As processed (before annealing)	Si(i)	0·49	$1{\cdot}10 \times 10^{15}$	$6{\cdot}2 \times 10^{-17}$	Lafevre 1980, 1982
200	Phosphorous vacancy pair (*V–P*)	0·43	$7{\cdot}15 \times 10^{14}$	$6{\cdot}96 \times 10^{-18}$	Vujicic *et al* 2000
250	Vacancy related complex	0·46	$3{\cdot}65 \times 10^{14}$	$4{\cdot}49 \times 10^{-17}$	Shinoda and Ohta 1992; Kaschieva *et al* 2009
300	Multi-vacancy-oxygen (V_2O_2 or V_3O)	0·34	$1{\cdot}62 \times 10^{14}$	$4{\cdot}87 \times 10^{-19}$	Kuchinskii *et al* 1987; Vujicic *et al* 2000

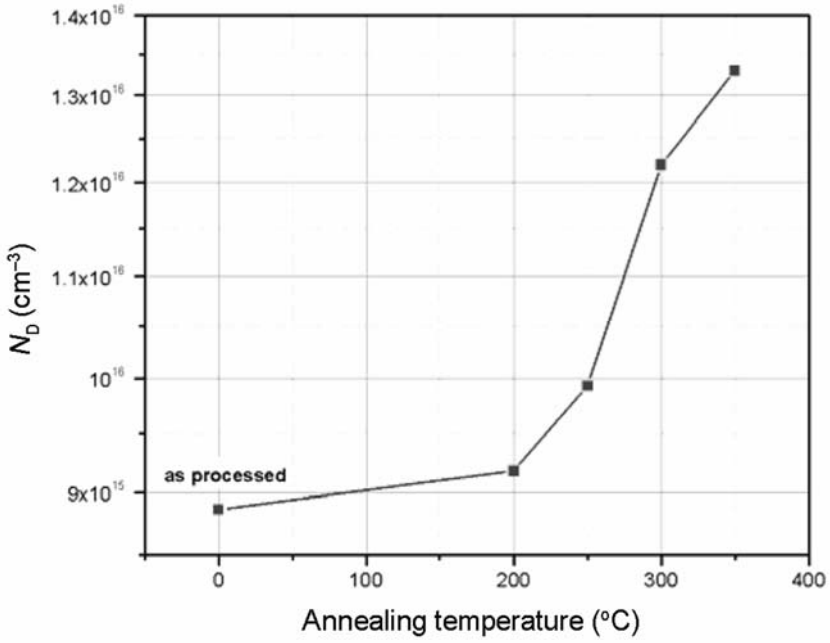

Figure 7. Substrate doping measured after each annealing temperature.

defect type is made on the basis of their finger prints such as activation energy and capture cross section by comparing with those reported in the literature.

As one can see from the figure 1, the DLTS spectrum of the 'as processed' sample exhibits one peak at a temperature of 302 K which corresponds to a deep-level (labeled E0) with activation energy of $E_C = 0{\cdot}49$ eV in the forbidden gap of silicon. This defect can be attributed to interstitial silicon or the self interstitial Si(i). This defect is most likely generated due to oxidation of silicon samples (Lafevre 1980, 1982). Thermal annealing of the device at various temperatures results in a shift in the temperature as well as peak height. The defect acquires a different energy level with reduction in the peak height as the annealing temperature is increased. The reduction in the peak height is an indication of the decrease in trap density. Table 1 exhibits the assignment of defect and its characteristics at different annealing temperatures. Carrier lifetime has been calculated from the DLTS data. Figure 6 shows that the carrier lifetime increases with annealing temperature. This is in conformity with the decrease in trap density with increase in annealing temperature as shown in table 1. Figure 7 shows the variation in substrate doping concentration with annealing temperature obtained from DLTS.

4. Conclusions

Deep-level defect induced during the fabrication of $Ni/SiO_2/n$-Si MOS structures can be attributed to interstitial silicon or the self interstitial Si(i). This defect is likely to be induced during a high-temperature thermal oxidation process. The characteristics of this defect

change with thermal annealing at different temperatures as the defect occupies new energy levels. The trap density is found to decrease with increase in annealing temperature. The recombination lifetime and substrate doping were found to increase as annealing temperature increases. The interstitial silicon defect completely anneals at 350°C. The present study thus brings about the importance of thermal annealing of devices to remove process induced defects in semiconductor fabrication.

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