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High-energy heavy ion testing of VLSI devices for single event upsets and latch up

S B UMESH, S R KULKARNI†, R SANDHYA, G R JOSHI*, R DAMLE† and M RAVINDRA

Components Division, ICG, ISRO Satellite Centre, Airport Road, Bangalore 560 017, India

†Department of Physics, Bangalore University, Bangalore 560 056, India

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Abstract. Several very large scale integrated (VLSI) devices which are not available in radiation hardened version are still required to be used in spacecraft systems. Thus these components need to be tested for high-energy heavy ion irradiation to find out their tolerance and suitability in specific space applications. This paper describes the high-energy heavy ion radiation testing of VLSI devices for single event upset (SEU) and single event latch up (SEL). The experimental set up employed to produce low flux of heavy ions viz. silicon (Si), and silver (Ag), for studying single event effects (SEE) is briefly described. The heavy ion testing of a few VLSI devices is performed in the general purpose scattering chamber of the Pelletron facility, available at Nuclear Science Centre, New Delhi. The test results with respect to SEU and SEL are discussed.

Keywords. High-energy heavy ions; single event effect; linear energy threshold; radiation hardened; upset and latch up.

1. Background

Radiation in space environment causes performance degradation, logic upsets and latch-up failures in integrated circuits. Spacecraft systems use radiation hardened hi-rel integrated circuits to protect against total ionization dose (TID) effects and single event effects (SEE) such as single event upset (SEU) and single event latch up (SEL). Radhard ICs have protection against both TID and SEE effects. In case of non-availability of radhard ICs, rad tolerant devices are chosen after examining the criticality of the device for specific application (Umesh *et al* 2004). Single event upset is defined by NASA as 'radiation-induced errors in microelectronic circuits caused when charged particles (usually from the radiation belts or from cosmic rays) lose energy by ionizing the medium through which they pass, leaving behind a wake of electron-hole pairs'. SEU are transient soft errors and are non-destructive. A reset or rewriting of the device results in normal device behaviour thereafter. An SEU may occur in analog, digital, or optical components, or may have effects in surrounding interface circuitry. SEUs typically appear as transient pluses in logic or support circuitry, or as bit flips in memory cells or registers. Also possible is a multiple-bit SEU in which a single ion hits two or more bits causing simultaneous errors. Multiple-bit SEU is a problem for single-bit error detection and correction (EDAC) where it is impossible to assign bits within a word to different chips (example, a problem for DRAM and certain SRAMs). A severe SEU is the single-event functional interrupt (SEFI) in which an SEU in the device's control circuitry places the device into a test mode, halt, or undefined state. The SEFI halts normal operations and requires reset to recover. SEL is a condition that causes loss of device functionality due to a single event induced current state. Kolasinski *et al* (1979) first observed SEL during ground testing. SELs are hard errors and are potentially destructive (i.e. may cause permanent damage). The SEL results in high operating current, above device specifications. The latched condition can destroy the device, drag down the bus voltage, or damage the power supply. Originally, the concern was latch up caused by heavy ions, however, latch up can be caused by proton in very sensitive devices (Adams *et al* 1992; Nichols *et al* 1992). An SEL is removed by a power off-on reset or power strobing of the device. If power is not removed quickly, catastrophic failure may occur due to excessive heating, or metallization or bond wire failure. SEL is strongly temperature dependent: the threshold for latch up decreases at high temperature and the cross-section increases as well (Mouret *et al* 1994, 1995).

Rad tolerant memory devices from M/s Atmel such as 1MB SRAM and 4K × 9 FIFO are being proposed for one such application in low earth orbit (LEO) missions. To assess the tolerance of these devices for SEU and SEL, heavy ion radiation testing was conducted at the Nuclear Science Centre, New Delhi.

In addition to these devices, a MIL-STD-883 class 'B' level 1MB EEPROM from M/s Atmel used in launch

*Author for correspondence (grjoshi@isac.ernet.in)

vehicle programme, a radhard MIL–STD–1553B Bus controller IC from M/s DDC-ILC, USA being proposed for use in Bus Management Unit (BMU) and bulk CMOS shift register IC from M/s Intersil and M/s STM were also tested for SEE.

The devices were exposed to low flux of heavy ions of silicon (Si^{8+}) and silver (Ag^{8+}). The test results with respect to SEE are discussed.

2. Introduction

The space environment of LEO and geo stationary orbit (GEO) contains high energy particulate radiation in the energy levels of a few MeVs to hundreds of MeVs. The sub micron CMOS VLSI devices in particular, are very sensitive to particulate radiation as compared to other technology devices. Different VLSI devices have similar packaging constituents. The packages are normally made out of ceramic substrate with kovar pins and top lid. Top lid will be removed and active devices are made using silicon as base material with diffusion of *p*- and *n*-types (V or III group elements like phosphor, antimony on boron, aluminium) and aluminium metallization. The packaging constituents will not vary from batch to batch. The products used for testing are qualified under space flow/ high reliability line which is the highest reliability product available. The high-energy particles impinging on these devices can cause SEU and SEL, resulting in device degradation or total failure.

The ASTM standard F1192M95 specifies the testing of the low feature dimensions less than 5 μm to heavy ions with linear energy transfer (LET) values in the range of 1–100 MeV-cm^2/mg (ASTM 95). The present experimental set up at NSC, New Delhi, provides low flux heavy ion irradiation with LET in the range of 1–70 MeV-cm^2/mg. As these particles cannot penetrate through the device package, the devices are tested with their top lid removed.

The gold (Au^+) ion beam, which can impart energies with LETs up to 70 MeV-cm^2/mg, was not available due to some technical constraints in the Pelletron facility like not able to deflect the heavy gold ions into general purpose scattering chamber (GPSC) where the experiment was scheduled. The experiments were conducted only up to 42 MeV-cm^2/mg using Ag^{8+} ion.

3. Experimental

Low flux region of GPSC of the Pelletron facility at NSC, New Delhi, was used for this purpose. A direct heavy ion beam produces very high flux in the range of 10^8–10^9 ions/cm^2/s whereas for SEE testing and monitoring of the device, the flux required is in the range of 300–500 ions/cm^2/s to the total fluence of 10^6–10^7 ions/cm^2. As the beam current in the Pelletron facility cannot be controlled to obtain a very low level of flux, a gold foil of thickness, 330 nm, is placed on the beam path to scatter the direct beam. A low flux chamber is connected to 20° port of the main GPSC chamber. The device under test (DUTs) is placed in the low flux chamber. Before irradiating, the heavy ion flux is measured using the surface barrier detector (SBD) and beam current is adjusted to ensure the flux is in the required range of 300–500 ions/cm^2/s. Subsequently the DUT card is placed in low flux chamber for irradiation. The signals from the DUT card are terminated to the 50 pins feed through connector. The test and measurement equipments are kept near the low flux chamber (Umesh *et al* 2004).

The devices are made to work functionally during the irradiation testing with certain test patterns that are sensitive to radiation and the device functionality and supply current are continuously monitored.

4. Device under test details

Table 1 describes the details of the devices tested for heavy ions.

5. Test system

The test block comprises of micro controller rabbit 3200 based system. The rabbit micro controller module has

Table 1. DUT details.

Device type	Manufacturer	Function	Process	Quality level	Total ionizing dose (TID) (krad (Si))	Manufacturer specified	
						SEU LET_{th} (MeV-cm^2/mg)	SEL LET_{th} (MeV-cm^2/mg)
65608E	Atmel	128 k × 8 SRAM	0·6 μ CMOS	ESA/SCC	30	2	100
67204F	Atmel	4 k × 9 FIFO	0·6 μ CMOS	ESA/SCC	30	7	100
AT28C010	Atmel	128 k × 8 EEPROM	0·8 μ CMOS	MIL	7 tested at ISAC	Not specified	Not specified
BU61582	DDC	1553 B Bus controller	Hybrid	MIL-PRF-38534 H^+	175	100	Immune
4094B	Intersil	8 Bit shift register	7 μ CMOS	QML V	100	75	75
4094B	SGS	8 Bit shift register	7 μ CMOS	ESA/SCC	100	36	72

512k × 8 Flash ROM, 512k × 8 Flash RAM and 56 bi-directional I/O ports. It has both serial and ethernet interfaces for loading, debugging and execution of programs. The ethernet interface helps in programming and execution of the test programs from a network.

The DUT I/O pins are connected to the bi-directional I/O ports of the rabbit system and the test signals to the DUT are generated through the I/O ports. The DUT functional test programs are developed in rabbit's Dynamic C environment in personal computer (PC). After the compilation, test programs are loaded into the rabbit system via serial or ethernet interface and executed.

The test results were stored on hard disk as files and also were displayed on the PC monitor.

6. Device testing methodologies

6.1 *SRAM 65608E*

All locations in 128k × 8 SRAM are filled with checkerboard pattern of 55_h (01010101) and AA_h (10101010) in alternate locations during irradiation. Data stored in the memory is continuously read and verified with the reference data pattern. In the event of any upset, the failure is recorded and the data is re-written again. This reading and writing process continues during the whole of exposure duration.

6.2 *FIFO 67204F*

Similar to SRAM all the data locations in the FIFO are filled with checkerboard pattern of 55_h and AA_h in alternate locations and the data is continuously verified with the reference data pattern. The upsets during whole of irradiation are recorded and monitored.

6.3 *EEPROM AT28C010*

EEPROM is programmed with checkerboard pattern of 55_h and AA_h in alternate locations. During irradiation, data is continuously read and verified with the initially programmed reference pattern. The upsets during irradiation are recorded and monitored.

6.4 *Shift register 4094B*

The 8-bit store and shift register is stored with a data pattern of alternate 1's & 0's and the data stored in the shift register continuously verified with the initially stored pattern and any data upset is recorded and monitored.

6.5 *MIL–STD–1553 BC/RT 61582*

The device 61582 operates in either bus controller (BC) or remote terminal (RT) mode of operation and has two bi-directional serial interface buses A and B for transmission and reception of data in the Manchester coded data format.

The test system checks the DUT in the BC/RT mode of operation for transmission and reception of data with another device acting as RT/BC for both bus A and B. The system also checks the device's internal 16k × 16 SRAM for the checkerboard pattern of 5555_h (0101010101010101) and $AAAA_h$ (1010101010101010). Any upsets in the internal RAM or in the transmission/reception control word/data are recorded and monitored during irradiation.

7. Test results and analysis

Table 2 shows the test results of SEU and SEL of all the devices exposed to heavy ion irradiation. During irradiation, the flux of the ions was 300 ions/cm^2/s.

Table 2. Test results.

Device type	Ion	Energy (MeV)	LET (MeV-cm^2/mg)	Fluence (ions/cm^2)	SEU	SEL
65608E	$^{28}Si^{8+}$	100	11	2·7 E10	Upsets overflow	No latch up
	$^{107}Ag^{8+}$	70	42	2·7 E5	Upsets overflow	No latch up
67204F	$^{28}Si^{8+}$	100	11	2·7 E5	~ 9000 upsets/h	No latch up
AT28C010	$^{28}Si^{8+}$	100	11	5·4 E5	No upsets	No latch up
	$^{107}Ag^{8+}$	70	42	5·4 E5	No upsets	No latch up
BU61582	$^{28}Si^{8+}$	100	11	5·4 E5	No upsets	No latch up
	$^{107}Ag^{8+}$	70	42	1 E6	No upsets	No latch up
4094B	$^{107}Ag^{8+}$	70	42	5·4 E5	No upsets	No latch up
4094B	$^{107}Ag^{8+}$	70	42	5·4 E5	No upsets	No latch up

The Atmel rad tolerant devices 128k × 8 SRAM 65608E and 4k × 9 FIFO 67204F as expected are found to be very sensitive to particulate radiation. The manufacturer's LET_{th} test data for the SRAM 65608E is 2 MeV-cm^2/mg and the exposure to $^{28}Si^{8+}$ produced large number of upsets and no SEL observed. The on-orbit integral flux per day of the particles in the LET range of 2 MeV-cm^2/mg is 50 in normal period and 10^6 during solar flares. The upset probability of this device is very high and should not be used in mission critical applications. Even in non critical applications the SEU test data must be considered and appropriate mitigation techniques such as triple modular redundancy (TMR), error detection and correction logic (EDAC), etc should be incorporated.

In case of FIFO 67204F, the manufacturer's LET_{th} test data is 7 MeV-cm^2/mg and exposure to $^{28}Si^{8+}$ produced upsets at the rate of 9000/h and no SEL observed. The on-orbit integral flux per day of the particles in the LET range of 7 MeV-cm^2/mg is 5 in normal period and 5×10^5 during solar flares. This device is also not suitable for mission critical applications and mitigation techniques such as TMR, EDAC, etc shall be incorporated in its usage in non-critical applications.

The 128K × 8 EEPROM AT28C010 is a MIL–STD–883 level device and non radiation hardened device. Exposure to $^{28}Si^{8+}$ with LET_{th} of 11 MeV-cm^2/mg and $^{107}Ag^{8+}$ with LET_{th} of 42 MeV-cm^2/mg did not cause any SEU or SEL. As the device basically is not a radiation hardened one and no manufacturer's or third party's data is available, further tests are required to be conducted with more samples to confirm the test results. A total ionizing dose test is also required in addition to SEU and SEL tests.

The shift register IC4094B made by M/s Intersil and M/s SGS-Thomson Microelectronics were exposed to both $^{28}Si^{8+}$ and $^{107}Ag^{8+}$ and passed. This shows that the device LET_{th} for SEU and SEL is beyond 42 MeV-cm^2/mg for both the devices.

The DDC make radiation hardened MIL–STD–1553B BC/RT 61582 was tested to heavy ion irradiation as a part of verification of the manufacturers test data. No SEU or SEL was observed and the device functioned normally.

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