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# Electrical characterization of low temperature deposited oxide films on ZnO/*n*-Si substrate

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**Abstract. Thin films of silicon dioxide are deposited on ZnO/*n*-Si substrate at a low temperature using tetraethylorthosilicate (TEOS). The ZnO/*n*-Si films have been characterized by atomic force microscopy (AFM) and scanning electron microscopy (SEM). The border trap density ($Q_{bt}$) and fixed oxide charge density ($Q_f/q$) of the $SiO_2$/ZnO/*n*-Si films are found to be $3{\cdot}9 \times 10^{10}$ cm$^{-2}$ and $1{\cdot}048 \times 10^{11}$ cm$^{-2}$, respectively. The trapping characteristics and stress induced leakage current (SILC) have also been studied under Fowler–Nordheim (F–N) constant current stressing.**

**Keywords. ZnO; TEOS; border trap density; AFM; hysteresis.**

## 1. Introduction

Zinc oxide (ZnO) is a versatile material with a wide band gap of 3·37 eV at room temperature and has been extensively studied for various applications such as varistors, transducers, transparent conducting electrodes, sensors and catalysts. While polycrystalline ZnO is commonly used in these conventional applications, there has been a growing interest in obtaining single crystal ZnO films on various substrates (Zu *et al* 1997; Chen *et al* 1998; Narayan *et al* 1998; Fons *et al* 1999; Liu *et al* 2000). ZnO on Si offers an interesting opportunity for various functional properties of ZnO which can be combined with the advanced Si electronics on the same substrate (Water and Chu 2002).

Plasma enhanced chemical vapour deposition (PECVD) of silicon dioxide from tetraethylorthosilicate (TEOS) and oxygen plasma has been extensively investigated because of its wide ranging applications in integrated circuit manufacturing and microelectronics technology as an insulator. The advantages of PECVD films using TEOS precursor over traditional silane-based films have led to the initial incorporation of the TEOS oxides as an intermetal dielectric with the effect of producing better yields and comparable dielectric isolation (Samanta *et al* 2001). TEOS has the following advantages: low temperature processing, void-free filling for good aspect ratio (up to ~ 0·8) features, uniform deposition, easy control, good reproducibility and low cost.

In this paper, the structure of rf sputtered ZnO films on *n*-Si substrate has been investigated by X-ray diffraction (XRD), SEM and AFM. We have studied the electrical and interfacial properties of MIS structure fabricated by deposited $SiO_2$ films on ZnO/*n*-Si substrate using microwave plasma deposition system.

## 2. Experimental

The undoped polycrystalline ZnO (100 nm) thin films were deposited by rf magnetron sputtering system using a ZnO target (purity > 99·99%) with a diameter of 0·0508 m at 450°C. Substrate was *n*-type silicon with (100) orientation. Only argon gas was introduced as a plasma gas up to 10 mTorr. After standard cleaning, dielectric films were deposited on the ZnO/*n*-Si substrate using a microwave (1400 W, 2·45 GHz) plasma cavity discharge system. The base pressure of the process chamber was 1 mTorr. TEOS was kept in a bubbler whose temperature was set at 70°C and the vapour was injected into the process chamber. Typically, a pressure of 1 Torr and a deposition time of 1 min were employed for film deposition. No external heating of the substrate was made. The thickness of $SiO_2$ film (~ 120 Å) was determined using a single wavelength (6328 Å) ellipsometer (Model Gaertner L-117). The electrical properties of the deposited films were studied using MIS capacitors with an Al gate area: $1{\cdot}96 \times 10^{-3}$ cm$^2$. The high-frequency (1 MHz) capacitance–voltage (*C*–*V*), conductance–voltage (*G*–*V*), current–voltage (*I*–*V*) and constant current stressing characteristics were studied using HP-4061A semiconductor test system and HP-4145B parameter analyser, respectively.

## 3. Results and discussion

An atomic force micrograph of ZnO film is shown in figure 1. The scan was taken on an area of 400 μm$^2$. The statistical information of the topography of the ZnO films

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as observed from the height histogram of the AFM image are: rms surface roughness ($Z_{rms}$) and average roughness ($Z_{av}$) to be 50·9 Å and 30·4 Å, respectively. XRD pattern (not shown) for the undoped ZnO film shows a major peak of preferential orientation along the (103) and a minor one related to (002) which is believed to be due to a polycrystalline structure. Figure 2 shows the SEM image of the cross-sectional view of ZnO/*n*-Si films showing a columnar structure which indicates an orientation parallel c-axis (002) (Water and Chu 2002).

To improve the reliability of oxides, it is crucial to understand the nature of defects at and near the $SiO_2$/ZnO interface. According to the Deal committee's classification (Deal 1980) of oxide charges the interface trapped charge ($Q_{it}$) which resides at the $SiO_2$/ZnO interface is in rapid electrical communication with the ZnO/*n*-Si substrate, whereas the oxide trapped charge ($Q_{ot}$) resides in traps in the oxide and does not communicate with the ZnO/*n*-Si substrate. However, the fact that the oxide traps close to the interface can communicate with the *n*-Si/ZnO substrate calls for the introduction of border traps ($Q_{bt}$) (Fleetwood *et al* 1993). The border traps are charged and discharged through electron tunneling from and to the substrate. The hysteresis in the high frequency capaci-

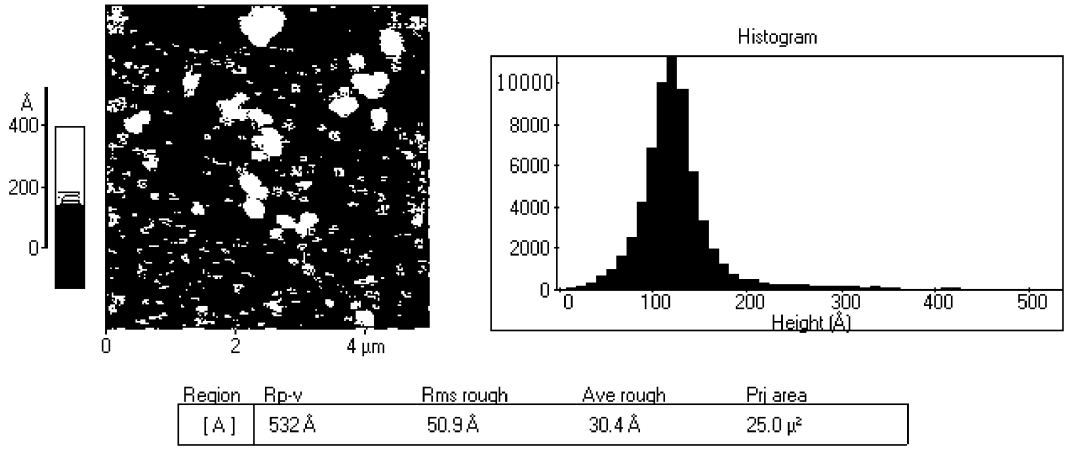


**Figure 1.** Atomic force microscope image of rf sputtered ZnO films deposited at 450°C.

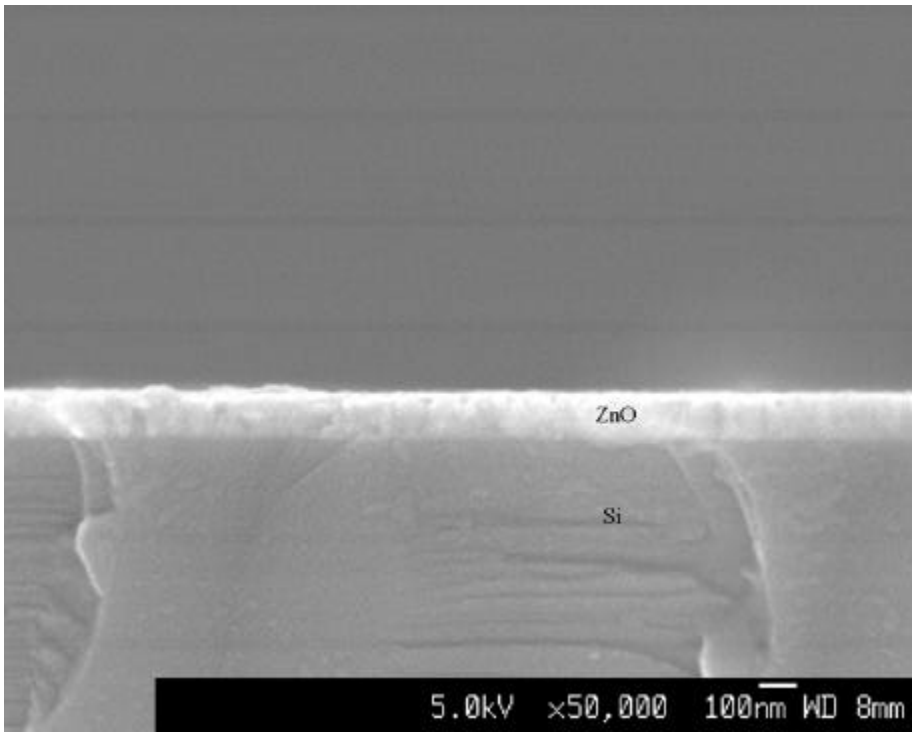


**Figure 2.** Cross-sectional view of the rf sputtered ZnO film deposited on *n*-Si.

tance–voltage (*C–V*) curve is commonly used to characterize the border traps.

Figure 3 shows the high frequency (1 MHz) *C–V* (HFCV) characteristics of $SiO_2$/ZnO/*n*-Si MIS capacitors with a gate bias sweep from + 5 to – 5 V and back to + 5 V at a rate of 0·1 V $s^{-1}$. The gate voltage was swept from inversion to accumulation to get a forward HFCV and from accumulation to inversion to get a reverse HFCV. These bidirectional HFCV curves exhibit a hysteresis. The hysteresis occurs due to the gate bias at which electrons fill the traps being different from the point at which the electrons leave the trap and/or due to the difference between the capture and emission times of the border traps (Fleetwood *et al* 1993). The hysteresis voltage ($\Delta V_H$) is found to have a value of 0·12 V. The appearance of a broad hysteresis and the significant shift in the flatband voltage indicate the presence of a large number of trapped charges at the interfaces. The amount of hysteresis is a measure of border trap and is given by

$$Q_{bt} = \frac{C_{ox}\Delta V_H}{qA}, \tag{1}$$

where $C_{ox}$ is the gate oxide capacitance in accumulation region, $q$ the electronic charge, and $A$ the gate area. $Q_{bt}$ was found to be $3{\cdot}9 \times 10^{10}$ $cm^{-2}$.

Figures 4 and 5 show the frequency dispersion of the *C–V* and *G–V* curves, respectively. The frequency dispersion in accumulation is usually attributed to the formation of an inhomogeneous layer at the $SiO_2$/ZnO interface. The capacitance of such a layer acts in series with the insulator capacitance causing frequency dispersion of capacitance in the accumulation. The frequency dispersion in depletion region is due to the presence of interface traps. The total capacitance in inversion increases with decreasing frequencies. This is because an inversion layer beyond the gate governs the response time of the minority carriers. The conducting inversion layer affects an a.c. current flow along the inversion layer which spreads laterally over an area that is much larger than the gate area. If the time constant of the minority charge carriers is comparable to the frequency, an additional capacitance is included. The conductance technique is used to determine the interface state density throughout the depletion region. From the *G–V* curves at different frequencies, the equivalent parallel conductance ($G_m$) is extracted for a single level interface state, characterized by time constant $t$, and is written as (Nicollian and Brews 1982)

$$\frac{G_m}{wC_{acc}} = \frac{[qD_{it}wt]}{(1+w^2t^2)C_{acc}}, \tag{2}$$

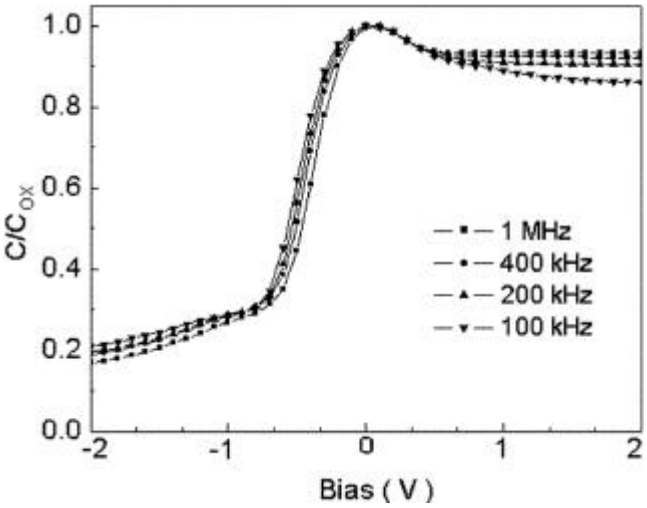


**Figure 4.** Frequency dispersion of *C–V* characteristics of MIS capacitors on ZnO films.

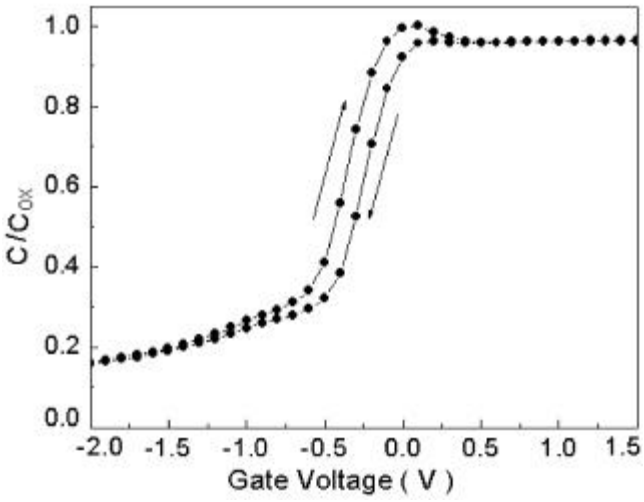


**Figure 3.** HFCV hysteresis of MIS capacitors on ZnO/*n*-Si for voltage sweep from inversion to accumulation and back to inversion.

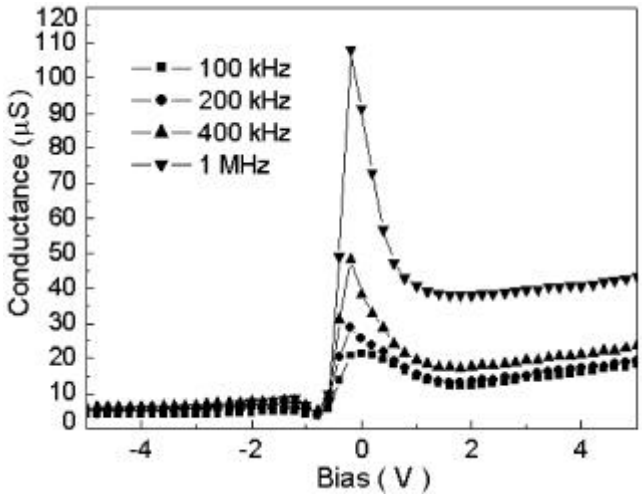


**Figure 5.** Frequency dispersion of *G–V* characteristics of MIS capacitors on ZnO films.

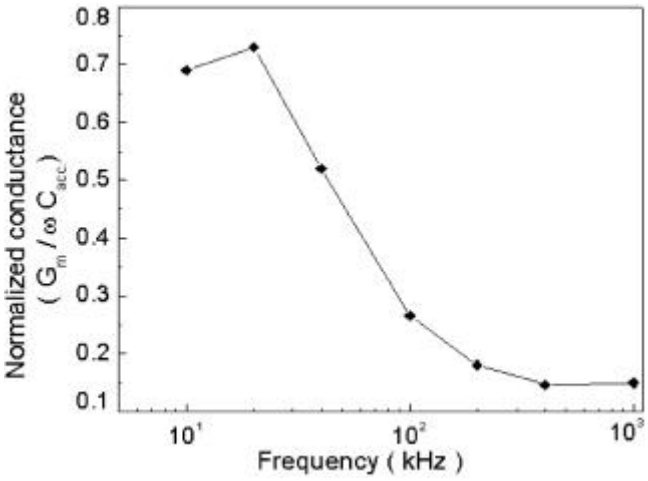


**Figure 6.** Plot of normalized equivalent parallel conductance as a function of frequency.

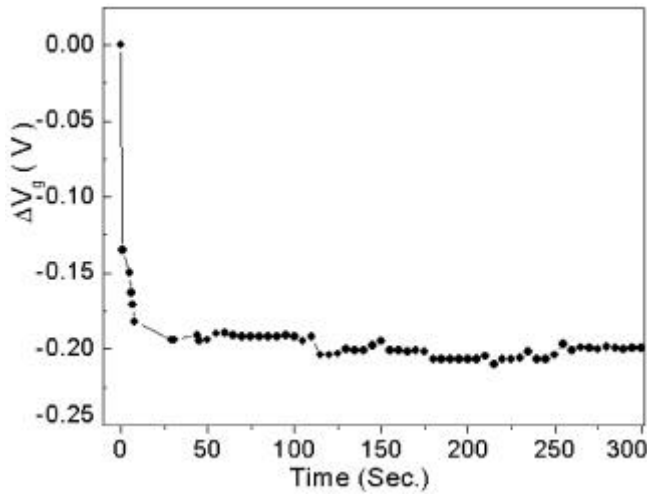


**Figure 7.** Gate voltage shift vs stress time under constant current stressing (7·6 mA $cm^{-2}$).

where $D_{it}$ is the density of interface states, $C_{acc}$ the insulator capacitance, $q$ the electronic charge and $w$ the frequency. When a continuum of interface states is present, this expression is modified as

$$\frac{G_m}{wC_{acc}} = \frac{[qD_{it}]}{2wtC_{acc}} \ln(1+w^2t^2). \quad (3)$$

The maximum value of $G_m/wC_{acc}$ is obtained for $wt = 1$ in (2) (single time constant model) and for $wt = 1{\cdot}98$ in (3) (continuum model). Figure 6 shows the plot of normalized equivalent parallel conductance ($G_m/wC_{acc}$) vs frequency. The value of $D_{it}$ was found to be $6{\cdot}84 \times 10^{11}$ $cm^{-2}$ $eV^{-1}$ for single time constant model (2) and $8{\cdot}52 \times 10^{11}$ $cm^{-2}$ $eV^{-1}$ for the continuum model (3) from figure 6.

The fixed oxide charge density ($Q_f/q$) was found to be $1{\cdot}048 \times 10^{11}$ $cm^{-2}$ calculated from the relation

$$Q_f/q = \frac{[C_{ox}(f_{ms} - f_F - V_{FB})]}{Aq}, \quad (4)$$

where $C_{ox}$ is the oxide capacitance in accumulation region, $f_{ms}$ the metal semiconductor work function difference, $f_F$ the Fermi potential of the ZnO semiconductor and $V_{FB}$ the flat-band voltage.

The charge trapping behaviour of the samples studied by continuously monitoring the change in gate voltage ($\Delta V_g$) required to maintain a constant current of 7·6 mA $cm^{-2}$ under gate injection is shown in figure 7. A significant negative gate voltage change indicates the hole trapping and the shift occurs because of combined effect of reduced electron trapping and positive charge due to slow donor type states (Senapati *et al* 2000).

The effect of constant current stressing ($J = 5{\cdot}0$ mA/$cm^2$) on Fowler–Nordheim (F–N) tunneling characteristics of $SiO_2$/ZnO/*n*-Si films with different stressing times, 100 s and 500 s, are shown in figure 8. It is observed that stress induced leakage current (SILC) is not significant

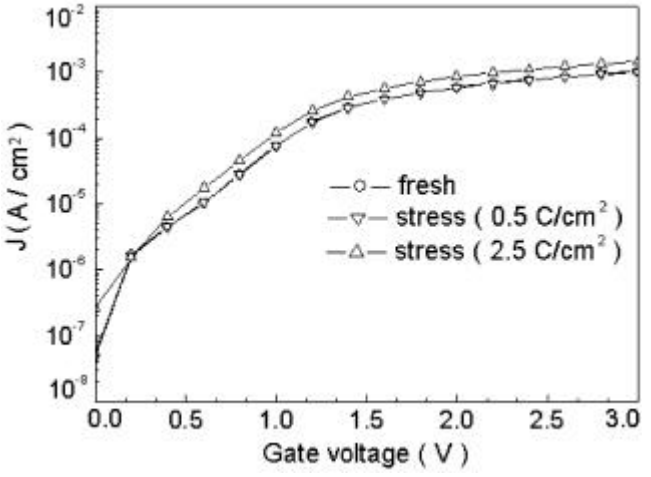


**Figure 8.** *J–V* characteristics before and after constant current stressing (5·0 mA $cm^{-2}$).

for 100 s stressing because of low trap generation. However, for 500 s stress at same current, the leakage current increases, which indicates the generation of localized charges and trap states near the injection interface.

## 4. Conclusions

The deposition of oxide films from TEOS plasma at a low temperature (< 200°C) on ZnO/*n*-Si has been demonstrated. Physical characterizations of the films were investigated using AFM and SEM. The charge trapping behaviour and SILC studies indicate a low trap generation under Fowler–Nordheim constant current stressing. Based on good electrical properties and reliability observed, it may be concluded that the deposited oxide films on ZnO/*n*-Si layer may find applications in microelectronics devices.

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