

Semiconductor applications of plasma immersion ion implantation technology

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Abstract. Many semiconductor integrated circuit manufacturing processes require high dose of implantation at very low energies. Conventional beam line ion implantation system suffers from low beam current at low energies, therefore, cannot be used economically for high dose applications. Plasma immersion ion implantation (PIII) is emerging as a potential technique for such implantations. This method offers high dose rate irrespective of implantation energy. In the present study nitrogen ions were implanted using PIII in order to modify the properties of silicon and some refractory metal films. Oxidation behaviour of silicon was observed for different implantation doses. Diffusion barrier properties of refractory barrier metals were studied for copper metallization.

Keywords. Plasma immersion ion implantation; oxidation rate; gate dielectric; diffusion barrier; copper metallization.

1. Introduction

Decreasing device dimensions of devices in integrated circuits (IC) from one generation to other, put many new demands on the ion implantation front. Decreasing cost of integrated circuits also necessitate cost effective processing techniques with high productivity options. Plasma immersion ion implantation (PIII) is the new technique that is emerging as promising candidate for ion implantation in low energy and high dose regime (Qian *et al* 1991). Although PIII was initially developed for metallurgical applications, now many semiconductor applications of this technique are being developed. Shallow junction implantation, deep trench doping, manufacturing the silicon-on-insulator (SOI) substrates, selective electroless copper deposition, thin film transistor hydrogenation, etc are the major applications (Chu and Chan 1995).

This technique offers many advantages over conventional beam line ion implantation like high dose rate, less sample charging and heating, no requirement of target or beam manipulation, compatibility with other IC processing tools, handling capability of large and complex non-planer samples, etc (Ensigner 1996). This technique also offers cost advantage in terms of initial investment and operational expenses. Since no mass separation is employed, multi charge ion species and contamination implantation are the limitations of PIII.

In PIII the sample is placed on a conducting substrate in a vacuum chamber and plasma is generated of ions to be implanted. Then negative voltage pulses are applied to

the wafer immersed in plasma. A plasma sheath will be created around the wafer and positive ions will accelerate through it and result in an implanted flux to all the exposed surfaces. Thus unlike conventional ion implantation in PIII no ion extraction and acceleration takes place, rather wafer get implanted while merged in plasma (Junes *et al* 1996).

This paper presents results of our studies carried out for altering the oxidation rate of silicon and nitriding the refractory metals to act as diffusion barrier for copper metallization.

2. Experimental

Silicon wafer of *n*-type and (100) orientation were cleaned with the standard cleaning method. All the samples were given a dip in diluted (5%) hydrofluoric acid (HF) to remove native oxide. Then an oxide layer of 40 Å was thermally grown on one set of samples. This thin oxide layer acts as screen layer to avoid ion channeling and avoid the silicon surface from contaminants. Immediately after cleaning, other sets of silicon samples were deposited with 600 Å titanium (Ti) and tantalum (Ta) films using d.c. sputtering. Then nitrogen was implanted using PIII in all the samples of SiO₂/Si, Ti/Si, and Ta/Si structures. In order to avoid cross contamination, samples of Si, Ti/Si and Ta/Si were implanted in different runs.

PIII system used in these experiments, as shown in figure 1, employs thermal plasma generated using impact ionization of electrons emitted from heated filament. Detailed description of system can be found elsewhere in literature (Mukherjee and John 1997). Before implantation,

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chamber was evacuated to a base pressure of 1×10^{-4} mbar. Nitrogen gas was introduced in the chamber and working pressure of 5×10^{-4} mbar was achieved by controlling the gas flow. Implantation was done by applying biasing pulses of -10 kV amplitude and $40 \mu\text{s}$ duration at 0.1 Hz frequency. Applied pulses and resulting ion current were measured using an oscilloscope. Final implantation dose was estimated using pulse parameter, sample area, and coefficient of the secondary emission (Rajkumar *et al* 2001). Frequency of the pulses was changed corresponding to different doses by keeping implantation time and other parameters constant.

Then silicon samples implanted at various doses were oxidized in dry oxidation cycle at 1000°C for 10 min. Before oxidation screen oxide layer grown earlier was removed in diluted HF. Thicknesses of the resulting oxide films were measured using ellipsometry. Samples with Ti and Ta films were metallized with copper using d.c. sputtering. Then samples were annealed at various temperatures. Diffusion behaviour of copper in underlying material was measured with change in sheet-resistivity of films.

3. Results and discussion

Nitrogen dose dependant oxidation behaviour of silicon is depicted in figure 2. It can be observed that oxidation rate decreases with increased dose in the range of 10^{14} to 10^{15} ions/cm². The reduction in oxidation rate is attributed to a surface rate limited oxidation reaction (Doyle *et al* 1995). It is believed that during implantation nitrogen ions make bond with silicon and thus limits the availability of silicon atoms ready for oxidation. At doses higher than 10^{15} ions/cm² top layer of silicon becomes fully nitrided and no oxidation takes place. These altered oxidation rates of silicon can be used to achieve multi

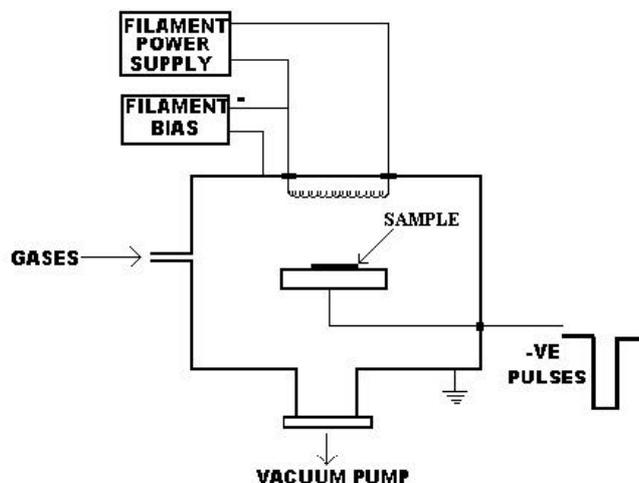


Figure 1. Schematic representation of plasma immersion ion implantation system.

thickness gate oxides in a self aligned manner, which are required for integration of different type of devices on single chip. This method can also be employed to nitride the gate oxide. Degree of nitridation (oxygen to nitride ratio) using PIII can be controlled more accurately as compared to annealing the oxides in nitrogen containing gases.

Figure 3 shows the change in sheet-resistivity as a function of annealing temperature for Cu/Si (no barrier film), Cu/Ti/Si (un-implanted barrier film) and Cu/Ti(N)/Si (barrier film implanted with nitrogen) structures. Annealing of Cu/Si at a temperature of 200°C leads to an increase in sheet resistance, which is indication of some high resistivity copper silicide phase formation. Cu/Ti/Si structure shows constant sheet resistance up to 400°C . At higher temperature it increases abruptly, this increase may be due to failure of Ti barrier. Here copper crosses

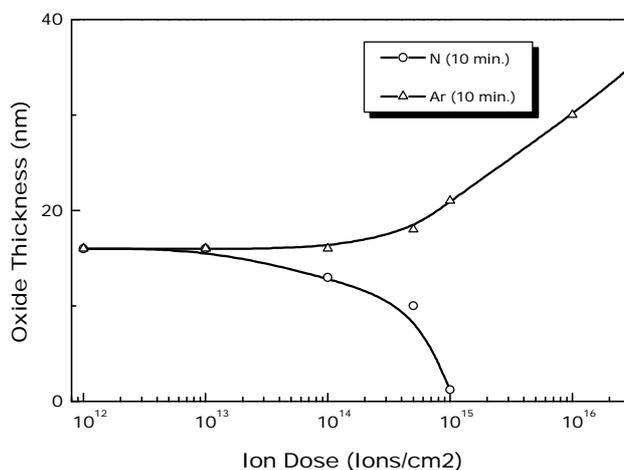


Figure 2. Oxidation rate of silicon implanted with nitrogen and argon at different doses.

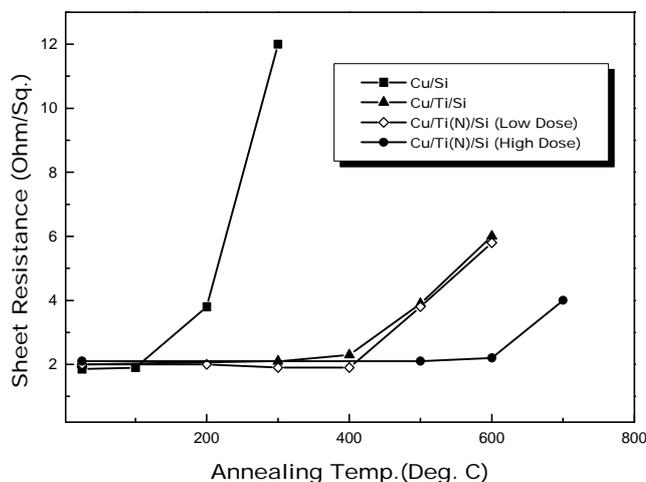


Figure 3. Sheet resistance of Cu/Si, Cu/Ti/Si and Cu/Ti(N)/Si structures as a function of annealing temperature.

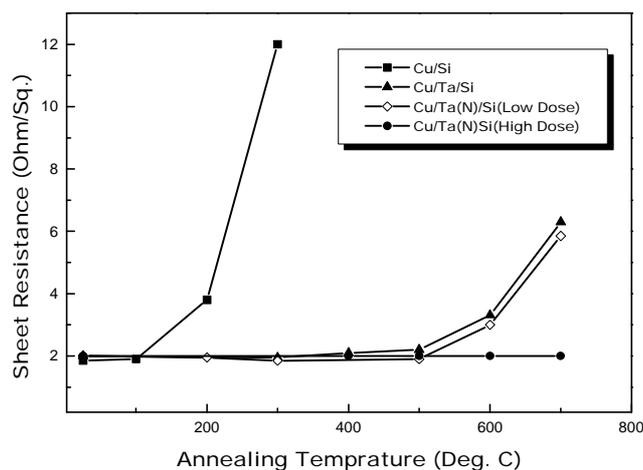


Figure 4. Sheet resistance of Cu/Si, Cu/Ta/Si and Cu/Ta(N)/Si structures as a function of annealing temperature.

the barrier film and reach Si–Ti interface in order to form copper silicide type phase. Nitrogen implantation of the order of 10^{15} ions/cm² in Ti does not show any improvement in its diffusion barrier properties. Sample implanted with 10^{17} ion/cm² dose of nitrogen shows that sheet resistance remains constant up to 600°C and a slight increase is noticed at 700°C. It indicates that the high dose of implanted titanium is more capable to stop penetration of copper through barrier layer. Reason for this improvement may be supposed to be the formation of some nitride phase after implantation of nitrogen in it (Wang *et al* 1990). This nitride phase may not have occurred in case of low dose implanted sample. This fact is confirmed by XRD results also.

Sheet resistance as a function of annealing temperature is plotted in figure 4 for Cu/Si, Cu/Ta/Si and Cu/Ta(N)/Si structures. Annealing of Cu/Si at a temperature of 200°C leads to an increase in sheet resistance while in Cu/Ta/Si it remains constant up to 600°C. In case of Cu/Ta(N)/Si (10^{15} ion/cm² dose) a small increase in sheet resistance is

observed in samples at 700°C while no increase is observed in case of Cu/Ta(N)/Si (10^{17} ion/cm² dose) sample. Sheet resistivity measurement shows that TaN layer with high dose (10^{17} ion/cm²) of nitrogen stops intermixing to occur. Results were also confirmed by X-ray diffraction (XRD) and scanning electron microscopic (SEM) techniques.

4. Conclusions

Above results suggest PIII can be employed to alter the oxidation rate of silicon and to synthesize the diffusion barrier for copper metallization. This technique offers high dose rate and different implantation doses can be achieved by changing the frequency of applied pulses.

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References

- Chu P K and Chan C 1995 *Semicond. Int.* 165
- Doyle B, Soleimani H R and Philipossian A 1995 *IEEE Electron. Device Lett.* **16** 301
- Ensigner W 1996 *Nucl. Instrum. & Meth. Phys. Res.* **B120** 270
- Junes E C, Linder B P and Cheung N W 1996 *Jpn. J. Appl. Phys.* **35** 1027
- Mukherjee S and John P I 1997 *Surf. Coat. Technol.* **93** 188
- Qian X Y, Cheung N W, Liberman M A, Current M I, Chu P K, Harrington W L, Magee C W and Botnick E M 1991 *Nucl. Instrum. & Meth. Phys. Res.* **B55** 821
- Rajkumar, Kumar M, George P J, Chari K S and Mukherjee S 2001 *Physics of semiconductor devices* (eds) Vikram Kumar and P K Basu (New Delhi: Allied Publishers Limited) Vol. 2 p. 1178
- Wang S Q, Raaijmakers I, Burrow B J, Sailesh S, Shailesh R and Kim K B 1990 *J. Appl. Phys.* **68** 5176