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Gallium arsenide digital integrated circuits

D BHATTACHARYA
Department of Electronics and Electrical Communication Engineering, Indian Institute of Technology, Kharagpur 721 302, India

Abstract. The motivations behind the development of GaAs integrated circuits (IC) are two-fold: to integrate high speed logic with optical sources and to meet the increasing demand of realising LSI/VLSI with higher speed and lower power dissipation for large scale computer applications. GaAs gigabit circuits have been growing in complexity to more than 3000 gates on a single chip. Although this is encouraging, more efforts are needed to improve production yield. By far the most work on GaAs digital IC has been done using MESFET as the active devices. MOSFET technology is yet to mature from the practical IC point of view. The logic gate types used in circuits are predominantly of the enhancement-mode driver and depletion-mode load configuration (E/D).

A brief survey of the state-of-the-art of GaAs digital IC is presented. Implemented circuits are described and compared with those achieved through various technologies. GaAs gate arrays, multipliers, accumulators and memories are discussed. At liquid N_2-temperature, a switching time of 5·8 ps/gate has been achieved for 0·35 μm gate devices. This and similar other results lead to the conclusion that at the VLSI level of future Gbit circuits, GaAs devices in the form of HEMT operated at 77 K can outperform Si-devices. At LSI complexities, experimental GaAs MESFET and 300 K HEMT have a lead on Si-circuits–it is then this range in which Gbit/GaAs should find their application.

Keywords. GaAs digital integrated circuits; very large scale integration; heterojunction bipolar transistor; high electron mobility transistor; Schottky barrier gate.

1. Introduction

The present day integrated circuit (IC) industry is dominated by silicon, but the demand for high speed signal processing and large scale computer systems has focussed attention on alternative materials and devices. Among the 'non-silicon' materials, GaAs has been investigated quite extensively for realising high speed digital IC. Although laboratory test circuits fabricated on GaAs have shown much promise, commercial viability in terms of the level of integration, yield and design testability is yet to be established (Steger *et al* 1986).

Early enthusiastic claims that GaAs is potentially five to six times faster than silicon, is based on the ratio of the low field electron mobilities but this claim is unlikely to be valid in operational circuits (Bosch 1984). Investigations have revealed that the speed advantage of GaAs metal semiconductor field effect transistor (MESFET) over Si-bipolar and Si MESFET is between 2:1 and 3:1 for customised serial structure circuits. But this advantage will be largely lost in interconnect-intensive parallel structure configurations. The present state-of-the-art scarcely points to the possibility that GaAs will totally replace Si, but it will be wrong to underestimate the capabilities of GaAs-based materials which can be configured into a variety of hetero-structures with a wide range of exploitable physical phenomena. The switching performances of high electron mobility transistor(s) (HEMT) and heterojunction bipolar transistor(s) (HBT) appear to provide GaAs with a significant lead.

The aim of this paper is to place GaAs digital IC in proper perspective. Those

design approaches which are finding increasing applications in digital IC are discussed. Comparisons are made with typical logic family performances for different technologies on the basis of available data. Likely improvements in performance vis-a-vis applications in the near future are also summarised.

2. High speed applications – material choice

The realization of ultra-high speed very large scale integration (VLSI) necessitates achieving: (1) a very low gate propagation delay (τ_d), (2) a low power per gate (P_d), (3) extremely low speed power product ($P_d\ \tau_d$), (4) very high gate densities, and (5) a very high yield. These in turn generate a number of requirements for the characteristics of the active devices needed to implement such circuits.

For a given power dissipation, the maximum allowable number of gates per chip or the maximum speed power product can be calculated for a given clock frequency, f_c using the equation

$$P = 2Nf_c(P_d\ \tau_d), \ldots \tag{1}$$

where N is the number of gates per chip.

The dynamic switching energies ($P_d\ \tau_d$) must exceed the stored energy on the switched capacitance C (which is the sum of input capacitances of the fan-out of the loading gates plus the parasitic capacitance) i.e.

$$P_d\ \tau_d > \tfrac{1}{2}C(\Delta V_L)^2, \ldots \tag{2}$$

where ΔV_L is the logic voltage swing. More precisely the $(\Delta V_L)^2$ term is the product of ΔV_L and V_{DD} (Eden 1980). Hence the logic swing voltage as well as the power supply voltage must be kept small for low values of $P_d\ \tau_d$. The requirement of small logic voltage swings dictates that the threshold voltages of the active devices involved should be very precisely controlled. In fact the standard deviation of the threshold voltages should preferably be less than 5% of the logic voltage swing (Eden 1980).

The current gain-bandwidth product of a field effect transistor (FET) in this near small threshold $(V_{gs} - V_T)$ is given by

$$f_T = \frac{g_m}{2\pi C_{gs}} = \frac{\mu_n}{2\pi L_g^2}(V_{gs} - V_T). \tag{3}$$

The propagation delay of a transistor with N similar devices is given by

$$\tau_d = \frac{1}{\pi f_T} = \frac{2C_{gs}}{g_m}. \tag{4}$$

In order to have very low propagation delay, the devices must have high g_m values which can be maximised by reducing the gate length. Dependence solely on the reduction of L_g (i.e. placing unreasonable pressures on the required lithographic precision) will seriously affect the yield. Improvement can also be effected by using a semiconductor having higher channel mobility μ_n. GaAs with about 6 times higher mobility than those for correspondingly doped bulk silicon is the natural choice for high speed FET devices. Very high electron channel mobilities of HEMT devices render a high value of g_m and f_T ideally suited for ultra-high speed digital circuits. The capacitance C (eqn. 2) is to a large extent determined by the substrate capacitance of

interconnecting lines; here again GaAs has an advantage over Si as it is possible to render GaAs into an electrically insulating state. For VLSI circuits, however, there will be large interconnections causing fringing and cross-over capacitances to dominate – which are independent of the material used. A detailed discussion on the crucial role of the interconnects in determining the power performance of the technology has been given by Solomon (1982). Other properties of GaAs, such as improved radiation tolerance and operating temperature range can be important in some applications (Milutinovic 1986).

For very short drift lengths, non-equilibrium effects may increase drift velocity and mobility and thus device speed. The velocity overshoot effect in GaAs leads to improvements in g_m and switching speed in sub-micron devices. The maximum electron velocity (ballistic) in GaAs has been found to be around 10^8 cm/s (Hess and Iafrate 1988); the steady state velocity, however, is smaller than 10^7 cm/s in GaAs for electric fields which are far above the Gunn threshold ($\approx$3·4 kV/cm) (Shichijo and Hess 1981). The impurity scattering will reduce both the steady state values and the overshoot. Although the overshoot effect is expected to be much smaller in Si than in GaAs, a significant increase of the average drift velocity (about 1·5 times its bulk V_{sat}) was found with decreasing gate length (Hess and Iafrate 1988).

The lack of passivation due to the absence of a native oxide of GaAs eliminates the possibility of MOS-type circuits which form the basis for the present day VLSI. GaAs substrates are mechanically much more fragile than silicon ones, thus causing handling problems. Insufficient wafer uniformity, purity and flatness are the main reasons for still low IC production yields (Bosch 1984).

Chromium-doped GaAs substrates have dislocation densities typically of the order of $10^3/cm^2$. High dislocation densities and uneven Cr-distribution often lead to excessively high variations in V_T. The diffusivity of Cr in GaAs is about 7×10^{-14} cm^2/s (Lindquist and Ford 1982) at a typical epigrowth temperature of 750°C. To produce an epi-layer of 0·25 μ thickness (growth time $\approx$1 min), the Cr penetrates a distance of 0·02 μm which is nearly 10% of the total active layer thickness. The Cr level near the interface reduces the electron concentration and drift mobility. To prevent out-diffusion of Cr into low resistivity FET channel layer on top of the SI substrate, buffer layers are sometimes provided. Buffer layers having a larger bandgap (GaAlAs) have reduced injection of channel electrons into the buffer. Undoped ingots of high resistivity have also been produced using the high pressure-LEC technique (Lindquist and Ford 1982; Bosch 1984). This method has the additional advantage of providing round larger area GaAs wafers. LEC-grown GaAs crystals contain dislocation densities in the 10^4 to $10^6/cm^2$ range (Noel *et al* 1988). However, significant reduction of the thermal-stress induced dislocations in three-inch-wafer SI GaAs has been achieved by the use of isovalent In-doping.

It may be noted from (2) that $P_d\tau_d$ products can be achieved by operating with very low logic voltage swing. This may be realised with the extremely uniform threshold devices showing higher degree of nonlinearity (rapid increase in transconductance for small voltage swing, ΔV_L, above the threshold). The threshold voltage should therefore be highly insensitive to normal processing parameter variations such as horizontal dimensions, vertical dimensions, doping level variations etc. In GaAs MESFET the pinch-off voltage is insensitive (Eden 1980) to

horizontal geometry variations (e.g. L_g) but is sensitive to both the thickness and doping level in the channel layer. A reasonable value of the pinch-off voltage uniformity achieved over a GaAs IC wafer is $\sigma_{V_p} = 50$ mV; a value much too high for low logic swing operation since, in order to accommodate the statistical variation in V_p, the logic voltage swing must be at least 20 times the standard deviation of V_p. The thermal noise level $V_n = kT/q$ is only 6·64 mV at 77 K, and logic swings of $10\,kT/q$ or higher are adequate, while a logic voltage swing of 100 mV requires a $\sigma_{V_p} < 5$ mV. In comparison, the threshold voltage for the heterojunction bipolar transistor (HJBT) (V_{BE} for specific I_C) is determined mainly by the energy gaps of the base and emitter regions rather than geometrical and doping factors. The threshold uniformity should be excellent ($\sigma_{V_{BE}}$ few mV) (Eden 1980), hence the logic swing is decided by the thermal noise level.

3. GaAs IC devices

The Schottky barrier gate field effect transistor (MESFET) is the key device used in GaAs IC. If the device channel is conducting at zero gate input voltage, a depletion-mode (normally ON) device is obtained. The D-FET has the largest current per device width of any GaAs FET and is the most widely used device (figure 1a). The large logic swings (typically 1 V) associated with D-FET circuits avoid excessively stringent requirement for FET pinch-off voltage uniformity. Because regions of the source–drain channel not under the gate are conductive in D-FET, precise gate alignments are not necessary. By decreasing the channel thickness, a normally OFF enhancement mode FET (EFET) with a positive threshold voltage can be fabricated (figure 1b). The advantage of EFET circuits is that unlike the DFET-only circuits, level shifting is not required in the logic gate. However the voltage swing of a circuit using EFET is limited by the forward turn-on voltage of the Schottky barrier transistor gate (0·71). This limits the noise-immunity of the gate and places stringent fabrication requirements on threshold voltage control and uniformity.

Special GaAs/$GaAl_xAs_{1-x}$ FET devices promise improved performance (Abe *et al* 1982) over typical EFET or DFET. One is the high electron mobility transistor (HEMT), also known as the modulation-doped FET (MODFET) (figure 1c). Part of the AlGaAs layer is heavily doped to provide mobile electrons for conduction. The GaAs layer is undoped, which reduces impurity scattering to allow maximum electron mobility. The free electrons diffuse from the heavily doped AlGaAs to the undoped GaAs, where they are confined by the energy barrier created at the heterojunction. Conduction takes place in the undoped GaAs where the electrons can travel at a high velocity. Electron mobility can be further enhanced by operating the device at low temperatures (about 77 K).

Enhancement and depletion-mode devices can be fabricated in HEMT technology. HEMT have a higher forward turn-on voltage of the Schottky-barrier gate than do the MESFET. This provides for a larger noise margin in enhancement/depletion (E/D) logic circuits. This feature is critical for obtaining higher yields at larger levels of integration. Although HEMT are fabricated from a more complex multilayer semiconductor structure, new fabrication methods such as molecular beam epitaxy (MBE) or metal-organic chemical vapour deposition (MOCVD) may allow them to become the dominant transistor structure in GaAs LSI circuits (Morkoc and Solomon 1984).

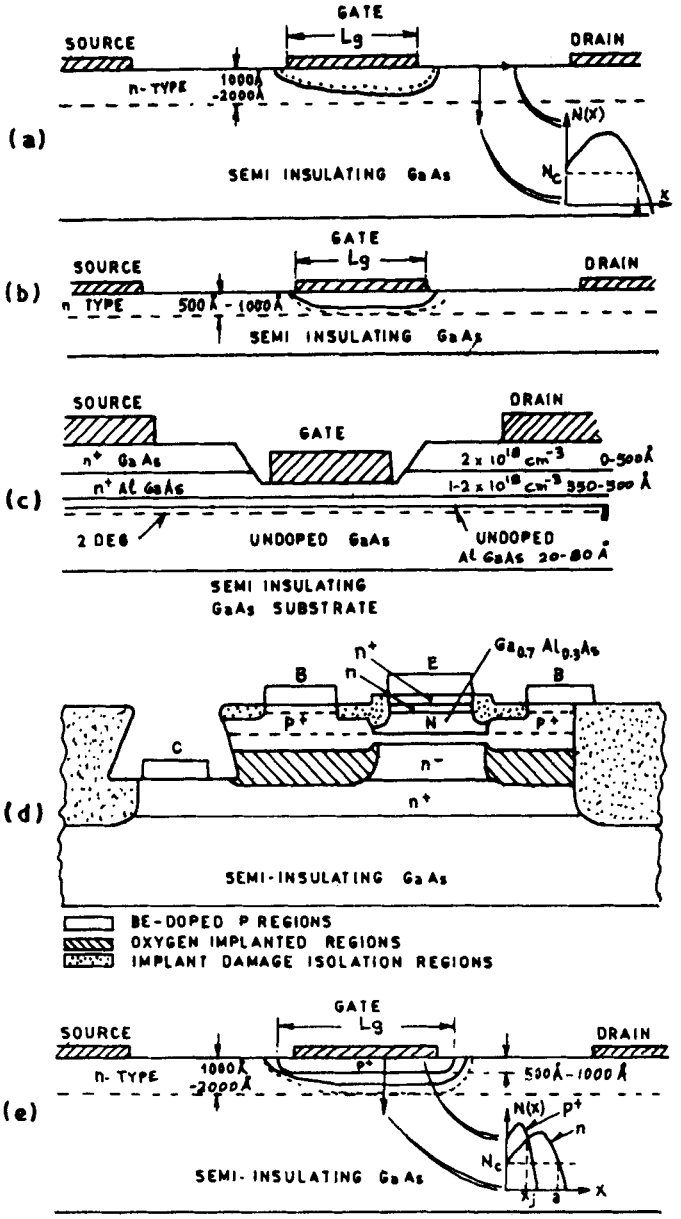

Figure 1. GaAs transistors. (**a**) Shows a depletion mode field effect transistor (DFET) with a threshold voltage of $-0{\cdot}7$ V to $-2{\cdot}5$ V, a high current capacity of 0·1 mA/μm, and high power dissipation of 0·25 mW/μm. (**b**) shows an enhancement mode field effect transistor (EFET) with a threshold voltage greater than 0 V, a low current capacity of 0·01 mA/μm, low power dissipation of 0·01 mW/μm, and tight process controls of less than ± 50 Å. (**c**) shows a high electron mobility transistor (HEMT), which is an enhancement and depletion device with a higher gate forward bias voltage of 0·7 to 0·9 V and high transconductance 450 mS/mm (300 K) to 520 mS/MM (77 K). (**d**) shows a heterojunction bipolar transistor (HBT) and (**e**) shows a junction field effect transistor (JFET) with large sidewall capacitance and tight process controls. Complementary devices are available.

Another promising GaAs technology produces heterojunction bipolar transistor (HBT) (figure 1d) (Eden 1980; Kroemer 1984). An HBT is fabricated with different semiconductor materials in its emitter and base regions. The heterostructure at the emitter-base junction allows the base to be heavily doped, reducing the parasitic base resistance while the transistor current gain is maintained. In GaAs technology, the emitter is AlGaAs and the base and collector are GaAs. Figure 1e shows a junction FET. Although these devices have reduced speeds compared to MESFET, GaAs JFET devices have the advantage of higher turn-on voltage of the gate (0·9 to 1·2 V) and the availability of both *p*- and *n*-channel devices. These make the devices attractive for low power LSI circuit implementations such as memories.

Figure 2 (Morkoc and Solomon 1984) compares the speed-power performance of important transistor technologies including HEMT (MODFET). Only the Josephson junction technology offers comparable propagation delay and lower power dissipation than the N_2-cooled HEMT. JJ devices however require liquid He-cooling for optimal operation, are highly sensitive to impurities and the thickness tolerance of deposited material is only 1Å. GaAs IC even with not-so-mature HEMT will far outweigh the JJ logics in terms of costs. Maximum transconductance is higher for the HEMT – 400 mS/mm of gate width at 77 K and 270 mS/mm at 300 K vs 230 mS/mm for the MESFET and 80 mS/mm for the MOSFET which normally operate at room temperature. For logic gates having voltage swings of 0·5 V for HEMT at 77 K, 0·8 V for MESFET and HEMT at 300 K and 2·5 V for MOSFET, the power dissipations are in the ratio of 1:2·6:25. For devices used as 50-ohm drivers, gate widths are 75, 150, 200 and 400 micrometers respectively for the HEMT (77 K), HEMT (300 K), the MESFET (300 K) and the MOSFET (300 K)

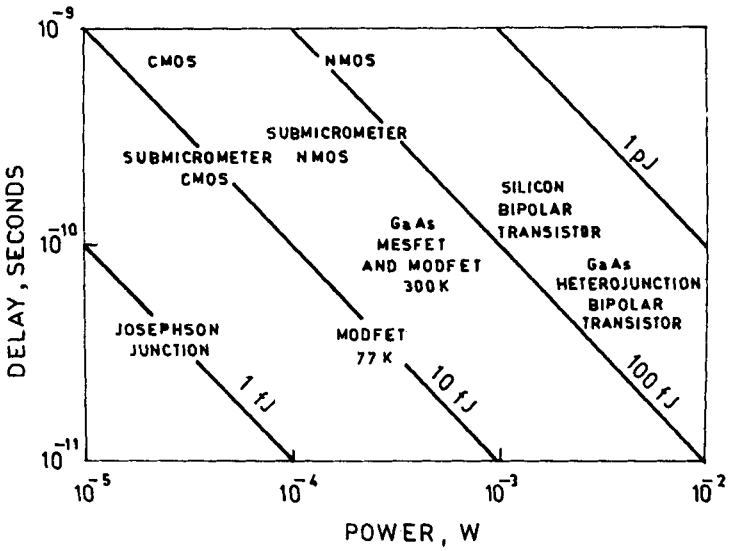

Figure 2. Power-delay continuums of important transistor technologies are indicated generally by circles, based on conservative design. The diagonal lines are lines of constant power-delay product. Only the Josephson junction offers comparable propagation delay and lower-power dissipation than the nitrogen-cooled (77 K) MODFET. The system-integration and -fabrication difficulties of the Josephson junction, however, appear insurmountable in the near future.

(Morkoc and Solomon 1984). The parasitic capacitance is less in GaAs devices, both HEMT and MESFET, because of the SI substrate. S-O-S MOSFET circuits share this advantage, but the advantage is getting eroded at higher levels of integration. The potential dimensional scaling of the HEMT, MESFET and MOSFET are comparable with minimum dimensions in the 0·1 to 0·2 micrometre range.

4. GaAs logic families

Buffered FET logic (BFL) and Schottky diode FET logic (SDFL) gate circuit approaches have been extensively employed for depletion mode GaAs IC. BFL circuits (Pengelly 1982; Long *et al* 1982) utilise relatively high pinch-off voltages ($-2{\cdot}5$ V) and level-shift diodes and have exhibited high power dissipation per gate (40 mW typical). Because of the high power dissipation, BFL is not suited for LSI complexity. Utilising ion-implanted planar approaches, low pinch-off (-1 V) MESFET may be fabricated and using two level shift diodes, the power dissipation can be kept at about 5 mW/gate and larger BFL circuits (≥ 200 gates) can be developed. The source follower output driver provides low sensitivity to fan-out loading and load capacitance.

The SDFL circuit approach offers large savings in area/gate (600 to 2000 μm^2) because of the very small sizes of the logic diodes and because of the fact that the diodes (Long *et al* 1982) being two-terminal devices require fewer crossings and vias than circuits using FET. This results in lower parasitic drain and source capacitances. The SDFL circuit approach permits high speed operation and provides lower power dissipation ($\sim 0{\cdot}2$ to 2 mW/gate).

Logic gates, employing enhancement mode FET are usually designed with direct-coupled FET logic (DCFL). These circuits have the lowest power consumption (about 50 to 300 μW/gate) (Larson *et al* 1986). There is no need for level shifting with DCFL gates, so power dissipation and packing density are greatly improved. A significant improvement of the directly coupled logic gate is to use a depletion mode active load. This active load sharpens the transfer characteristics and improves the speed and $P_d\tau_d$ product. However the fabrication of the depletion mode active load requires a carrier concentration profile which is different from that of the enhancement mode devices.

Since enhancement and depletion devices are also available in HEMT technology, HEMT circuits can also be realised with any of the above logic families. Normally -OFF enhancement-mode MESFET offers circuit simplicity because the logic gates require only one power supply. The permissible voltage swing is rather low however because Schottky barrier gates on GaAs cannot be forward biased above approximately 0·8 V without drawing excessive current. A desirable value for the logic swing is 0·5 V which dictates a very tight control in the fabrication of very thin active layers so that the FET is totally depleted at zero gate bias but has a high gm/unit gate width when the device is ON. The more difficult fabrication procedure of E-MESFET logic compared with D-MESFET logic can be partially overcome by the use of a *p-n* junction gate FET (JFET). The reason behind this is that a JFET can be biased to approximately 1 volt without excessive current being drawn (Zuleeg *et al* 1988). McDonnell–Douglas EJFET process uses selective implantation with Mg-ions to define *P*-gate region (Pengelly 1982). An alternative circuit

approach has been adopted by Thomson–CSF which tolerates a wider range of pinch-off voltages. The approach uses a so-called 'quasi-normally-off' logic (Lehovec and Zuleeg 1982). In this circuit approach, transistors operate as enhancement-mode devices with a pinch-off voltage close to zero, but whose actual value can be either positive or negative.

If production control alone dictates the circuit selection, BFL and SDFL have an edge over DCFL. This is because they are less affected by small changes in threshold voltage and have larger noise margins. Wide noise margins are required to obtain high production yield. It will be of course incorrect to think that the wide noise margins have anything to do with avoiding cross-talk or overcoming noises inherent in the circuit components.

Table 1, which is taken from Larson *et al* (1986) presents a comparative assessment of the logic-gate-level performance parameters. BFL gates typically demonstrate delays of approximately 90 ps and a sensitivity of 30 ps/FO.

5. Technology

The processing sequence of fabricating GaAs IC differs from organisation to organisation, but agencies like Rockwell International, LEP France, Plessey Corporation have developed a process technology in order to realise the advantages of ion implantation. The processing steps followed by Rockwell are described (Pengelly 1982; Eden and Welch 1982) with reference to a planar GaAs integrated circuit incorporating a FET, a level shifting and a switching Schottky diode. Fabrication of the device wafer is started by the deposition of a Si_3N_4 layer onto a flat, qualified, SI substrate – this layer remains on the slice during all subsequent fabrication steps. A first photoresist stage defines the device and circuit areas which require low dose implants such as the channels of FET. A shallow Se implant is then followed by a deeper n^+ implant for device contact areas or Schottky barrier switching diodes after exposure, encapsulation of the slice with Si_3N_4 and annealing at 850°C in an H_2-atmosphere. This high temperature anneal converts the shallow *n*-Se-implanted areas ($\approx$1500 Å thick) into the FET-active channel layers with pinch-off voltage dictated by the implant conditions. The n^+ implanted areas using sulphur at higher dosage provide a high conductivity region. Device contact areas are defined next with a standard photoresist and lift-off technique. After alloying the

Table 1. Typical logic family performance for different technologies.

Logic family	Speed (ps)	Fan-out sensitivity (ps/FO)	Capacitance sensitivity (ps/fF)	Power (mW/gate)
BFL (1 μm)	90	20	0·67	10·0
BFL (0·5 μm)	54	12	0·67	10·0
UFL (1 μm)	146	35	2·8	2·5
CII (1 μm)	100	40	2·22	0·36
DCFL (1 μm) (E/D)	54	35	1·84	0·25
HEMT (0·5 μm) (E/D) (77 K)	11	7	0·32	1·3

From Larson *et al* (1986).

ohmic contact area at 450°C, a photoresist operation is again performed to define the Schottky barrier metallization for the FETs and diodes. Ti–Pt–Au is used for the Schottky barriers as well as for the first layer circuit interconnections. A dielectric layer is then deposited onto the entire wafer as insulation for the second layer interconnection and dielectric for circuit capacitors. Via holes through the dielectric are used for interconnections between the first and second layers of metals. All these steps are sequentially shown in figure 3.

The 'normally off' condition of E-MESFET requires an extremely thin, lightly doped channel region. Such thin active layers are extremely surface-sensitive, highly

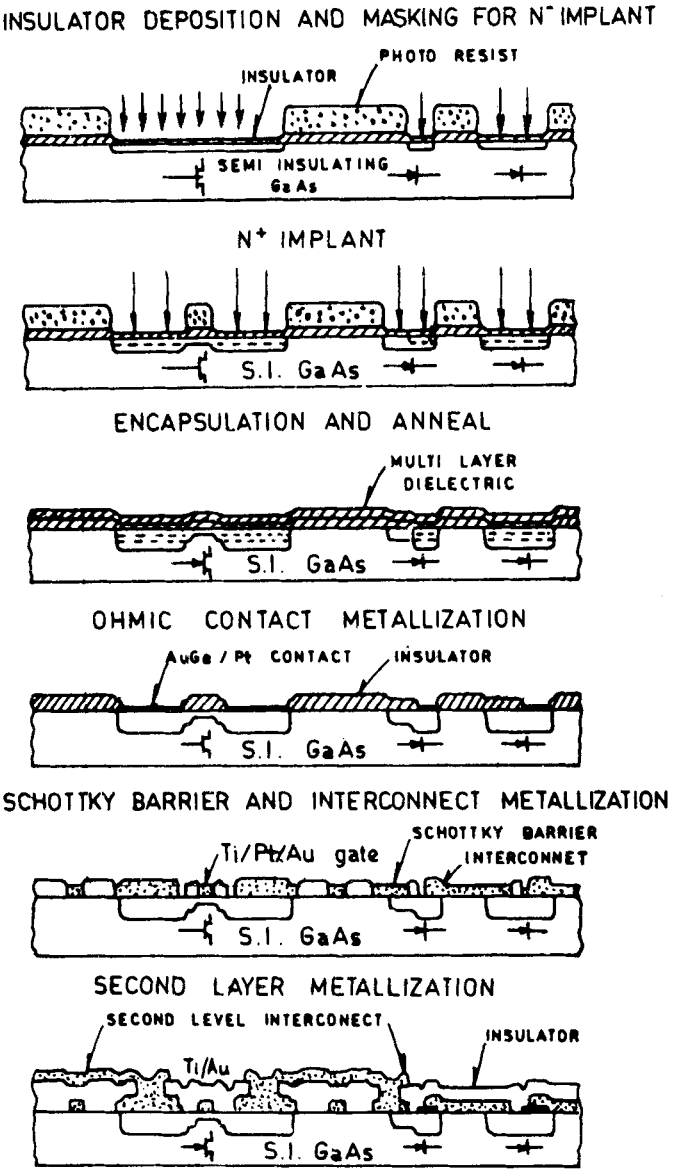

Figure 3. Planar SDFL GaAs IC fabrication steps.

resistive and difficult to control. More recently, E-MESFET have been constructed using techniques borrowed from self-aligned-gate (SAG) fabrication in Si-NMOS. The SAG technique uses the Schottky gate as a mask for implanting the source and drain regions of a device. This approach poses a problem of finding a gate metal system that can withstand the 800°C temperature required to anneal devices after ion-implantation. Fujitsu, among others, has overcome this problem using tungsten silicide gate metallization to fabricate 1 kb RAMS and 10 k transistors (3168-gate) 16×16 bit multipliers. The SAG process however produces high carrier concentration regions immediately adjacent to the gate depletion region, which influences gate threshold voltage. Recognition of this problem has led to the development of T-bar gate structures by laboratories such as Nippon Telegraph, Japan, Hughes Research Laboratories, California and Cornell University, Ithaca. The T-bar structure automatically places the heavily doped region 0·1 to 0·2 micrometers away from the critical gate channel depletion region, thus minimizing effects on threshold voltage while still ensuring low series resistance between the source and drain. Two other approaches need to be mentioned; JFET by McDonnell Douglas Corp. and the reactive gate approach of Toshiba Corp. Both these techniques use 'virtual' recessed gate structures, placing the gate below the channel surface region by *p*-type implantation or reaction between a platinum gate and the GaAs surface in the case of reactive gates.

LSI level complexity with HEMT has been realised (Watanabe *et al* 1987; Kajii *et al* 1988) by Fujitsu using the MBE growth technology and the selective dry etching process. The basic epi-layer was grown using MBE and in MBE growth a wafer with a low surface defect (less than $40/cm^2$) was necessary to obtain reasonable chip yield. For the selective dry etching process (gate fabrication), there is a great difference in the etching rates between GaAs and AlGaAs. The etching rates of GaAs and AlGaAs are 520 nm/mm and 2nm/mm respectively. Using this technique the gate recessing process was well controlled. The standard deviation in the threshold voltage was around 10 mV and 20 mV for E- and D-HEMT respectively. In the first stage of fabrication the active region was isolated by O^+-ion implantation, source and drain were metallized and non-selective wet chemical etching was used to etch the top GaAs layer as well as using a thin AlGaAs etching stopper for E-HEMT.

6. Implemented circuits

A ring oscillator consisting of chains of an odd number of inverters or logic gates (N) provides a propagation delay τ_d from the oscillation frequency through the relation $\tau_d = 1/2fN$. This represents intrinsic speed ($P_d \tau_d$ is also measured) since capacitive loading due to parasitics is generally minimum due to compact layout and fan-out of 1. In contrast, frequency dividers provide a more realistic picture of the overall performance of a particular circuit and device approach because fan-in, fan-out and capacitance loading are greater in an actual circuit. The fastest binary divider is complementary-clocked NAND/NOR implemented master–slave flipflop (MS-FF) with $f_{max} = 1/2\tau_d$. Other types which require only about half the number of gates are slower and achieve only frequencies $1/4\tau_d$ or $1/5\tau_d$ with D-type FF. NTT, Japan has fabricated a BFL MS binary frequency-divider with 0·5 μm gate FET which operates at 10·6 GHz with 258 mW power dissipation (Osapune *et al* 1986).

Using HEMT devices, Bell Laboratories reported a type D-FF divide by two circuits with maximum frequencies as 3·7 GHz and 5·9 GHz at 300 K and 77 K respectively with transistor gate lengths of 1 μm (Drummond *et al* 1986). The highest frequency results from Fujitsu (Drummond *et al* 1986) are for division up to 5·5 GHz at 300 K and 13 GHz at 77 K using a dual-clocked MS circuit with 0·4 μm gate length. OKI Electric, Japan has reported an ultrahigh speed complementary-clocked MS flipflop which used transmission gates and DCFL inverters to achieve a maximum toggle frequency of 14·4 GHz (Schneiderman 1988). A divide-by-8 frequency counter using EFET has demonstrated (Lindquist and Ford 1982) a maximum clock frequency of 3·8 GHz with a power dissipation of 1·2 mW/gate. This corresponds to a gate delay time of 66 ps and $P_d\tau_d$ product of 79 fJ.

Fast binary multipliers are required in high speed computing and signal processing applications. The level of complexity in a 8-bit multiplier is at the LSI-level, which requires about 3000 FET and 3000 Schottky diodes. Reported performance data of various parallel multiplier IC (Bosch 1984) is shown in table 2. NEC, Japan has reported a 12 × 12-bit multiplier with multiplication time 4 ns and chip power dissipation of 2·5 W (Vlahos and Milutinovic 1988). The low power dissipation of $\approx$2 mW/gate with 150 ps/gate propagation delay (lower power operation of 0·6 mW/gate was possible using lower V_P and marginally higher multiply time 6 ns) indicates that SDFL approach is suitable for the VLSI range of complexity, EFET approach is capable of providing improved performance, but is limited in yield.

Table 2. Implemented parallel multipliers.

Technology	Minimum dimensions	Multiplication	Chip power	Source
4 × 4 bit				
GaAs	1·4 μm	6 ns	39 mW	Toshiba '82
*e*MES	1·2	3·7	54	Fujitsu '82
JFET	1·5	3·5	70	Sony '83
Si CMOS	1·0	25	15	NEC '82
5 × 5 bit				
GaAs SDFL	1·0	3·8	180	Rockwell '81
6 × 6 bit				
GaAs	2·0	6·4	173	Fujitsu '82
*e*MES	2·0	10·6	350	Toshiba '84
8 × 8 bit				
GaAs SDFL	1·0	5·25	900	Rockwell '83
Silicon	1·5	5·0	1400	Matsush '83
Bip.	1·5	10	660	NTT '83
CMOS	2·0	65	50	I. Micro'ckt. '83
16 × 16 bit				
GaAs EMES	2·0	10·5	952	Fujitsu '83
Si Bip.	2·0	50	1200	AMU '82
*n*MOS	1·5	18	1000	Bell '83
CMOS	2·0	90	125	TRW '82
	1·0	65	250	NEC '82
	1·5	45	100	NEC '84

SDFL approach appears to be the only one meeting the power dissipation, gate delay and fabrication yield required for LSI.

Table 3 projects some of the experimental data reported in static random access memory (RAM). Compared to Si-circuits, it is observed (Bosch 1984) that for 1-k bit RAM the GaAs circuits are faster by a factor of 1·6 while for 4-k bit RAM this factor drops to 1·3. Several GaAs gate arrays in SDFL, BFL and DCFL have been reported. Tables 4 and 5 illustrate some recently reported gate array (Saul 1987) performance figures for Si and GaAs. An important parameter in any gate array is the loaded propagation delay time. Empirical loaded propagation delay time (τ_{pd}) is given by Ikawa *et al* (1984).

$$\tau_{pd} = \tau_{pdL} + (f-1)\,\tau_{pdF} + L \cdot \tau_{pdL} + C \cdot \tau_{pdC}$$

where τ_{pdL} = un-loaded (FO = 1) propagation delay time;

Table 3. Implemented GaAs static random-access memories.

Decoding	Access time (ns)	Chip power (mW)	Reference
1024 × 1	1·3 (min)	1400	Mclevige *et al* (1987)
1024 × 1	1·0	300	Bosch (1984)
1024 × 1	3·8	38	Bosch (1984)
1024 × 4	3	2200	News item (1988)
256 × 4	2·3	550	Mclevige *et al* (1987)
4096 × 1	7	750(75°C)	Microwaves and RF
4096 × 4	4·1	1460	Vlahos and Milutinovic (1988)
4096 × 4	13 ns.	450	Microwaves and RF

Table 4. GaAs gate arrays.

Manufacturer	Process/ logic family	Gate length (μm)	Number of gates	Gate delay (μm)	Power/gate (mW)	Number of gates dissipating (1W)	Functional throughput rate (gate Hz W^{-1})
Fujitsu	GaAs DCFL	1·2	1520	217	2·6**	385	$4{\cdot}4 \times 10^{11}$
Harris†	GaAs DCFL	1·5	170	130	35	29	$5{\cdot}6 \times 10^{10}$
Honeywell	GaAs SDFL	1	432	110	1·5	667	$1{\cdot}5 \times 10^{12}$
NEC	GaAs BFL	1·4	3000*	177	2·3	435	$6{\cdot}1 \times 10^{11}$
OKI	GaAs SBFL	1	1000	185	0·27	3700	$5{\cdot}0 \times 10^{12}$
Tektronix	GaAs DCFL	1	1224	225	0·25	4000	$4{\cdot}4 \times 10^{12}$
Texas Instruments	GaAs HI^2L	3	4000	400	1·0	1000	$6{\cdot}3 \times 10^{11}$
Toshiba	GaAs DCFL	1	1050	350	0·20	5000	$3{\cdot}6 \times 10^{12}$

From Saul (1987)

*Only 2000 can be used due to the prohibitive power consumption; **At 77 K with delays of 158 ps; †Product currently available.

Table 5. Silicon gate arrays.

Manufacturer	Process/ logic family	Minimum feature size (μm)	Number of gates	Gate delay (μm)	Power/gate (mW)	Number of gates dissipating (1W)	Functional throughput rate (gate Hz W^{-1})
Fairchild	Si bipolar	1·5	2840	250	2·0	500	5×10^{11}
NEC	Si bipolar	1·5	2000	700	1·9	520	$1{\cdot}9 \times 10^{11}$
Honeywell	Si bipolar	1·25	5000	600	1·0	1000	$4{\cdot}2 \times 10^{11}$
Siemens	Si bipolar	2·0	9000	600*	2·2	450	$5{\cdot}6 \times 10^{11}$
NTT	Si SST–1 bipolar	1·0**	2500	80	2·6	380	$1{\cdot}2 \times 10^{12}$
Plessey	Si bipolar	3·0	600	400	10	100	$6{\cdot}3 \times 10^{10}$
Plessey	Si bipolar	3·0	2500†	250/ 350	1·2	810	$5{\cdot}9 \times 10^{11}$

From Saul (1987)
*Figure adjusted for compatibility; **emitter 0·5 μm; †semi-custan chip so not strictly compatible.

τ_{pdF} = increase in delay time/FO and F = number of FO;
τ_{pdL} = increase in delay time/interconnection length;
τ_{pdC} = increase in delay time/one cross over load;
L = interconnection length; and
C = number of cross-overs as a load.

So far as gate delay is concerned, the advantage of GaAs is less clear, but it may be noted that an advantage towards GaAs of approximately 1·5 times on throughput rate is realised.

A word generator circuit fabricated by HP (Hewlett–Packard) (Pengelly 1982) contains 400 transistors and 230 diodes contained in a chip size of 1·6 × 1·1 mm. Buffered depletion mode logic is used with typical F/F frequency divider output transition time of 80 ps. The word generator is capable of generating bit streams at data rates of up to 4 Gbit/s. Larger MSI circuits, like an 8-input data multiplexer containing 64 gates have been fabricated and evaluated (Eden and Welch 1982). This circuit would be useful for parallel to serial conversion or a high speed data transmission link. A 1-input to 8-output data demultiplexer using 60 gates have also been reported. Operation of both the multiplexer and demultiplexer have been demonstrated at a clock frequency of 1·1 GHz, with power dissipation of the multiplexer circuits varied from 75 mW to 375 mW. A 128-bit shift register has been designed by Toshiba VLSI Research Center for data buffering memory in high speed computer applications; the register dissipates 3·4 W and functions at 2 Gbit/s (Schneiderman 1988).

The first applications for HEMT logic have been at room temperature and at relatively low level of integration. Using 1 μm long HEMT gates in a ring oscillator of about 25 stages Fujitsu in 1982 reported a switching delay time of about 12·8 ps at 77 K (Solomon 1982). Rockwell has reported (Drummond *et al* 1986) a 12·2 ps/ stage delay with a power–delay product of 13·7 fJ for a ring oscillator with a 0·9 μm

gate transistor at 300 K. A switching time of 5·8 ps per gate at 77 K has been achieved for 0·35 μm gate devices (Kajii *et al* 1988).

The real leverage for the HEMT is in large digital systems such as supercomputers at 77 K. A comparison of HEMT and MESFET in large systems by Fujitsu (figure 4) illustrates the HEMT advantage of high speed at low power (Morkoc and Solomon 1984). Both the chip delay and the system delay (composed of the chip and package delays) at progressively increasing levels of integration were considered. As the integration level is increased, the on-chip wiring capacitance increases and the power per logic gate is reduced (to stay within chip power constraints). The circuit delay increases but the inter-chip delay drops with larger gate count of the individual chips. The result is a minimum system delay at an optimum level of integration. For a 77 K HEMT it is around 100 K gates. The obtained 100 ps minimum system delay would theoretically allow the construction of a computer having an operation-cycle time of a few ns, and thus about 100 MIPS capability.

Cooling improves the performance of GaAs MESFET and Si-*n*MOS. The speed increases when cooled to 77 K by 30 to 40% (Bosch 1984). EFET logic has been demonstrated (Mizutani *et al* 1980) to have a better performance at liquid N_2 temperature. A gate propagation delay of 51 ps which is 40 to 50% lower than the room temperature value has been achieved with a 20-μm gate width ring oscillator.

7. Conclusion

GaAs has matured as semiconductor material to provide a viable IC technology. Compared with the established silicon technology, the advantage of GaAs seems to be only 1·5:1 for room temperature operation (Saul 1987). Silicon-on-sapphire technology might improve the chance of silicon further, but clock frequencies beyond 2 GHz appear to be out of reach for S-O-S circuits with 1 μm-channel length. GaAs circuits will be superior to S-O-S circuits even at clock frequencies

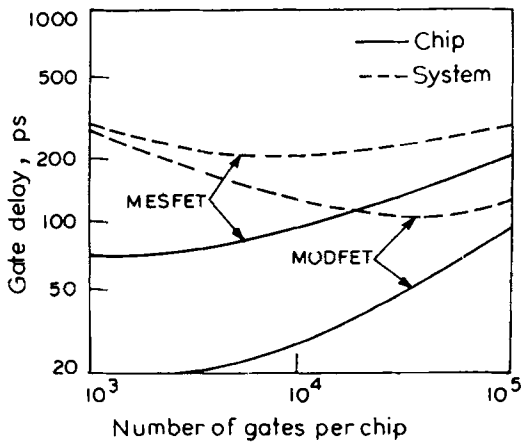

Figure 4. Propagation delay, whether measured on a chip or a system basis, will always be lower for MODFET than for MESFET. The optimum integration level for MODFET (the integration level yielding the lowest system delay) will be somewhere between 10,000 and 100,000 gates per chip. For purposes of comparison, power generation was set at 20 watts per square centimeter.

well below 2 GHz in VLSI, because GaAs offers lower power dissipation at equal speeds. GaAs is more radiation-hard than Si and is tolerant of wider temperature variations.

It has been noted (Bosch 1986) that the speed–power product of the loaded gate increases for the various transistor types in the following: HEMT (300 K), GaAs EFET, Si-CMOS, Si-bipolar, GaAs DFET and Si-NMOS. On the other hand, the maximum gate number (for an assumed chip dissipation of 1-cm^2 area) which can be accommodated can be arranged in descending order as Si-CMOS, Si-bipolar, HEMT (300 K), GaAs EFET, GaAs DFET and Si-NMOS.

From the IC implementations, the following conclusions may be derived from the frequencies and speeds obtained at the same power levels:

(i) The advantage of GaAs, particularly HEMT is obvious for implementing frequency dividers with low level of complexity.

(ii) In 4×4 bit multiplier IC, GaAs leads Si by a factor of 2·5 because of MSI level of complexity. The 8×8 bit multiplier has comparable performance with either GaAs or Si. But in 16×16 bit configurations Si has an edge over GaAs-based circuits. There are evidences on the other hand that GaAs-devices can out-perform silicon devices in the form of HEMT at 77 K.

Until recently, it has not been possible to grow defect-free GaAs wafers. Consequently GaAs devices have been limited in size and have had poor yields. Since the base material cost is ten times that of silicon, the advantage has been very much with silicon. Much of the design expertise and software techniques used in Si may prove to be transferable to GaAs. These together with recent advances in base material and processing may make GaAs more competitive. GaAs on Si offers possibilities for realizing new types of functional devices and IC with GaAs and Si devices (Kaminischi 1987).

If optical fibre systems are to progress to high data rates, GaAs technology and circuit design must be developed to achieve the speed and function complexity required for multiplexing and regeneration of signals. The future prospect of GaAs IC is to integrate high speed logic with optical sources (lasers and LED) and detectors for which Si is not suitable.

Concerning the architecture of Gbit/s circuits and sub-systems, serial processing, pipeline approaches and desirably unity fan-out structures like in systolic arrays should be preferred (Bosch 1984; Gilbert *et al* 1986). These architectural measures might in many cases require the development of new optimum signal-processing algorithms.

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