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GaAs MESFET and related processes

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Abstract. Since inception of GaAs MESFET in 1971, growth and processing technology of GaAs has matured to the extent that the analogue as well as digital IC production is persued at the industrial level. The ever increasing demand for higher frequency of operation, low noise figure and higher gain has led to newer device structures such as HEMT and HJBT based on GaAs and related compounds. Furthermore there exists exciting and proven capabilities in GaAs and related compounds to generate, detect and convert light into electrical signals. This has opened up vast field of opto-electronic devices and their integration with MESFET and other conventional devices.

Basic building block of all these developmental activities still remains the GaAs MESFET, which have also been extensively used as low noise amplifiers, mixers, oscillators and high power amplifiers in descrete form. This paper reviews the design aspects, fabrication technology, d.c. and microwave characterization for both low noise and high power MESFET.

Various technological advancements like via-hole for source grounding, air-bridge technology for low parasitic interconnects and polymide passivation, which have helped in further improvement in terms of higher frequency of operation, low noise and high power output are reviewed.

Finally some representative results on the devices fabricated at CEERI are also presented.

Keywords. GaAs devices; GaAs technology; MESFET.

1. Introduction

The inherently superior electronic properties of GaAs material coupled with recent advances in material and process technologies have opened up a vast field of GaAs-based discrete devices for low noise and high power microwave applications, high speed digital and analogue integrated circuits (IC) and integrated optoelectronic circuits (IOEC). In particular, the GaAs metal semiconductor field effect transistors (MESFET) have made a major impact on a wide range of microwave components by virtue of their very low noise figures and high associated gains. Whereas low-noise FET are already invading the 30 GHz range with noise figures as low as 3dB or less, power FET have started replacing costly and bulky parametric amplifiers and low power travelling wave tube (TWT) (Dilorenzo and Khandelwal 1982; Nogami *et al* 1982; Kim *et al* 1987). However, high yield reproducible fabrication methods and improved performance of the device are of prime concern in satisfying the high demand for GaAs MESFET. Such an advancement has been achieved by novel device structures in conjunction with the improved quality of epitaxial material and related processes. For example, shortening the gate length, introducing the gate recess structure, applying N^+ contact layers and use of undoped buffer layers have resulted in the development of much improved low noise, high frequency and high power GaAs MESFET.

In this paper, a brief review of the current status of GaAs MESFET including

design considerations for both low noise and power FET, materials, fabrication technology and characterization techniques are described.

2. Current status

Figures 1, 2 and 3 represent the state-of-the art results in low noise and power FET respectively. It is apparent from figure 1 that the submicron gate length GaAs MESFET with appropriately scaled unit gate width have superior noise figures at microwave frequencies through the *K*-band. However, the low noise scene has considerably changed since the emergence of high electron mobility transistor (HEMT) devices. Around 2dB noise figures have been measured at 40 GHz (Berenz 1985) and the high frequency operation have been pushed to 60 GHz (figure 1). The state-of-art power FET are capable of giving 1 Watt of power output at 28 GHz. Figure 2 shows maximum power output as a function of frequency (W/mm). The output power decreases as the frequency increases, the best reported value is 0·3 W/mm at 94 GHz. Figure 3 shows the maximum power output from a single

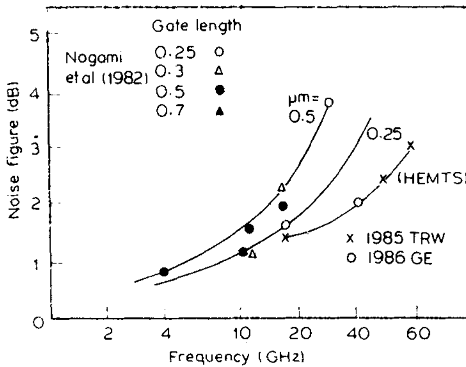

Figure 1. Current status of low noise GaAs FET and HEMT.

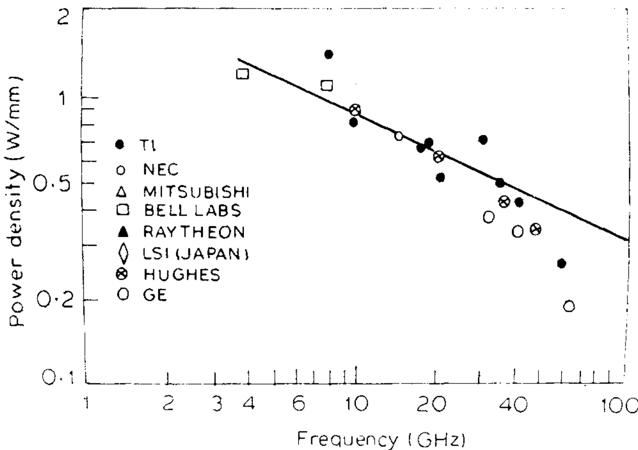

Figure 2. Power density of GaAs MESFET at various operating frequencies.

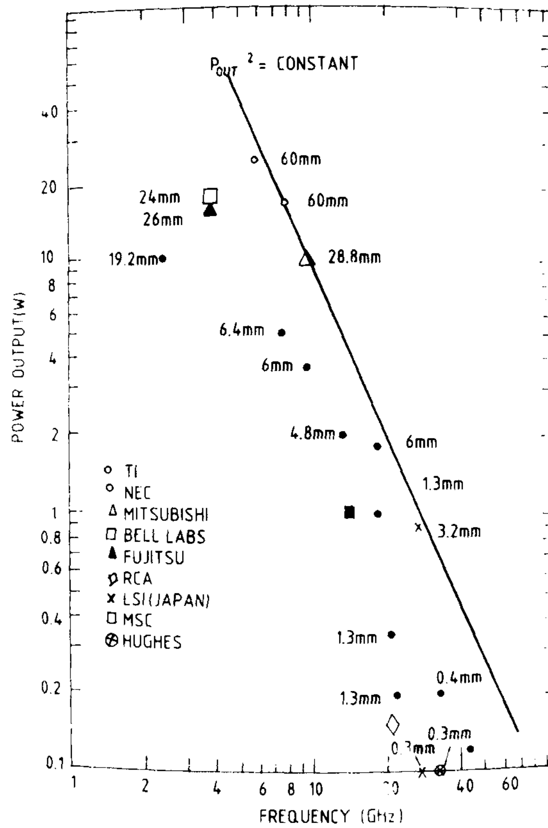

Figure 3. Power output from a single FET at various frequencies.

device. These results have been possible due to a number of improvements in material and device technology and geometries.

3. Design considerations

3.1 *Low-noise FET*

For low noise design, it is important to consider the major parasitic elements associated with the FET for a particular device structure and optimise them. This is crucial because material and layout parameters are directly related to the low noise behaviour of this device. Specifically, the quality of the material at the substrate/active layer interface, the gate length, the gate metal loss and source resistance, all affect the noise performance of the FET. Figure 4 shows the major parasitic elements associated with the recessed structure FET. The noise figure for such a device structure is given as (Fukui 1979; DiLorenzo and Khandelwal 1982)

$$F_0 = 1 + kfL^{5/6}\left(\frac{N}{a}\right)^{\frac{1}{6}}\left[\frac{3\cdot3\,W^2\rho}{hL} + 0\cdot6\,W^2\sqrt{\frac{\rho f}{hL}} + \frac{1\cdot8}{N} \times\left(\frac{L_{SG1}}{a_1} + \frac{L_{SG2}}{a}\right) + \sqrt{\frac{0\cdot18\,R_c}{Na_2}}\right]^{\frac{1}{2}} \tag{1}$$

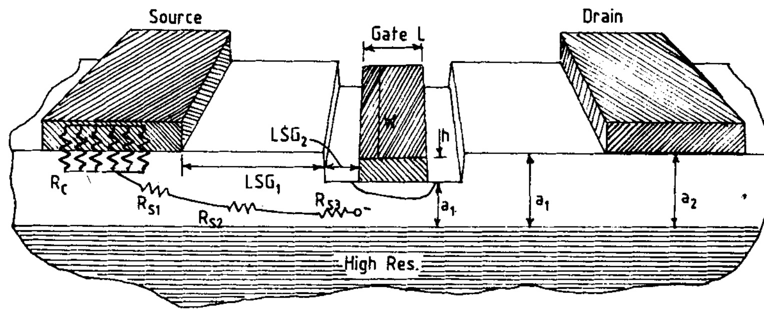

Figure 4. Schematic diagram of FET.

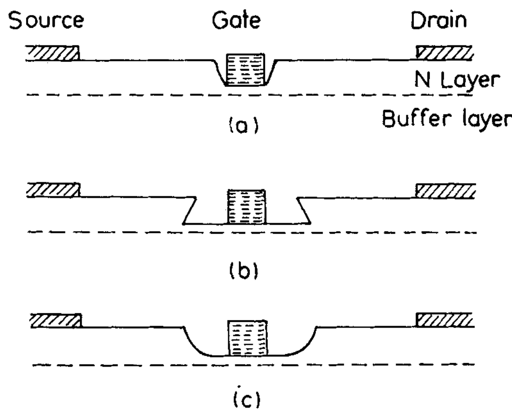

Figure 5. Different types of FET-recessed channel structures.

Here, N is the carrier density in $10^{16}\,\mathrm{cm}^{-3}$, W the gate width in mm, h the gate metallization thickness (in microns), and ρ the gate metal resistivity in 10^{-6} ohm cm.

In (1) the terms I and II represent the noise contribution from the gate metal loss and depend on gate length, unit gate width and conductivity and thickness of the metal used. The most important factor influencing the noise behaviour of the FET is the source series resistance which is represented by the term III. Particularly for conventional flat-type FET structures, the source resistance is found to be nearly double the expected value due to the surface depletion layer (DiLorenzo and Khandelwal 1982). In fact, this causes the poor noise behaviour of such device structures. Gate recessing combined with N^+ contact layer considerably reduces source resistance. The specific contact resistivity should be 10^{-5} ohm cm^2 or less in order to have negligible influence on noise behaviour.

Various recess structure as shown in figure 5 have also been tried to optimise source resistance (Furutsuka *et al* 1978). The first two structures suffer from the large gate-fringing capacitance and thin active layer which make it difficult to reduce the source resistance effectively. In the channel structure shown in figure 5c, there is a smooth change of the active layer and the source resistance is minimised without increasing the gate-fringing capacitance. This structure is considered the optimum recess structure for low noise applications.

3.2 *Power FET's*

The maximum a.c. output power P_{ac} of a MESFET operating in class A is given by

$$P_{a.c.} = 1/8 I_{DSS}(B_{VDS} - V_{DSS}), \quad (2)$$

where I_{DSS} is the full channel current, V_{DSS} the saturation voltage for the drain current and B_{VDS} the avalanche breakdown voltage between the drain and source.

To optimize the MESFET for higher power output, one has to maximize both I_{DSS} and B_{VDS}. The simplest and most widely used method to increase I_{DSS} is to increase the gate width, which is achieved by connecting several gates in parallel. However, an increase in gate width reduces the input impedance and problems of matching with a 50-ohm microstrip have to be tackled.

A high source–drain breakdown is important not only for high power output but also for the stable operation of the amplifier and preventing catastrophic device burn-out. One way to improve B_{VDS} is to include an N^+ contact layer in the source and drain regions either by epitaxial growth or by selective ion implantation. This helps in reducing the electric field near the source and drain, leading to an increased B_{VDS} (Fukuta *et al* 1976). A similar effect has also been observed by forming a smoothly recessed deep channel structure which helps in reducing the field at the drain contact resulting in increase of breakdown voltage (Hasegawa *et al* 1978). One simple way to achieve the same effect is to place the gate electrode near the source together with gate recessing which helps in suppressing the localized electric fields (Moncrief 1980).

Besides maximizing B_{VDS} and I_{DSS}, thermal design is most important in improving the ultimate performance of the power FET. It is well-known that the transistor transconductance g_m is an inverse function of absolute channel temperature. The most important of the thermal effects are the thermally activated failure mechanisms from the reliability point of view (DiLorenzo and Khandelwal 1982).

The parameters associated with thermal design are gate finger width, gate to gate spacing, substrate thickness, heat sinks and mounting procedure. One of the most popular method to optimize the thermal behaviour is through the use of the plated integral heat sinks (Asaro *et al* 1978). In this procedure the source inductance could also be reduced by allowing direct source grounding to the heat sink by a plated-through hole. Another approach involves a flip chip bonding to the package heat sink (Mitsui *et al* 1979).

Besides the above design considerations for a power FET, the standard design equations from low-noise FET for current, cut off frequency f_t, unilateral gain U and stability factor K can be used for high frequency designs also.

Recent advances in GaAs power FET applications have reached amplifier operations up to 60 GHz. As operational frequency increases, the required gate length decreases. At these gate lengths active layer thicknesses also need to be reduced to overcome short channel effects. Consequently a highly doped channel layer is generally used to allow for high current modulation for power generation. The resulting device has low breakdown voltage and tends to operate at low drain bias voltage. Therefore output power per unit gate width decreases as operating frequency increases.

4. Technology

Defect-free GaAs material with uniform and desired doping levels and thickness and sharp interfaces is essential for GaAs MESFET development. Normally $N^+/N/N^-/SI$ GaAs is used for both low noise and power FET fabrication. The N^- undoped buffer layer is just an extension of the *SI* GaAs substrate, which is used to prevent adverse effects caused by Cr-diffusion in the active layer during growth and also to preserve the sharpness of the carrier profile. The buffer layer also helps in preserving the high mobility right up to the interface. Detailed specifications of the various layers and their thickness ranges required are presented in table 1.

Normally all the three $N^+/N/N^-$ layers are grown *in situ* using either VPE, MOCVD or MBE techniques. Although all the three techniques are reported to provide the desired uniformity of doping with accurate thickness control suitable for FET development, only the vapour phase epitaxial process is commonly in use. The MBE process provides well-controlled film thicknesses, sharp doping profiles, good compositions and exceedingly smooth surfaces but it is a slow process and its high cost restricts this technique for special applications. Direct ion implantation in qualified SI substrates followed by passivation and annealing is also finding greater use with competitive performances.

These layers are normally assessed for their suitability in low noise and power FET fabrication. Conventionally, test structures are used to evaluate the carrier density profile using the C–V method, isolated pads for buffer layer resistivity with and without illumination and Van der Pauw structures for mobility evaluations.

4.1 *Fabrication of low-noise FET*

The process flow charts for the fabrication of low noise recessed gate, self-aligned flat type and power FET are illustrated in figure 6. After mesa etching, source and drain contacts are formed by evaporating AuGe/Ni layers. Alloying of ohmic contacts is usually performed at 460°C for a min in H_2 or N_2 ambient. Recessing of the channel region is done either by wet chemical or dry etching. Electron-beam lithography followed by Schottky metal (Al or Ti/Pt/Au) evaporation and lift-off is used for submicron gate fabrication. Si_3N_4/Silox/polyimide passivation and overlay metallization of Ti/Pt/Au is used to improve the reliability and facilitate the bonding of these devices.

In self-aligned flat-type FET fabrication, the tedius gate alignment between source and drain is done automatically. For this, the hangover of the photoresist on top of the Schottky metal or mushroom structure formed by electroplated gold as Schottky metal contact, have been used for the formation of source and drain contact. High temperature refractory Schottky metals have also been used for fabricating self-aligned ion-implanted FET.

Table 1.

Parameters	N^+ contact layer	N active layer	N^- buffer layer	SI substrate
Carrier concentration Resistivity	$10^{18}\,cm^{-3}$	0·5 to $2\times10^{17}\,cm^{-3}$	$10^{14}\,cm^{-3}$	$<1\times10^{7}$ ohm cm
Thickness (microns)	0·1 to 4	0·2 to 0·5	2·5 to 0·5	350
Dopant	S or Si	S	None	Cr/O/undoped

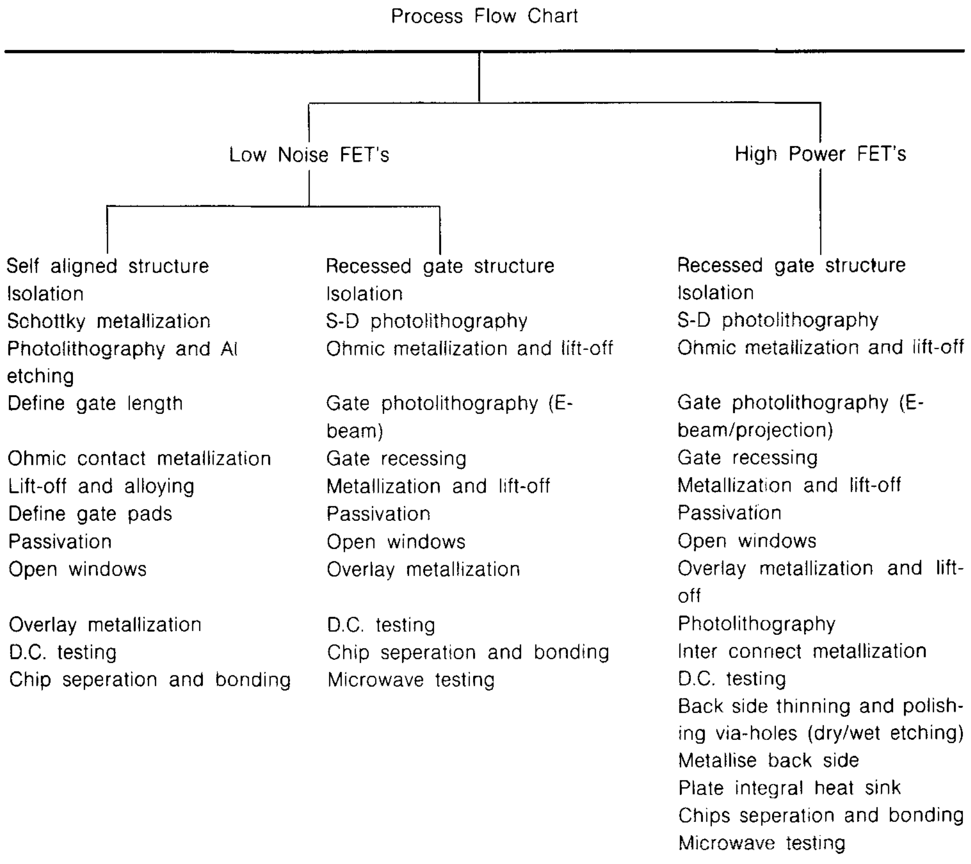

Figure 6. Process flow chart for various structures.

4.2 *Fabrication of power FET*

It is clear from the flow chart (figure 6) that the fabrication steps for high power FET require some additional steps to complete the processing. Power FET structures can be broadly classified into two groups depending upon how the unit cells are connected. The fabrication sequence up to the Schottky metal follow the same routine as that of low-noise FET (figure 6). In a power FET structure, crossover of interconnect metal is done using a dielectric layer as intermetal isolation or the air-bridge technology (§ 6·1). Normally, plasma-enhanced Si_3N_4/SiO_2 or an organic dielectric such as polyimide could be used as the dielectric layer for intermetal isolation. Ti/Pt/Au(0·2/0·2/1·0 μm) layers are used for interconnecting the respective gate source and drain bus. The other type of power FET structure uses wire bonding or flip chip configuration and connections via holes.

After the epi-side fabrication is complete, the wafers are thinned from the backside to obtain a final thickness of 50 to 100 μm. This is followed by Ti/Au metallisation, which is further plated to form a 1 micron thick gold layer. In some cases, source and substrate is connected through a via hole, formed as a part of thinning and gold plating. However, significant improvement due to this process are observable only beyond 7 GHz.

5. DC and microwave characterisation of MESFET

Saturation current and transconductance provide useful information on carrier density while pinch-off voltage provides qualitative information regarding active layer thickness and its interface quality. Initially on a few samples, gate source breakdown voltage and forward diode characteristics are also observed to check the Schottky diode and related parameters.

Besides this, d.c. saturated and unsaturated transfer characteristics, contact resistance etc. yield useful information on parasitic resistances. A detailed analysis of these are presented in Fukui (1979).

For stable operation of power FET, the breakdown voltage between source and drain is also of great importance; for C band operation this should be typically around 20 volts.

The following measurements are needed for the microwave characterization of FET (Camisa *et al* 1984).

i) S parameter measurements,
ii) noise figure measurements,
iii) maximum available gain measurements and
iv) power saturation measurements.

These measurements could be easily accomplished with a conventional set-up using network analysers.

6. Recent technological developments

In this section, state-of-the-art processes presently in use abroad to further improve the device performance are described.

6.1 *Air bridge and via hole technology*

In power FET and complex GaAs digital as well as analogue IC, parasitics associated with the interconnection over the active channels of the FET become substantial and limit the high frequency gain advantage of the device. Air bridge and via-holes provide low parasitic interconnect capacitance and low inductance.

Typical fabrication steps for making plated air bridges and via-holes are shown in figure 7. It is clear from the figure that air bridge technology requires two levels of lithography followed by electroplating or sputtering and lift-off. For via-hole fabrication, a conical etch profile is essential to connect the front side layers. Although controlled chemical etching could be used for this purpose, ion milling or laser techniques are preferred (Camisa *et al* 1984; Daga *et al* 1986).

6.2 *Polyimide processes*

Polyimide, an organic dielectric, having very good dielectric properties is finding tremendous use in GaAs technology as a passivation layer for scratch protection and also as a dielectric layer for intermetal isolation in power FET and IC. Low-temperature processing and easy patterning are some of the advantages of this process (Singh *et al* 1987).

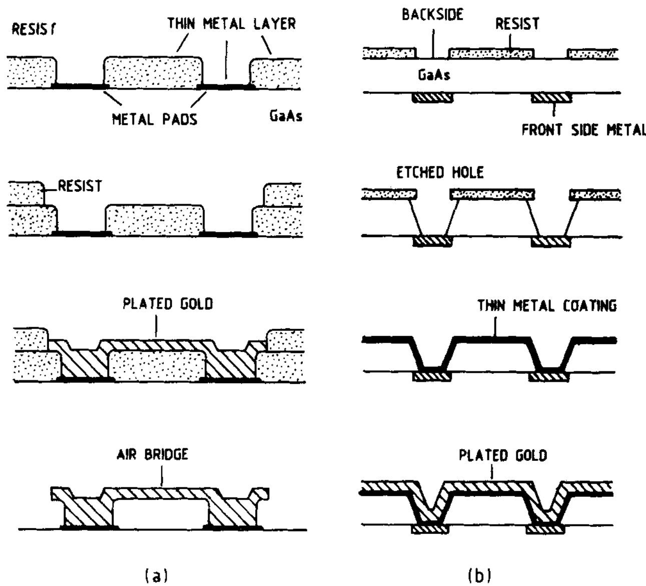

Figure 7. Fabrication steps for (**a**) air-bridge and (**b**) via-holes.

Due to high band gap of GaAs as compared to silicon, GaAs devices are preferred for high-temperature operating conditions. But degradation in the contact metal system is a major drawback. Presently greater emphasis is laid on developing high temperature contacts for GaAs material. Although refractory metals and their silicides show stable Schottky contact up to 800° C on GaAs, various metal systems are being investigated for ohmic contacts.

Due to the ever-increasing quest for high frequency operation for GaAs FET, lithographic processes combined with lift-off are continuously being investigated. Electron beam lithography combined with the multilevel resist system resulting in high aspect ratios facilitates easy lift-off. The modification of the top photoresist layer by some chemical treatment to obtain the desired resist profile for easy lift-off is also being attempted.

7. Work at CEERI

For the last 8 years a small group of researchers are pursuing investigations on GaAs MESFET which has now been extended to digital as well as Monolithic Microwave Integrated Circuits (MMIC). At CEERI, both recessed gate and self-aligned low noise FET having gate lengths 2 μm and 1·25 μm, respectively, on epitaxial and ion implanted material have already been dèveloped. Figure 8 shows the cross-sectional view of the process steps followed for their development. The DC characteristics of various types of FET developed are illustrated in figures 9 and 10. Packaged devices have been tested for their microwave performance and showed a gain of 7·5 dB with noise figures of around 3 dB (Daga *et al* 1985).

Most of the state-of-the-art processes such as the air bridge and via-hole technology (Singh *et al* 1988), rapid thermal annealing for implanted layer activation, and polyimide processing for intermetal isolation, have been

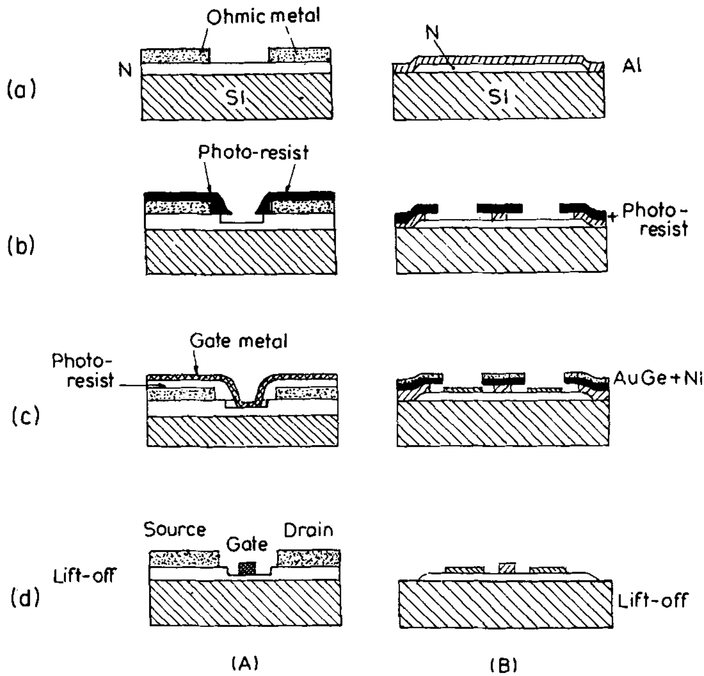

Figure 8. Process steps of the (A) recessed gate structure and (B) self-aligned GaAs MESFET.

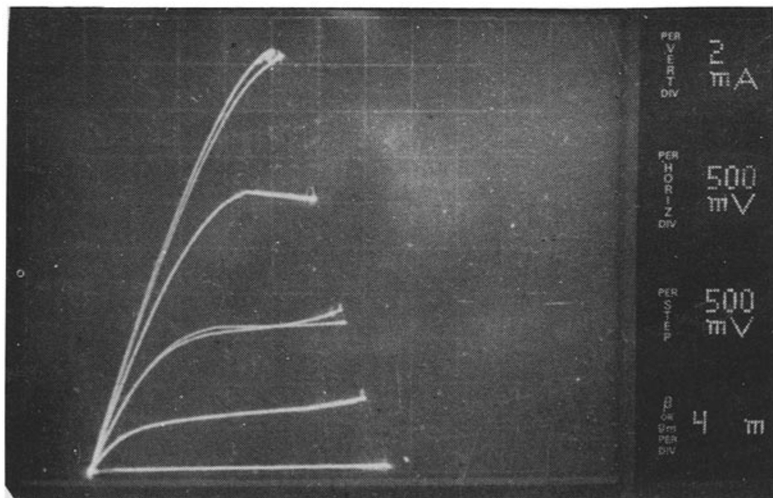

Figure 9. DC characteristics of the devices fabricated at CEERI, recessed gate structure (Ids $\simeq 20$ mA; $gm \geqslant 12$ m mho; $L = 2\ \mu$m).

standardized and presently are being incorporated in power FET, and IC development programmes.

The process followed for the development of air bridge and via-hole technology is illustrated in figure 7. For optimising the process and acquiring design

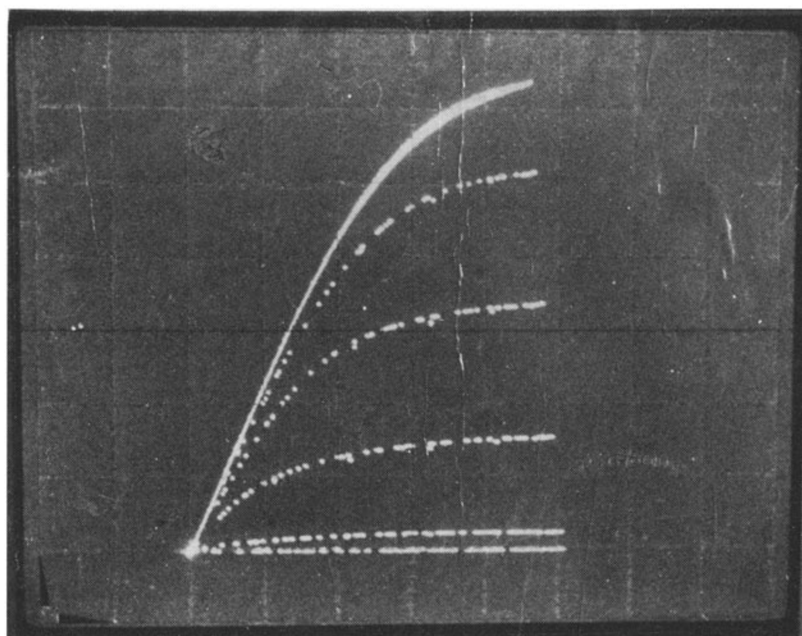

Figure 10. Self-aligned (Epi). $x-0{\cdot}5$ V/step, $y-5$ mA/step, $VG-0{\cdot}5$ V/step, $Ids \geqslant 35$ mA, $gm \geqslant 20$ m mho and $L = 1{\cdot}25$ to $1{\cdot}5\ \mu$m.

Table 2. Optimum 1/*w* ratio for different widths of air bridges.

Width (microns)	Optimum 1/*w*
15	11
30	5
17	2·5
87	2·0
120	1·5

data base at CEERI, bridges of different dimensions from $15 \times 70\ \mu m^2$ to $80 \times 280\ \mu m^2$ were fabricated. The optimum l/w ratio has been found to decrease with increase in the widths of air bridges (table 2). This implies that air bridges of smaller widths should be used to connect larger distances before a post is required (Singh *et al* 1988). Figure 11 shows the photomicrograph of a typical air-bridge fabricated at CEERI.

Figure 12 shows the micrograph of vias of different dimensions etched simultaneously on a single chip using the wet-etching technique. It has been observed that apart from etch rate, etching behaviour strongly depends upon the temperature of the etchant. In addition, magnetic stirring and angular rotation of the substrate during etching has helped us in fabricating via-holes of the order of $15 \times 15 \mu m^2$. Incidentally, the damage introduced to the chip during the thinning process has been found to severely restrict the etching.

In the polyimide process (Singh *et al* 1987), optimisation for obtaining excellent

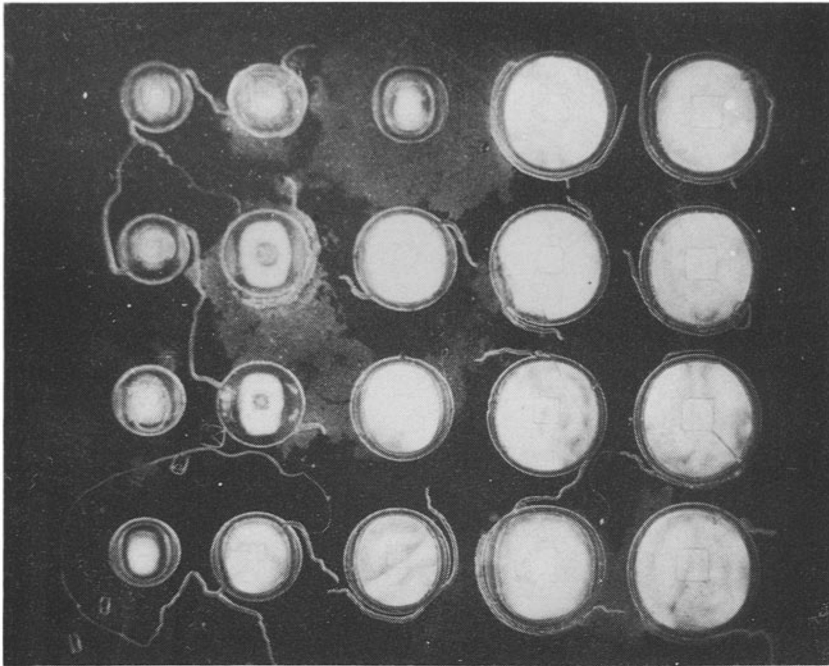

Figure 11. Photomicrograph showing via holes of different dimensions on a single chip.

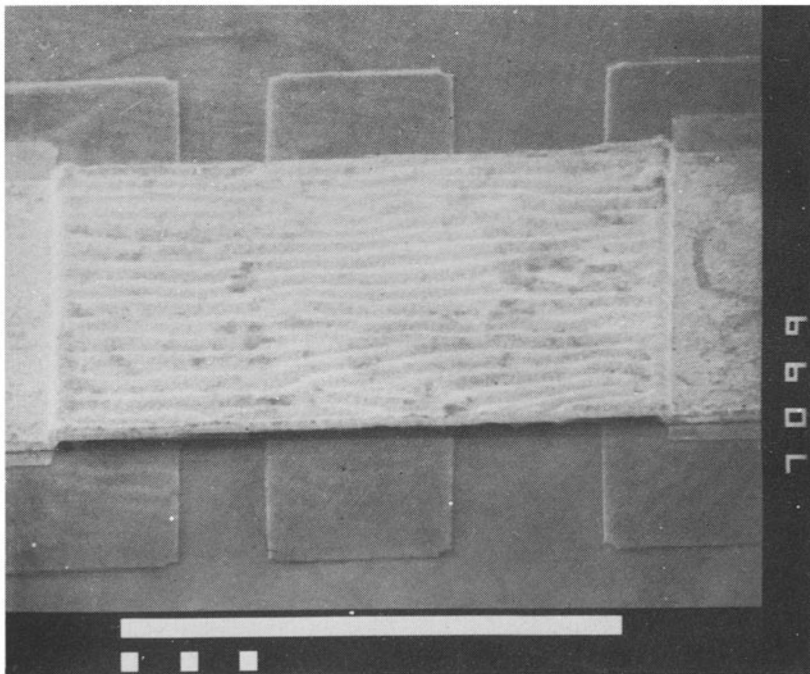

Figure 12. Typical SEM photograph of an air-bridge.

insulating properties with breakdown strengths of 2 MV/cm, degrees of planarization of about 58%, fine line patterning ability with sloped vias of 45° to 60° have been carried out. Figure 13 shows taper angle of sloped vias obtained under different imidisation conditions. Statistical distribution of breakdown field strengths of polyimide layers having different thicknesses is illustrated in figure 14. Various temperature cycles for rapid thermal annealing for the activation of implanted impurities have been tried. Activation of about 70 to 80% with good surface morphology and mobility has been achieved.

Our present emphasis at CEERI has been to establish GaAs low noise, power FET and IC technology incorporating the above mentioned state-of-the-art unit processes for microwave applications and to provide fabrication support to various microwave systems groups within the country for their design verification and applications.

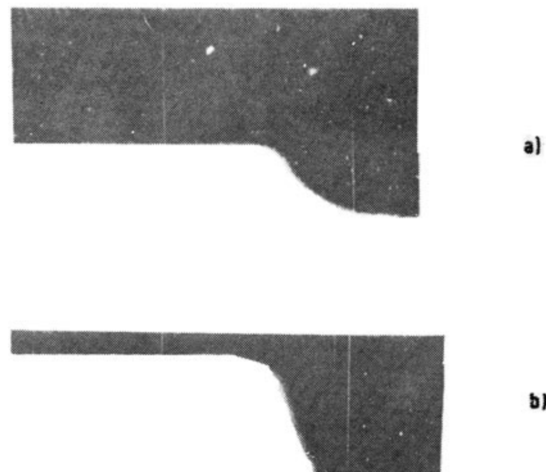

Figure 13. Dependence of taper angle of sloped-edged vias with polyimide film preparation conditions. Imidisation 80%; dilution, (**a**) 1:1, 45°, (**b**) 1:2, 60°.

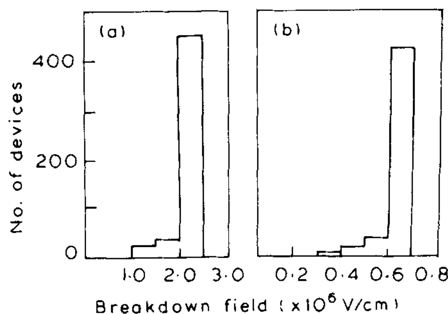

Figure 14. Statistical distribution of dielectric breakdown field strength of polyimides. (**a**) Thickness, 1 μm and (**b**) 0·4 μm.

8. Conclusion

In this paper we have reviewed the current status and technology of GaAs MESFET for low noise and high power microwave applications. The status of GaAs MESFET technology and several state-of-the-art unit processes being developed at CEERI are also included. It can be seen that over the past several years, GaAs MESFET technology has matured to the extent that various fabrication houses abroad are offering foundry services to user agencies. However, R and D efforts are still continuing to further reduce the gate length to 0·1 μm or less for higher frequency of operation and to achieve noise figures of a few tenths of a decibel and power outputs of more than a Watt/mm. Although some isolated efforts in this area are continuing in some R and D institutions within the country, the time is considered ripe to concentrate efforts on bridging the gap in this fast emerging area of technology.

Acknowledgements

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