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Transistors made in laser recrystallized polysilicon on insulator films

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Abstract. LPCVD polycrystalline silicon films were deposited on thermally oxidized silicon as well as on LPCVD silicon nitride deposited on silicon. A CW argon ion laser was used to recrystallize the polysilicon film into large grains (grain size from 5 μm to 40 μm). Boron was then implanted and standard N-channel silicon gate process and N-channel metal gate process were carried out to realise MOSFETs on this material. Channel mobilities upto 450 cm^2/V-sec for electrons have been measured. This thin film MOSFET has a four-terminal structure with a top and a bottom gate and the influence of one gate on the drain current due to the other gate has been investigated. Comparison of the I_D–V_D curves of the devices with physical models was found in good agreement.

Keywords. Recrystallisation; semiconductor; silicon; laser; MOSFET; silicon-gate process.

1. Introduction

Polycrystalline silicon formed by low pressure chemical vapour deposition (LPCVD) is commonly used in integrated circuits for interconnections, gate electrodes and resistors. However, the relatively small grain size (of the order of 500 Å) tend to limit its application since the grain boundaries usually affect the transport properties. The earliest MOSFETs fabricated on thin films of polysilicon have shown poor mobilities and transconductances (Kamins 1972). It has now been well demonstrated that the grain size of polysilicon deposited on thermally-oxidized silicon can be increased dramatically by annealing the material with either a scanning CW laser beam (Gat *et al* 1978; Kamins *et al* 1980) or a heated graphite strip (Tsaur *et al* 1981). The grain size can be as large as 100 μm by 100 μm extending through the thickness of the film. This has generated a considerable amount of work (Lam *et al* 1982; Colinge *et al* 1983) devoted to the fabrication of device-worthy silicon-on-insulator (SOI) films as an alternative to the classical silicon-on-sapphire (SOS). A variety of applications such as large flat panel displays and 3-D integrated circuits offer a significant promise for the future.

We report here our results of MOSFETs made by laser recrystallization.

2. Experimental

The samples were made on 2 inch diameter P type $\langle 100 \rangle$ silicon wafers. A 1 μm thick oxide was grown in steam ambient and a 500 nm thick film of polysilicon was deposited by low pressure chemical vapour deposition (LPCVD) of silane. A capping layer of silicon nitride was then deposited by LPCVD of dichlorosilane and ammonia. The thickness of the nitride was 60 nm which gives the optimum antireflection effect for the two laser

wavelengths (488 nm and 514·5 nm) used in the recrystallization. The wafers were then recrystallized using a cw argon ion laser operating in the multiline mode. The substrate was heated to 350°C on a vacuum held chuck and the laser beam was scanned in a serpentine fashion using an X-Y mirror galvanometer deflection system. A plano convex lens of focal length 250 mm was used to focus the beam on to the substrate to give a spot size of about 60 to 70 μm. The scan speed was 10 cm/sec with spacing between successive scan lines of about 20 μm. The laser power used was between 11 W and 13 W.

As a result of the recrystallisation, long crystallites (upto 40 μm in length, 5 to 10 μm in width) were formed in a chevron shape. The capping nitride was then stripped in hot phosphoric acid. Boron was implanted into the large grain silicon at 80 keV to a dose of 1×10^{12} ions/cm^2. (This dose was calculated to make the recrystallised polysilicon p-type with an average concentration of $1\text{-}2 \times 10^{16}$ atoms/cm^2). Standard N-MOS silicon gate process was carried out from this stage. A 100 nm silicon nitride was deposited, active areas of transistors defined by photolithography and nitride etched in a CF4 plasma. Local oxidation was then carried out to convert the unwanted polysilicon into oxide. The nitride was then stripped, a gate oxide of 100 nm was grown at 1050°C in oxygen, 0·5 μm polysilicon was deposited and patterned into gates. The source, drain and gates were then doped by $POCl_3$ at 975°C. After opening contact holes, aluminium was evaporated and patterned. The devices were then sintered at 500°C in N_2 for 45 min. Figure 1 shows the cross-section of the completed structure. Some wafers were processed for N-MOS meal gate devices.

3. Results and discussion

The MOSFET device characteristics were measured with an automated measurement system controlled by a desktop computer. Figure 2 shows a typical drain current I_D versus drain voltage V_D family of curves as a function of the top gate voltage V_{G1} for a particular bottom gate voltage V_{G2}. Referring back to figure 1, we notice that the 1 μm silicon dioxide on which the recrystallized film is sitting acts as a second gate dielectric with the underlying support of silicon as the gate electrode. This four-terminal structure of the laser recrystallized film is thus unique and consequently, the device has two channels for current to flow from source to drain—a top channel below gate 1 and a bottom channel above gate 2.

The MOSFET, now called MISIMFET (metal-insulator-semiconductor-insulator-metal), has therefore four cases of operation:

(i) When the voltages on both gates are large and negative the silicon below the gates are accumulated and the transistor is in the OFF state.
(ii) The voltage on one gate forms an inversion layer (i.e. a channel) while the other gate is in accumulation.
(iii) The voltage on one gate forms a channel while the other gate forms a depleted region.
(iv) Both the gate voltages are such that a channel is formed below each gate.

The drain current I_D therefore is a function of drain voltage V_D, gate 1 voltage V_{G1} and gate 2 voltage V_{G2}. This dependence can be seen in figure 3 which is the I_D–V_{G1} curve for a small drain voltage (V_D = 100 mV) as a function of the back gate voltage V_{G2}. For

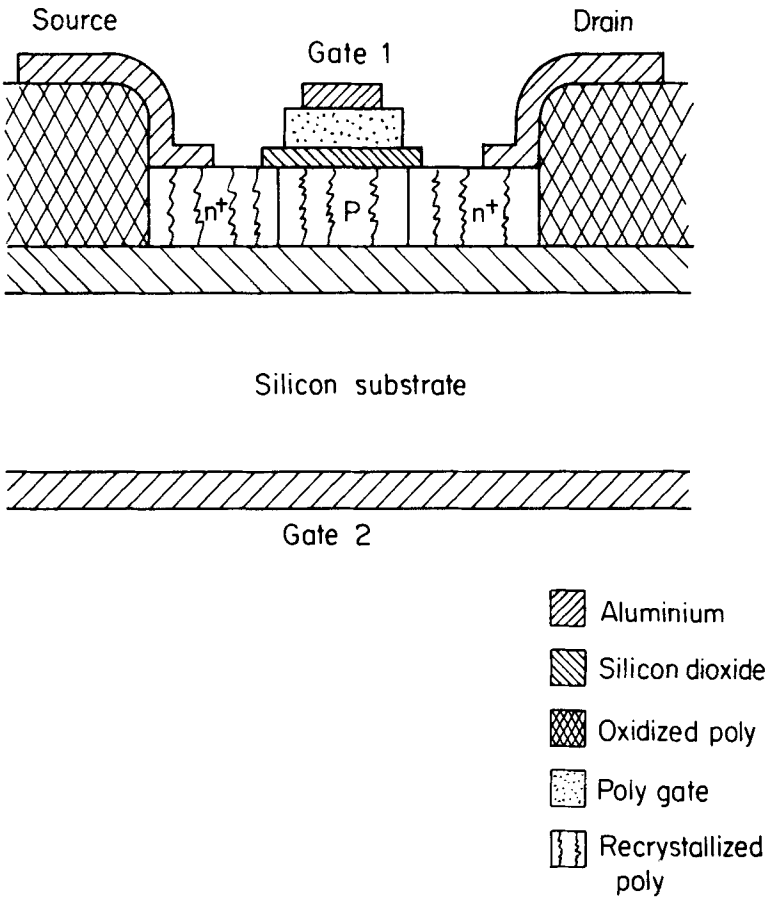

Figure 1. Cross-sectional view of completed MOSFET on laser recrystallized polysilicon.

$V_{G2} < -45$ V and $V_{G1} < -4$ V, we see the drain current is practically zero. This is case 1 above, when both channels are OFF. For $V_{G1} > -4$ V and $V_{G2} < -45$ V, the drain current starts increasing showing that channel 1 has inverted while channel 2 is still off. For $V_{G2} > -45$ V and $V_{G1} < -4$ V, we see that the drain current again increases showing that channel 2 has inverted while channel 1 is off. This is case 2. For $V_{G1} \geqslant -3$ V and $V_{G2} \geqslant -35$ V both channels are conducting and we have case 4. Case 3 falls between these two voltage limits.

The expression for the drain current when channel 2 is accumulated is

$$I_D = \mu \frac{W}{L} C_{01} (V_G - V_{T1}) V_D,$$

where μ is the mobility, W and L are the device width and length, C_{01} is the gate 1 capacitance, V_D is the drain voltage (= 100 mV), V_{T1} is the turn on voltage of channel 1. The slope is

$$\partial I_D / \partial V_G = \mu \frac{W}{L} C_{01} V_D$$

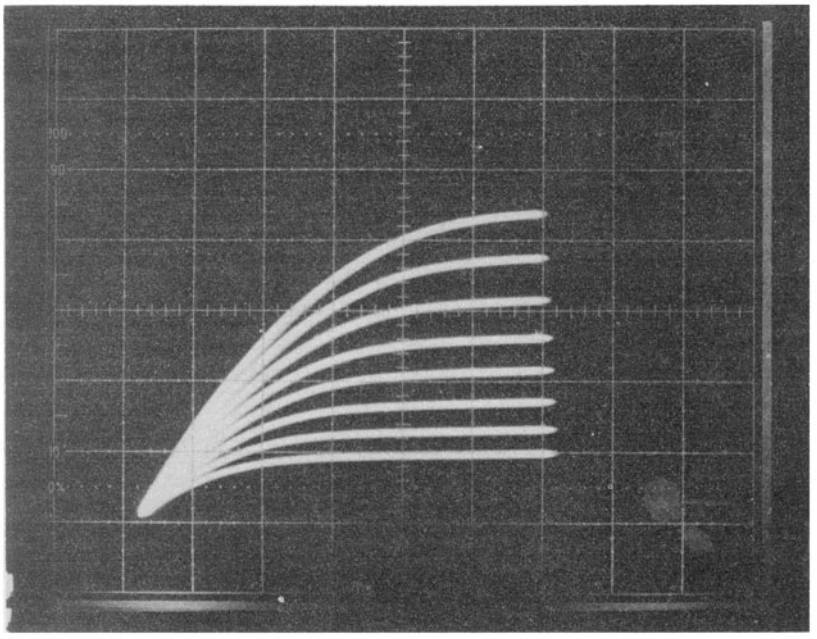

Figure 2. Photograph of the I_D–V_D characteristics of the n-channel Si gate MOSFET as a function of front gate voltage V_{G1} for a fixed back gate voltage V_{G2}.

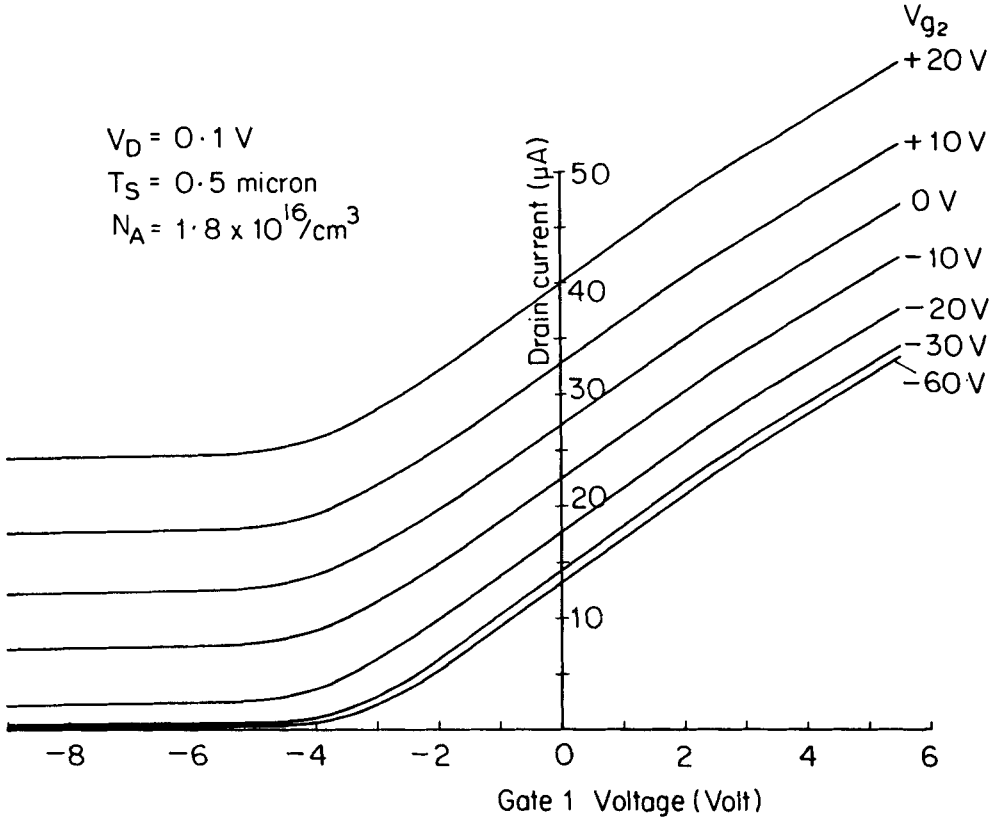

Figure 3. Drain current vs front gate voltage V_{G1} as a function of back gate voltage V_{G2}.

and the intercept is V_{T1}. We have measured mobilities from 250 cm^2/V-sec to 450 cm^2/V-sec with the front channel threshold voltage of $-3{\cdot}2$ to $-3{\cdot}5$ V and back channel threshold voltage of -30 V to -35 V.

There have been two models proposed in literature for explaining the I_D–V_D behaviour of the MISIM structure, one by Lim and Fossum (1984) and the other by Barth *et al* (1983). The second model is exact while the first one makes some approximations. Both models take into consideration the fact that silicon is finite in extent (0·5 μm in our case) and so far a given impurity concentration, the depletion regions from the top and the bottom will meet at some point making the entire film depleted. As a result, there is "communication" between the top and bottom gates, thereby controlling the drain current. We have matched our data with the Barth-Apte-Angell model and this is shown in figure 4 with a good fit.

Since our device has a W of 100 μm and L of 20 μm, there are a couple of grain boundaries in the active region of the transistor perpendicular to the current flow. The mobility and threshold voltages are thus modulated by these grain boundary charges and this gives a small error to our modelling effort. We have taken care of these effects by a voltage-dependant mobility (as can be seen in figure 3, where the slope is not constant).

The parameters which were used to fit the data are the mobilities $\mu n_1 = 295$ cm^2/V-sec of front channel and $\mu n_2 = 310$ cm^2/V-sec of back channel, V_{FB1}, the front channel flat band voltage of $-6{\cdot}1$ V and V_{FB2}, the back channel flat band voltage of -52 V. The front gate oxide is 1000 Å while the back gate oxide is 1 μm.

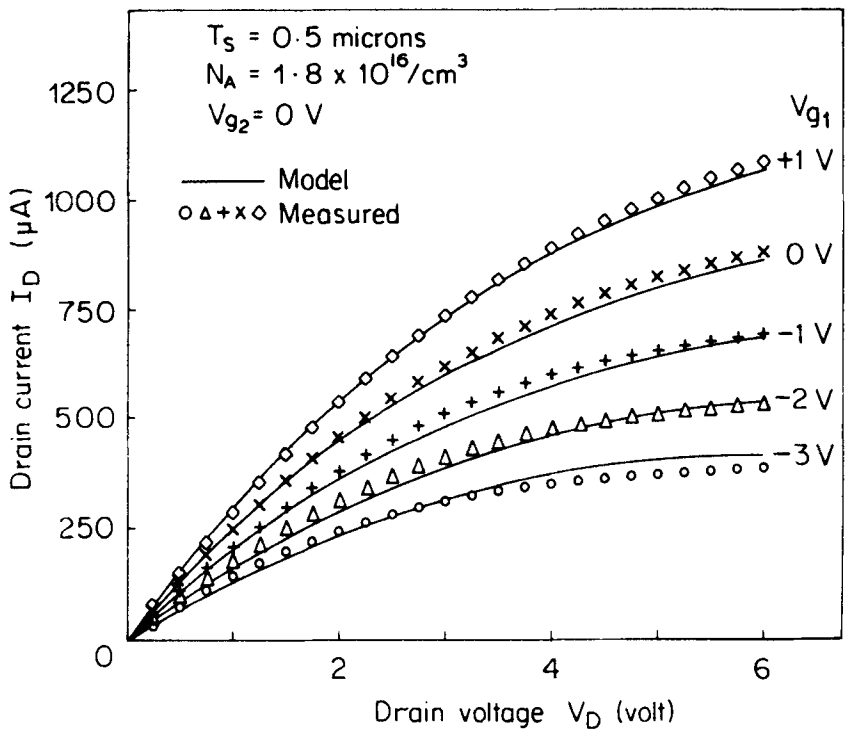

Figure 4. Experimental and calculated I_D–V_D curves for the MISIMFET.

4. Conclusions

We have fabricated N-channel silicon gate and metal gate MOSFETS by recrystallization, using a CW laser beam, LPCVD polysilicon deposited on thermally oxidized silicon. Surface electron mobilities upto 450 cm^2/V-sec have been measured. We have demonstrated the 4-terminal behaviour of our structure and applied a model to explain the I_D–V_D curves as functions of the two gate voltages. Laser beam recrystallized polysilicon films on insulators have a bright future for realising device-worthy silicon-on-insulator films and making 3-D integrated circuits.

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