

Proximity effect of electron beam lithography on single-electron transistors

SHU-FEN HU^{1,*}, KUO-DONG HUANG², YUE-MIN WAN² and
CHIN-LUNG SUNG¹

¹National Nano Device Laboratories, No. 26, Prosperity Road I, Science-based Industrial Park, Hsinchu 30078, Taiwan

²Department of Electronic Engineering, I-Shou University, Kaohsiung 840, Taiwan

*Corresponding author. E-mail: sfhu@mail.ndl.org.tw

Abstract. A simple method, based on the proximity effect of electron beam lithography, alleviated by exposing various shapes in the pattern of incident electron exposures with various intensities, was applied to fabricate silicon point-contact devices. The drain current (I_d) of the device oscillates against gate voltage. The electrical characteristics of the single-electron transistor were observed to be consistent with the expected behavior of electron transport through gated quantum dots, up to 150 K. The dependence of the electrical characteristics on the dot size reveals that the I_d oscillation follows from the Coulomb blockade by poly-Si grains in the poly-Si dot. The method of fabrication of this device is completely compatible with complementary metal-oxide-semiconductor technology, raising the possibility of manufacturing large-scale integrated nanoelectronic systems.

Keywords. Semiconductors; transport; nanostructures.

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1. Introduction

Recent years have seen dramatic developments in nanometer-scale silicon (Si) structures and especially in silicon nanodevices that utilize the quantum or single-electron charging and low power consumption features of a single-electron transistor (SET), which make them promising base elements for microelectronic and nanoelectronic circuits in the future. The main limitation, which tends to hinder progress in this direction, is the requirement of very small structural elements in the devices. For operation at room temperature, the devices should be smaller than 10 nm, below the limit of resolution of modern nano-lithography processes. A silicon (Si)-SET has the widest range of applications among the various SETs, because it can be fabricated by the process used to make large-scale silicon integrated (LSI) circuits. The main problem is to make SETs with the desired electrical characteristics.

Electron beam lithography (EBL) is a technique for creating extremely fine patterns (submicron patterns, 0.1 μm and below) for integrated circuits. Such patterns

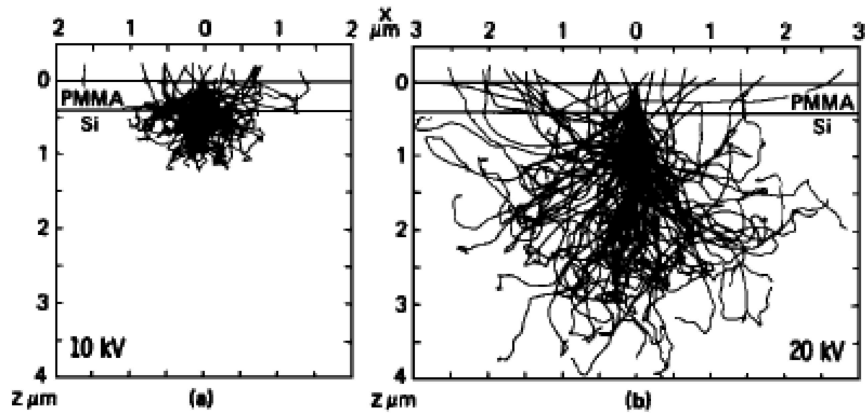


Figure 1. Monte Carlo simulation of electron scattering in resist on a silicon substrate at (a) 10 kV and (b) 20 kV (from Kyser and Viswanathan [1]).

can be made because the spots of electrons are very small, whereas the optical lithography is limited by the wavelength of light which is used for exposure. The wavelength of the electron beam is so small that diffraction no longer determines the lithographic resolution. Accordingly, electron beam lithography is the most commonly used technique in this field, and many researchers have been investigating its application to make nanopatterns.

In electron beam lithography, the well-known proximity effect refers to variation in the width of patterned lines with the density of other shapes nearby. The variation, of course, makes increasing the resolution difficult. The electron proximity effect has been a major obstacle in achieving fine resolution in electron beam lithography. As charged particles, electrons undergo forward and backward scattering when they are incident a resist-coated substrate. Figure 1 presents typical electron trajectories simulated by the Monte Carlo simulation package MOCASEL [1]. The simulation that assumed electrons with energies of 10 keV (left) and 20 keV (right) were incident on a resist-coated photomask substrate (chrome on quartz plate). The scattering of these electrons causes undesirable resist development energy to accumulate around the patterned areas. This accumulated energy from the scattered electron only slightly affects isolated patterns, but significantly more energy accumulates in densely patterned areas. Hence, isolated patterns are somewhat narrower than designed, and lines in densely patterned areas are somewhat wider than designed. The distribution of intensity of exposure has a Gaussian intensity profile, because electrons are forward-scattered and back-scattered. The main ways to compensate for the proximity effects are to adjust the dosage of the electron beam according to the density of the patterns, or to anticipate the changes in dimensions of the features and make compensating adjustments in advance. Nevertheless, this work reports the fabrication of SETs from silicon point-contact, made by exposing different shapes in the pattern to incident electrons with various intensities.

2. Experimental

The point-contact structures are fabricated by choosing an appropriate electron-beam dose and pattern development time. The substrates used in this work were p-type Si substrates, with a thin 25 nm polysilicon layer on top of a 200 nm thick buried SiO₂ layer. The top polysilicon layer was doped by phosphorous at 620°C for 30 min in a low-pressure chemical vapor deposition (LPCVD) system and annealed at 925°C for 20 min in a nitrogen atmosphere. The sheet resistance of the polysilicon layer is around 25–50 Ω/cm^2 at room temperature. The point-contact structures were formed by direct writing electron-beam using a Leica Weprint 200 system with an NEB22A electron-beam resist and a transformer coupling plasma (TCP) silicon dry etcher. The 40 keV acceleration voltage of the Leica Weprint 200 system yielded a fine beam with a diameter of about 20 nm; the beam current density was 4 A/cm². After exposure to the e-beam, the pattern was developed in an NEB, and baked at 115°C for 120 s. Figure 2 schematically depicts the mechanism used in this work for forming point-contact structures [2]. When the resist is exposed to the electron beam at the tip of each electrode (at distance between the tips of the electrodes of 90, 100 and 110 nm), then the resist in the interelectrode region is also partially exposed because the beam has a Gaussian intensity profile (indicated by the dotted lines (middle)). Since the designed gaps of 90, 100, 110 nm are close to actual beam size, both beams overlap in the gap region. Therefore, an overall beam dose whose profile is described by a solid line (bottom) interacts with the resist in this region. Consequently, after developing, the area dosage remains higher than threshold exposure dosage and forms a point-contact structure. Finally, etching is performed in LAM TCP 9400SE, using 5–20 mTorr mixing in an atmosphere of Cl₂, O₂, HBr and SF₆ at 65°C. Figure 3 shows the scanning electron micrograph of the 20 nm \times 20 nm point-contact structure. After the pattern had been transferred, a 5 nm-thick gate oxide was grown at 925°C for 2.5 min in oxygen, further reducing the point-contact dimension. Then, 50 nm-thick n-type poly-Si was deposited by a LPCVD system to form the control gate.

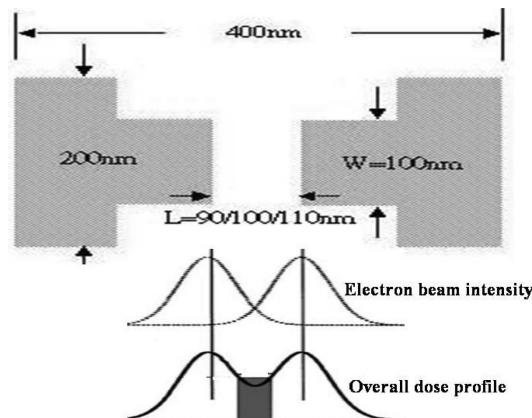


Figure 2. Mechanism of fabrication of a point-contact structure.

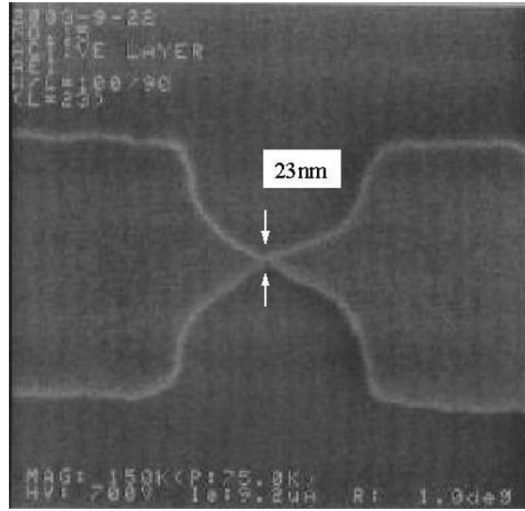


Figure 3. Scanning electron microscopy image of active area structure of point-contact device.

The gate poly-Si was lithographically patterned and etched to cover the Si point-contact structure. After another 200 nm-thick TEOS (tetraethylorthosilicate) oxide layer was deposited and contact patterning performed, an aluminum metal film was deposited and patterned to provide electrical contacts to the device. An HP4156B semiconductor parameter analyzer measured the characteristics of the device at 300 K in air and at low temperatures from 4 K up to 150 K in a liquid He-4 system, with Keithley 4200 semiconductor characterization system.

3. Results and discussion

Figure 4 presents the 20 nm \times 20 nm Si point-contact device. Figure 4a schematically depicts its structure. Figure 4b shows a scanning electron micrograph of the device. The point-contact device was characterized electrically from 4 to 300 K. The source-drain (I_d) current was measured with respect to the source-drain voltage (V_d) and the gate voltage (V_g), and single-electron effects were observed over the entire temperature range. Figure 5 plots the I_d - V_d characteristics of the device measured from 77 to 300 K as the gate voltage (V_g) is fixed at zero. A Coulomb gap of \sim 200 mV is observed as the temperature is increased, because an increase in the tunneling probability is thermally activated.

Figure 6 plots single-electron current oscillations in the I_d - V_g characteristics at 40 K. V_d increases from -10 mV to 10 mV in 1 mV steps. Oscillations with multiple periods are observed, and these may be associated with single-electron charging in a multiple dominant charging island. The increase in the background current with gate voltage, which similar to that of SETs fabricated in crystalline silicon, may be explained by a transistor-like metal-oxide-semiconductor field effect transistor [3,4]. Figure 7 shows the I_d - V_g characteristics of the point-contact

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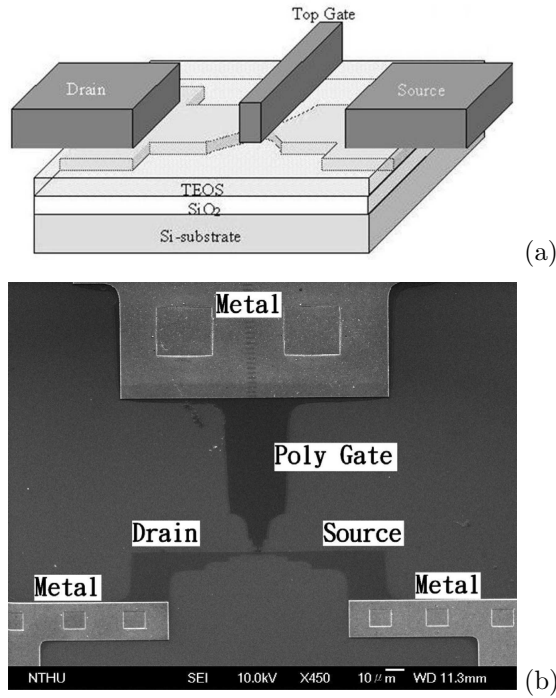


Figure 4. (a) Schematic diagram and (b) a scanning electron microscopy image of the point-contact device.

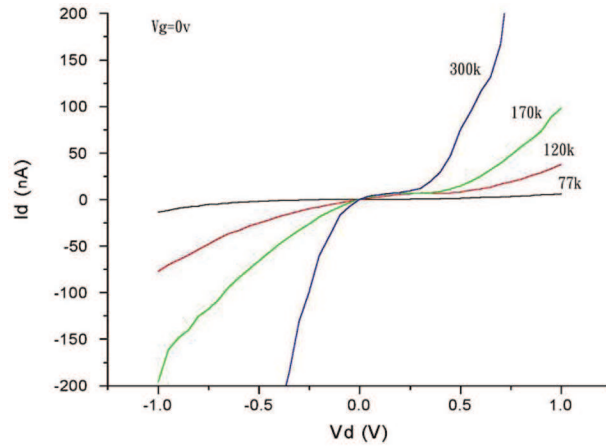


Figure 5. Dependence of the drain current I_d on the drain-source voltage V_d at various temperatures when the gate voltage (V_g) is fixed at zero.

at a lower temperature of 4 K. At this lower temperature, the characteristics are more complicated and additional oscillations in I_d are observed. These effects may be associated with single-electron charging in multiple grains in the

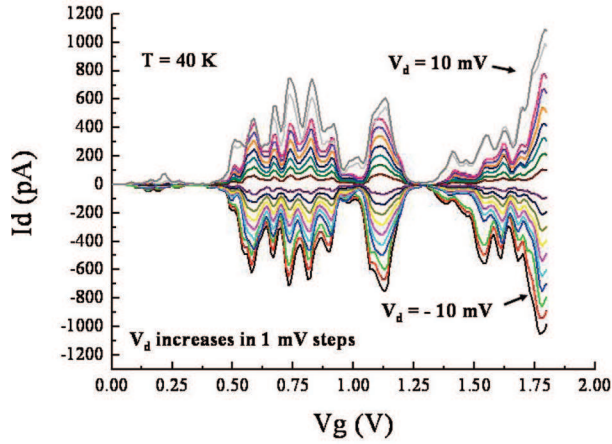


Figure 6. Drain current I_d vs. the control gate voltage of a device at 40 K. V_d increases from -10 mV to 10 mV in 1 mV steps.

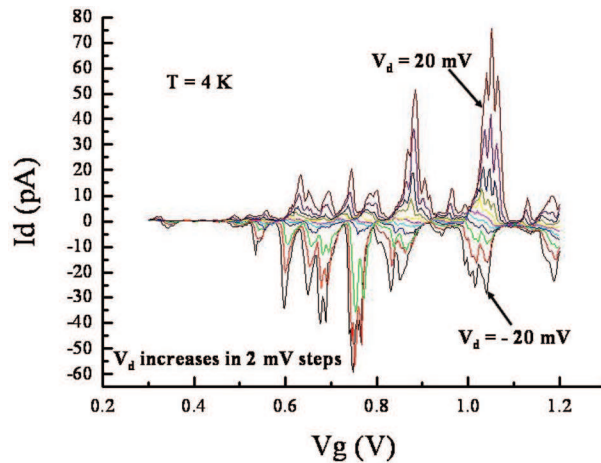


Figure 7. Gate-bias sweep of device at 4 K showing periods of oscillation of current. V_d increases from -20 mV to 20 mV in 2 mV steps.

point-contact. These peaks manifest the fact that the electrostatic energy, when the bulk electrode contains N excess current carriers, equals that when the quantum dots contain $N + 1$ excess carriers [5]. Therefore, the current carrier passes the quantum dots to the other bulk electrode by tunneling through the barriers on each side of the quantum dots. When the energy equality does not hold as the electric potential of the gate electrode, no electron tunnels to and from the quantum dot. Thus, the electron number in the dot takes a fixed value, say zero, when both the electrodes are grounded. The charging effect, which blocks the injection/ejection of a single charge into/from a quantum dot, is called a Coulomb blockade effect. Figure 8 plots the dependence of the current oscillations on temperature. These oscillations persist up to 150 K with a period $\Delta V_g \sim 0.5$ V. The fine structure

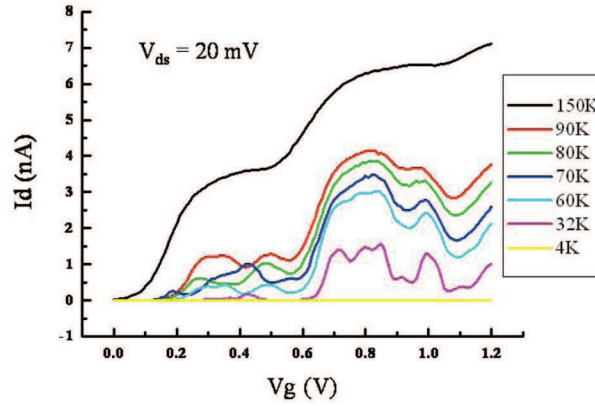


Figure 8. Dependence of current oscillations on temperature. V_g is swept from 0 to 1.2 V when V_d is set to 20 mV.

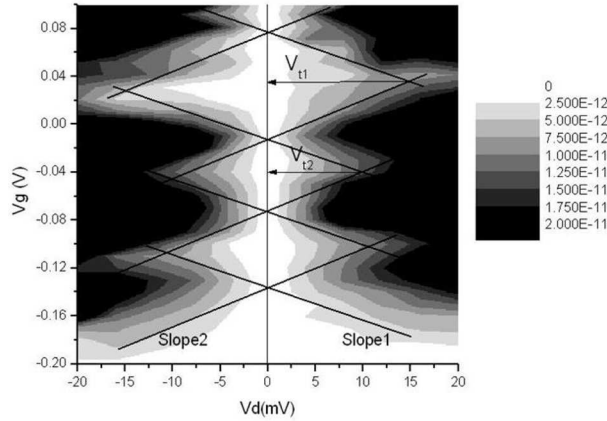


Figure 9. I_d as a function of V_g and V_d , and the curves are the constant I_d contours. The measurement temperature was 40 K; the gate-bias is swept from 0 V to 16 V, and V_d increase from -2 mV to 2 mV.

superimposed on the oscillations disappears at 150 K, corresponding to a gate-island capacitance $C_g = e/\Delta V_g = 3.2$ aF. The current oscillations are superimposed on a generally increasing current background, resulting in a non-zero valley current in the oscillations. This behavior has also been observed in nanowire multiple-tunnel junction single-electron transistors, fabricated in silicon-on-insulator material [3,4], and may be related to a field-induced enhancement of the carrier concentration in the device. The gate may also increase in the tunneling probability.

Figure 9 plots I_d as a function of V_g and V_d ; the curves are the constant I_d contours. The straight lines emphasize the rhombus-like region of the plot. In the rhombus, the nanodots stably contain an integer number of electrons. Thus, the current that flows through the quantum dots is drastically reduced due to Coulomb blockade effect under the conditions defined by V_g and V_d in the rhombus-like

region. These observations are consistent with the predictions of the orthodox theory of the operation of SET. Furthermore, the slopes of the straight lines that define the rhombus-like region provide important information about the nanodots. The experimental values of the control gate capacitance C_g , the drain capacitance C_d , the source capacitance C_s , and the total capacitance C_Σ can be experimentally determined. The two slopes of the edges of the rhombus-like region are 3.3 and 2.67, which equal C_d/C_g and $(C_g + C_s)/C_g$ respectively. The range $|V_d|$ of the drain-source voltage V_d from 0 mV to the tip of the rhombus-like region is 10–15 mV. Accordingly, the total capacitance $C_\Sigma = C_g + C_d + C_s$ [6], calculated from the range of V_d according to $C_\Sigma = e/|V_d|$ is 10–16 aF. Solving for C_g, C_d , and C_s yields $C_g = 1.78$ – 3.2 aF, $C_d = 2.97$ – 2.24 aF, and $C_s = 5.87$ – 10.56 aF. The threshold voltage V_b is obtained as 10–15 mV from the Coulomb diamond graph. Then, C_Σ is derived at about 10–16 aF. The theoretical value of the control gate capacitance C_g can also be approximated. The width of the nanodots defined in figure 3 is 20 nm. Additionally, the thickness D of the gate oxide, which equals the distance between the control gate and the dots, is 5 nm. Therefore, C_g is estimated as $C_g = \varepsilon_r \varepsilon_0 A/D$, where the relative dielectric constant ε_r of silicon dioxide is 3.9, so C_g is 3.5 aF, which is consistent with the previously calculated value of 1.78–3.2 aF. The Coulomb dots should therefore be smaller than 15 nm (width) \times 15 nm (length) \times 20 nm (thickness).

4. Conclusions

Silicon point-contact devices were fabricated on a polysilicon film. The devices were fabricated based on the proximity effect associated with electron beam lithography, alleviated by exposing various shapes in the pattern to electrons with various intensities. The devices consist of top-gated quantum dots between the source and drain electrodes. The electric characteristics of the devices included single-electron charging effects up to 150 K, consistent with the expected electron transport through gated quantum dots. The growth/deposition of materials and the fabrication of the device are compatible with silicon technology, raising the possibility of manufacturing large-scale integrated nanoelectronic systems.

Acknowledgement

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References

- [1] D F Kyser and N S Viswanathan, *J. Vac. Sci. Technol.* **12(6)**, 1305 (1975)

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- [2] K Liu, Ph Avouris, J Bucchignano, R Martel, S Sun and J Michl, *Appl. Phys. Lett.* **80**, 865 (2002)
- [3] H O Muller, D A Williams, H Mizuta and Z A K Durrani, *Mater. Sci. Eng.* **B74**, 36 (2000)
- [4] R A Smith and H Ahmed, *J. Appl. Phys.* **81**, 2699 (1997)
- [5] *Single charge tunneling* edited by H Grabert and M H Devoret (Plenum, New York, 1992)
- [6] *Transport in nanostructures* edited by David K Ferry and Stephen M Goodniik (Cambridge University Press, Cambridge, 1997)
- [7] Yasuo Takahashi, Akira Fujiwara, Yukinori Ono and Katsumi Murase, *Proc. 30th IEEE Int. Symposium on Multiple-Valued Logic* (2000) pp. 411–420